



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 8, August 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.118

 9940 572 462

 6381 907 438

 ijirset@gmail.com

 www.ijirset.com

LPF and HPF designing in 1-D & 2-D DWT based on 9/7 Wavelet Coefficient: A Study

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ABSTRACT—Discrete wavelet transform provides an efficient computing method for sparse representation of wide class of signals. The DWT only analyzes the lower frequency sub bands implicitly ignoring any information embedded in the higher frequency sub bands. There are few applications where signal information is equally distributed in the entire signal spectrum. In this paper, a high speed area efficient 1-D & 2-D discrete wavelet transform (DWT) using 9/7 filter based canonical signed digit (CSD) Technique is described. Being an area efficient architecture free of ROM, multiplication, and subtraction, CSD can also expose the redundancy existing in the adder array consisting of entries of 0 and 1.

KEYWORDS: - 1-D Discrete Wavelet Transform (DWT), CSD Technique, Low Pass Filter, High Pass Filter, Xilinx Simulation.

I. INTRODUCTION

The digital signal processing (DSP) has become an integral part of everyday life. The increasing number of electronic devices has led to a situation where almost everyone has to deal with digitally processed data. A digital signal can be a sequence of samples extracted from a continuous signal or any discrete set of data like, e.g., image in bitmap form. However, still more often, the digital signal is directly derived from the continuous signal as its representation [1].

Nowadays, numerous computational problems are so complex that they not only require computer aided processing, but also a very efficient processing of huge data sets, often in real time [2]. Therefore, there are efforts to optimize the known algorithms both from the perspective of the processing time and the precision of the results as well. Current processors are often optimized to extreme physical operational conditions, e.g., the widths of the electric paths are regularly close to the atomic size. This causes the need to look for new techniques to increase the computational efficiency. Increasing the frequency also meets the physical barriers. Those are only a few of the reasons why parallel computing is becoming more and more popular [3, 4]. The conversion of traditional, sequential computation algorithms to their parallel counterparts requires suitable implementations and poses a real challenge for software engineers involved in algorithm optimization [5].

The quality of the developed algorithms is, of course, subject to evaluation. There are different evaluation methods. Often we refer to computational complexity or time complexity. In the case of parallel devices and, in particular, graphics cards, the problem is much more complicated. The number of basic operations such as arithmetic, logic, and memory accesses does not directly affect the actual computation time. Extra parameters like versatility, simplicity, ease of implementation, ease of modification, utilization of hardware resources, achieved acceleration, complexity of communication, synchronizations, portability and others are also highly important. Among these and other reasons, time efficiency models are created for specific architectures. In the end, it often eventually turns out that only experimental studies give a real insight into performance characteristics of a chosen computational method. Software designers always try to minimize the computational complexity, memory usage or other criteria of the overall cost [6]. However, such approaches are not always successful. It is quite often the case that a simpler algorithm with worse traditional computational complexity performs better because of the advantages resulting from its computational structure design.

II. DISCRETE WAVELET TRANSFORM

An important reason for transforming data from one form into another is the desire to analyze the features of the signal that are more visible after the transformation than in the original form. Such transformations are also sometimes called

mappings. The fundamental group of transformations is linear transformations which are one of the axioms of linear algebra. These are homomorphic mappings preserving the spatial structure. A special case of linear transformations is orthogonal ones possessing an important property of their inverse matrix being the transposition of the forward one. Computing the inverse matrix for multidimensional data can be a much more complex problem than a simple transposition for transformations. It is common to use harmonic functions as basic functions due to the fact that harmonic signals do not change their shape after passing through a linear system (only their phase and amplitude changes) [7].

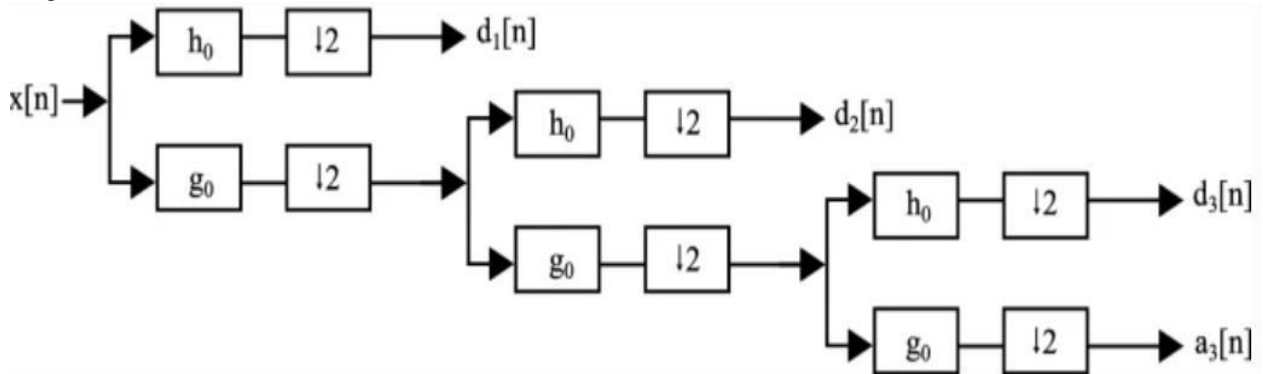


Fig. 1: Example decomposition tree of DWT with filters h and g

Wavelet transformation can be implemented using low-pass and high-pass filters. The organization of the calculations means that in each step, the high-pass filter produces detailed results, while the result of the low-pass filter depends on the scaling function. Thus, the time resolution remains at a good level for high frequencies and the frequency resolution remains at a good level for low frequencies. The number of decomposition stages depends on the size of the transform. The reconstruction process is based on the inverted version of the scheme presented in Fig. 1.

III. LITERATURE REVIEW

Jhila Jana et al. (2021, [1]), a point by point investigation of exceptionally enormous scope coordination (VLSI) models for the one-layered (1-D) and two-layered (2-D) discrete wavelet change (DWT) is introduced in numerous viewpoints, and three related designs are proposed too. The 1-D DWT and opposite DWT (IDWT) designs are arranged into three classifications: convolution-based, lifting-based, and B-spline-based. They are examined with regards to equipment intricacy, basic way, and registers. With respect to the 2-D DWT, the huge measure of the casing memory access and the bite the dust region involved by the inserted inner cradle become the most basic issues. The 2-D DWT designs are sorted and examined by various outer memory filter strategies. The execution issues of the inward cradle are additionally talked about, and some genuine tests are given to show that the region and power for the inner support are exceptionally connected with memory innovation and working recurrence, rather than the expected memory size as it were. Other than the investigation, the B-spline-based IDWT engineering and the covered stripe-based check technique are likewise proposed. Last, we propose an adaptable and productive engineering for a one-level 2-D DWT that takes advantage of many benefits of the introduced examination.

Zhang et al. (2019, [2]), a clever inner collapsed equipment productive engineering of staggered 2-D 9/7 discrete wavelet change (DWT) is proposed. For staggered DWT, the unfurled structure is to a greater extent utilized contrasted and the collapsed structure, in view of its low memory utilization and low time delay. Notwithstanding, a bunch of information substantial each couple of clock cycles caused the befuddle among clock and information in the unfurled structure. The bungle normally should be addressed by multi-clock or complex information change, which expands the utilization of equipment assets and the intricacy of the general framework. To take care of the above issue of the unfurled structure, we change the information input timing by utilizing a solitary clock space and collapsing the DWT design of various levels in shifting degrees, as per their own clock-to-information proportions. For a picture of size of $N \times N$ pixels and 3-level DWT, the proposed design requires just 6N words fleeting memory. For 3-level DWT with a picture of size 512×512 pixels, the equipment assessment and correlation of the current structures show that, the equipment assessment result shows something like 30.6% region delay-item (ADP) decline, and no less than 22.4% semiconductor delay-item (TDP) decline for $S = 8$, and 25.77% semiconductor delay-item (TDP) decline for $S = 16$.

Mishra et al. (2017, [3]), ongoing combination of pictures procured from numerous sensors is huge in different fields, including military and aeronautics, to diminish the vulnerability in the gained pictures and for more extensive fleeting and spatial inclusion. Current ways to deal with multi-sensor picture combination have a high computational intricacy and challenging to carry out in equipment. This paper presents a technique in light of two-scale deterioration and altered Frie-Chen administrators to combine pictures gained from infrared and apparent picture sensors and its relating equipment execution. The proposed strategy accomplishes 48%, 15%, and 100 percent upgrades in complete edge moves, primary comparability, and night vision contrast, separately, regarding those of the most recent distributions known to the creators. The relating equipment design, orchestrated utilizing the Xilinx device, is displayed to consume 4% of the assets in the Virtex 4 field programmable entryway exhibit (FPGA-xc4vlx200). The proposed design has one unit of throughput for each clock cycle and can handle 30 top quality pictures/sec. The proposed engineering is additionally broke down utilizing the abstract plan vision device with the 90-nm UMC standard integral metal-oxide-semiconductor cell library. It is observed that the design consumes 251.6 mW of force and has a region identical to 580K NAND2 entryways. The lower equipment asset necessity and backing of parallelism and pipelining make the proposed calculation appropriate for low-power, ongoing picture combination applications.

Pemmaraju et al. (2017, [4]), picture combination is an information combination innovation which keeps pictures as primary exploration contents. It alludes to the methods that coordinate multi-pictures of similar scene from various picture sensor information or incorporate multi pictures of similar scene at various times from one picture sensor. In this paper Wavelet based Image combination calculation is utilized and executed on a Field-Programmable-Gate Array-based equipment framework utilizing a Xilinx Platform Studio EDK 10.1 FPGA Spartan 3E is carried out. The FPGA innovations offer fundamental computerized blocks with adaptable interconnections to accomplish fast advanced equipment acknowledgment. The FPGA comprises of an arrangement of rationale blocks, like Look up Tables, doors, or flip-failures and some measure of memory. At long last, the proposed calculation in this task was applied to trials of multi-center picture combination and correlative picture combination. The calculation will be moved from PC to FPGA board utilizing JTAG link. The outcome will be moved back to framework to examine equipment asset taken by FPGA utilizing Visual Basic.

Samit Kumar Dubey et al. (2017, [5]), abridge the circuit intricacy and enhance the execution are proposed; DWT is applied to the periodic and non-periodic signal that used to speech and video signal. This paper designed 9/7 DWT based on DA and KSA. The drawback of this paper is KSA not proper work in all the binary bits and sources of info, which profoundly expands the circuit unpredictability. Proposed procedures depends on rapid region productive 2-D discrete wavelet change (DWT) utilizing 9/7 channel based altered Distributed Arithmetic (MDA) Technique also, kogge stone snake. MDA strategy is connected to low and high pass channel of the discrete wavelet change. This method comprises of viper, move enroll and free of multiplier. Plan and result are actualized in Xilinx programming and confirmed resistor exchange level (RTL) and waveform.

Rakesh Biswas et al. (2017, [6]), proposed a programmable one-dimensional discrete wavelet packet transform processor. Compared with existing architectures, the proposed processor can carry out both wavelet pieces of data to be abandoned are located. In any case, the picture pressure innovation has turned into a mainstream decision for dealing with the very mind boggling spatial determination of the current picture catching sensors. The fantastic video transmission for TV and media has additionally lifted the utilization of picture pressure. In addition picture pressure attempts an important association in various basic and incalculable applications, for example, Video conferencing, TV, biomedical imaging, remote detecting (utilizes satellite symbolism for atmosphere and earthly data total), copy transmission (FAX)[7], space investigation, records handling and transmission, controlling remote vehicle for military, squander administration, and so on.

Mamatha I. et al. (2016, [7]), the previously mentioned application particularly demonstrates the necessity for sufficient capacity, significant data transfer capacity for transmission, and delayed transmission period for picture, sound, and video signals. In this present circumstance, the innovation that can be gotten to and executed under these conditions is the picture pressure. Picture pressure gives answer for every one of the difficulties looked in above zones. It lessens the measure of sight and sound information required for capacity and transmission. It packs the information, at that point stores it or transmits it. At the point when the information is required to be perused, at that point the picture decompression replicates the first data. For example, when the pressure proportion is 32:1, at that point the capacity zone, exchange speed, data transfer capacity utilization and transmission postpones requirements can be limited by a factor of 32, with no misfortune in quality. The portrayal of the photo is first changed from the given spatial space to substitute area with the assistance of well-known flag changing and coding procedures.



Maurizio Martina et al. (2015, [8]), the existing method consumed more memory is used to storing the intermediate computational multiplier based DWT. The DWT has to process massive amounts of data at high speed, making it unsuitable for real time image compression with better performance. The objective of the research work is to derive efficient architectures for the hardware implementation of the multiplier-less DWT, compared to the existing architectures.

Basant Kumar et al. (2013, [9]), the optimization factors are the speed, low area and hardware complexity involved, with the size of the given input image and the required levels of decomposition. The modified distributive arithmetic (MDA) based DWT architecture for the 9/7 wavelet filter coefficient multiplier-less architecture is optimized, to achieve better speed and higher hardware utilization, by using a single clock for the predict and update operations.

In the cutting edge mechanical industry, it is very difficult to go over a field that isn't impacted by the advanced picture preparing. It assumes a vital part in all specialized areas, somehow. Keeping in mind the end goal to keep up a conservative portrayal, just few applications are depicted that are identified with the proposed work. By and large, the fields that make utilization of advanced picture handling can be divided into morphology, criminology, photography, microscopy, biomedical imaging, remote detecting, transportation, explore sciences, military application, and numerous others.

IV. CSD TECHNIQUE

Let us consider the following sum of products [4]:

$$R = \sum_{k=1}^L X_k \times Y_k \tag{1}$$

Where X_k are fixed coefficients and they Y_k are the input data words. Equation (1) can be expressed in the form of a matrix product as:

$$R = [X_1 \quad X_2 \quad \dots \quad X_L] \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_L \end{bmatrix} \tag{2}$$

Both X_k and Y_k are in two's complement format. The two's complement representation of X_k may be expressed as

$$X_k = -X_k^M 2^M + \sum_{i=N}^{M-1} X_k^i 2^i \tag{3}$$

Where $X_k^i = 0$ or 1 , and $i = N, N+1 \dots M$ and X_k^M is the sign bit and X_k^N is the least significant bit (LSB).

Equation (3) can be expressed in matrix form as:

$$X_k = [2^N \quad 2^{N+1} \quad \dots \quad 2^M] \begin{bmatrix} X_k^N \\ X_k^{N+1} \\ \vdots \\ -X_k^M \end{bmatrix} \tag{4}$$

Similarly Y_k can be represented in two's complemented format as:

$$Y_k = -Y_k^X 2^X + \sum_{i=W}^{X-1} Y_k^i 2^i \tag{5}$$

Where $Y_k^i = 0$ or 1 , and $i = W, W+1, X$ and Y_k^M is the sign bit and Y_k^N is the least significant bit (LSB).



Now on combining equations (1) and (3), we get-

$$R = -(R^M \cdot 2^M) + \sum_{i=N}^{M-1} (R^i \cdot 2^i) \tag{6}$$

Where

$$R^i = \sum_{k=1}^L X_k^i Y_k, \quad i = N, N+1 \dots M$$

Table 1: present the high-pass and low-pass wavelet filters coefficient

	Wavelet filters coefficients	Multiplied by 128	7 bit binary representation
h_0	0.60294901823	77	1001101
h_1	0.26686441184	34	0100010
h_2	0.07822326652	10	0001010
h_3	0.01686411844	2	0000010
h_4	0.026748757410	3	0000011
g_0	0.55754352622	71	1000111
g_1	0.29563588155	38	0100110
g_2	0.02877176311	4	0000100
g_3	0.045635881557	6	0000110

V. VLSI SYSTEM

DWT algorithms can be implemented in a programmable system such as general purpose computer or digital signal processor. These programmable systems use a fixed computing architecture and perform arithmetic operations sequentially and they offer limited throughput for computationally intensive algorithms such as DWT. However, DWT algorithms can be implemented general purpose programmable systems for high-throughput applications employing parallel processing. Engaging general purpose programmable system to perform a specific task is not cost-effective. Besides, general purpose computing systems occupy substantial amount of space and consumes power which makes the deployment of signal processing system difficult in a resource constrained and hostile environment. In recent years, there is tremendous growth of portable and wireless devices in various applications. Portable and wireless devices are resource and power constrained, and uses complex signal processing algorithms including DWT. Besides, high-throughput rate, low-area and low-power are considered the key requirements of systems implementing digital signal processing algorithms especially for portable and wireless devices which are battery operated. Therefore, realization of DWT in resource and power constrained environment and delivering real-time performance is a challenging task for portable and wireless devices.

VI. CONCLUSION

In this paper studied of canonical signed digit paradigm named CSD for VLSI implementation of digital signal processing (DSP) algorithms involving inner product of vectors and vector-matrix multiplication. Mathematical proof is given for the validity of the CSD scheme. The CSD is a very efficient architecture with adders as the main component and free of ROM (free memory), multiplication, and subtraction. For the adder array, a systematic approach is introduced in this paper to remove the potential redundancy so that minimum additions are necessary. CSD is an accuracy preserving scheme and capable of maintaining a satisfactory performance even at low CSD precision.

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