



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJIRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 3, March 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 7.569

 9940 572 462

 6381 907 438

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Review of Different Types of Reversible Shift Register Based on Sequential D-FF Circuit

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ABSTRACT: Reversible computations have attracted a lot of attention in recent years due to the ability to reduce energy dissipation that is needed in nano circuits. The main purpose of designing reversible circuits is to reduce the energy consumption that occurs due to the loss of input bits in irreversible circuits. In this paper, the studied of sequential circuit and shift register is introduced. Four types of reversible shift register including serial-in to parallel-out (SIPO), parallel-in to parallel-out (PIPO), parallel-in to serial-out (PISO) and serial-in to serial-out (SISO) are studied using the reversible flip-flop. The shift register is one of the most extensively used functional devices in digital systems. A shift register consists of a group of flip-flops connected together so that information bits can be shifted one position to either right or left depending on the design of the device. The end of the paper expected result and conclusion is explain.

KEYWORDS: SISO, SIPO, PISO, PIPO, Reversible Gate

I. INTRODUCTION

A digital circuit plays a vital role in the present communication era, use transistors to produce logic gates in order to realize various arithmetic and logical expressions. The benefits of digital circuits are better noise margin and quality than analog circuits. The error detection and correction is also easier with digital signals. One of the basic components in the digital circuit is a shift register. In many applications such as digital filters, processor in personal computers, communication receivers and image processing Integrated Circuits (IC) is a generally used instance [1, 2]. In recent days the requirement of the shift register is increased in terms of word length, to handle the large size and high quality images in the image processing ICs. A 4K-bit and a 2K-bit shift registers are utilized in the image extraction as well as vector generation in VLSI chips and 10-bit 208-chain Liquid Crystal Display (LCD) column driver IC respectively. It is fairly simple to design a shift register by connecting the required number Flip-flops in series based on its length up to N-bits. There is no circuit between the Flip-flops in the shift register; Flip-flops have superior speed than area and power consumption. The smallest Flip-flop is ideal to reduce area and power consumption by using the shift register. In many applications, pulsed latches have recently replaced Flip-flops, as a pulsed latch is much smaller than a flip-flop. However, due to the existence of timing problem, the pulsed latches cannot be used in a shift register [3].

A linear feedback shift register is a combination of series of flip flop and XOR or XNOR logic gates. Its output is pseudo randomly cycle through a sequence of binary values after certain number of clock cycle [4, 5]. The repetition of random output depends on the number of stages in the LFSR. Therefore, it is an important component in communication system where, it play important role in various application such as cryptography application, CRC generator and checker circuit, gold code generator, for generation of pseudorandom sequence, for designing encoder and decoder in different communication channels to ensure network security, Design for Test (DFT) and Built in Self-Test design (BIST).

A linear feedback shift register is linear in the sense that its input bit is a linear function (XORing or XNORing) of LFSR previous state [6].

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. The power dissipation during the test mode is 200% more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. Linear feedback shift registers have multiple uses in digital systems design. Here we have implemented a 32 bit length sequence on FPGA using VHDL with maximum length feedback polynomial to understand the memory utilization and speed requirement. Also, we have presented the comparison of performance analysis based on synthesis and simulation



result as well identify the simulation problem for long bit LFSR. The target device we have used Xilinx Spartan 3A and performed simulation and synthesis using Xilinx ISE. The HDLs are VHDL and Verilog. We prefer VHDL for programming because it is widely used.

II. LITRATURE REVIEW

B. Naresh Kumar Reddy et al. [1], pseudorandom Number Generator (PRNG) are utilized in Built in Self Test (BIST) to lessen testing cost and time. The direct criticism shift register (LFSR) design generator is generally utilized in creating test vectors for PRNG. LFSRs play an indispensable job in producing test vectors in equipment check or testing and they are additionally utilized in the cryptography region. This paper gives the plan of 4-digit LFSR 2 Phase-timed Adiabatic Static CMOS Logic (2-PASCL) and Reversible Rationale Gates (RLG). The proposed 4-bit LFSR is integrated and reproduced utilizing Vivado configuration suit 2018.3 and executed on a Kintex-7 FPGA board. Contrasted and the outcomes acquired with notable LFSR designs, the proposed technique is utilized to work on the presentation, and diminishing the power utilization what's more, area of processors.

Sonam Gour et al. [2], during the time spent enormous scope incorporation parcel of semiconductors are carried out in an exceptionally least region. Combinational rationale has extremely valuable in quantum and numerous modern plans. Diminishing the power and postponement is the rule object in VLSI plan. Smothering sub-limit spillage current in enormous scope joining is fundamental for accomplishing green processing and working with the more utilization of force hardware. In this paper the shift register is executed regardless of MTCMOS procedure. The Cosmos Scope instrument is utilized to dissect the power delay with the reproduction in HSPICE. The Shift Register is manufactured by utilizing the 32nm and 45nm BPTM model document. With the assistance of MTCMOS method in Shift Register a decrease in spillage power is 44% in 32nm with the applied voltage of 0.7V and 57% in 45nm with the applied voltage of 0.9V. Energy is decreased by the 5% for 0.7V for 32nm and 21% for 0.9V at 45nm.

S. Gupta et al. [3], reversible circuits are one of the most encouraging advancements that permit the proliferation of the contributions from the noticed results and hence decreasing the power scattering as hotness. Numerous fundamental and all inclusive rationale doors for example nand, nor, or, and so on are irreversible and bring about energy utilization during estimations. In the reversible innovation, similar to quantum circuits energy isn't consumed during the whole computation process and these circuits can be utilized for low-power and quantum correspondence applications circuits. Counters are considered as quite possibly the main consecutive circuit utilized in some constant applications. This paper presents another way to deal with plan a quantum practical reversible up/down counter circuit utilizing elite or amount of item (ESOP) articulations and TR entryways. The proposed counter circuits are reproduced in the Xilinx Vivado test system to check the usefulness of the proposed plans. The relative review demonstrates that the proposed counters are better than the best past plans as far as quantum cost (QC) and door count (GC). In addition, they are exceptionally near or better than the beforehand accessible plans as far as trash yields (GO) and Ancilla inputs (AI).

Karthik et al. [4], superior execution goes back and forth are dissected and arranged into two classes: the restrictive precharge furthermore, the restrictive catch innovations. This grouping depends on the most proficient method to forestall or lessen the excess inside exchanging exercises. Another flip-flop is presented: the restrictive release flip-flop (CDFF). It depends on another innovation, known as the contingent release innovation. This CDFF decreases the inner exchanging exercises, yet additionally produces less misfires at the result, while keeping up with the negative arrangement time furthermore, little - to-defer attributes. With an information exchanging movement of 37.5%, the proposed flip-flop can set aside to 39% of the energy with the very speed as that for the quickest beat back-peddles.

G. Prakash et al. [5], quantum-dab Cellular Automata (QCA) is arising nanotechnology that can address paired data utilizing quantum cells without current streams. It is known as a promising option of Complementary Metal-Oxide Semiconductor (CMOS) to address its downsides. Then again, the shift register is quite possibly the most broadly involved functional gadgets in computerized framework. Additionally, QCA can possibly accomplish alluring elements than semiconductor based innovation. Be that as it may, tiny scope and Nano-manufacture limits force an obstacle to the plan of QCA-based circuits and require for shortcoming lenient investigation is showed up. Accordingly, the point of this paper is to plan and reproduce an advanced a D-flip-flop (as the principle component of the shift register) in view of QCA innovation, which is stretched out to plan an upgraded 2-bit general shift register. This paper assesses the presentation of the planned shift register within the sight of the QCA shortcoming. Gathered outcomes utilizing QCA Designer apparatus exhibit the shortcoming lenient component of the proposed plan with least timing and region utilization.



Partho Ghose et al. [6], reversible rationale is an arising innovation that assumes a significant part in the fields of low power calculation and can be applied in cryptography, interchanges, quantum figuring and so forth Reversible shift registers are quite possibly the main component in creating reversible memory circuits. In this paper, we present effective plan of various reversible shift registers, for example, Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out and Parallel In Parallel Out registers. We have likewise laid out suitable lemmas to show various properties of the proposed plans. Reasonable calculations for planning the reversible shift registers are likewise referenced. Near investigation uncovers that our proposed plan requires negligible number of reversible entryways and steady information sources, and furthermore creates less number of trash yields than the cutting edge plan. Besides, to explain the legitimacy of our plan, every one of the proposed circuits have been recreated utilizing DSCH3.

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III. PROBLEM STATEMENT

The primitive is not a parallel load shift register, but a solution to the parallel load problem comes through observing exactly what is happening during the last N chip periods of an N -stage LFSR. Consider an eight-stage LFSR that has just reached a condition where it is eight chip rate clock cycles. During these last eight clock cycles, the contents of the shift register are shifted out as the last eight states of the sequence. Also during this eight-cycle period, the XOR feedback path will be generating eight new bits to inject into the shift register as the next eight bits of the sequence. However, the eight feedback bits calculated during the last eight cycles of the current sequence will not be shifted out as part of the sequence because they will be overwritten by the bits.

IV. SHIFT REGISTER

This sequential device loads the data present on its inputs and then moves or “shifts” it to its output once every clock cycle, hence the name Shift Register.

A shift register basically consists of several single bit “D-Type Data Latches”, one for each data bit, either a logic “0” or a “1”, connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be “SET” or “RESET” as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

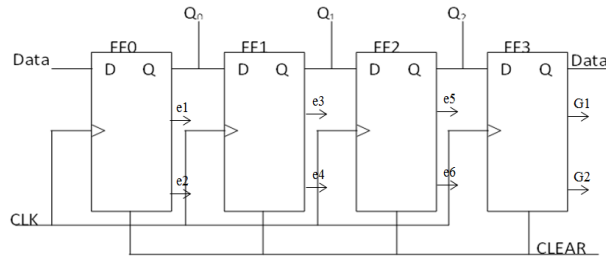


Figure 1: Flow Diagram of Serial in Parallel Output Shift Register

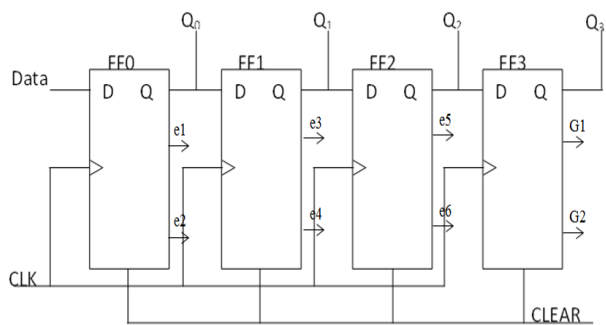


Figure 2: Flow Diagram of Parallel in Serial Output Shift Register

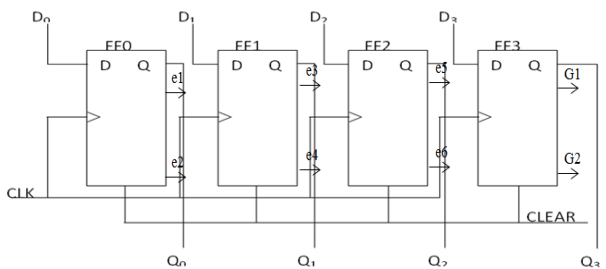


Figure 3: Flow Diagram of Parallel in Parallel Output Shift Register

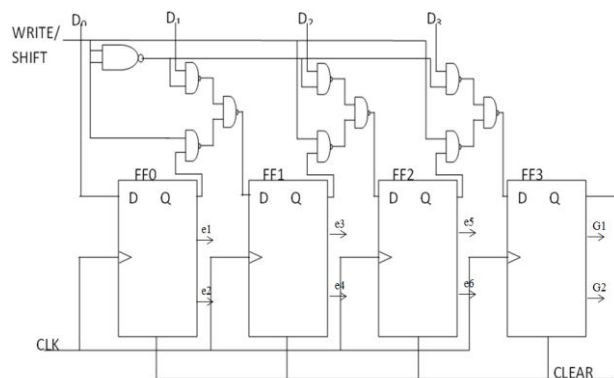


Figure 4: Block Diagram of Reversible Parallel in Serial out Shift Register

V. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gate available. It is most commonly used for fan out purposes. The 3x3 reversible gates include

Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

o BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 5, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

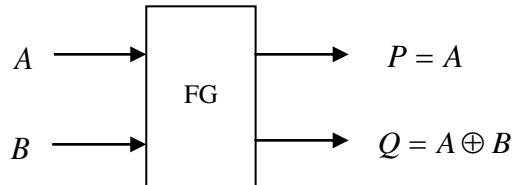


Figure 5: Feynman gate

In figure 6, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

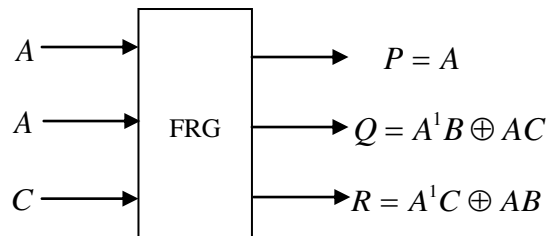


Figure 6: Fredkingate

Figure 7 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

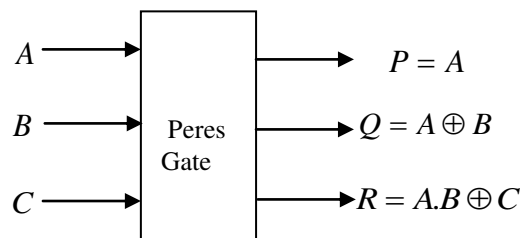


Figure 7: Peres gate

The HNG gate, presented in fig, produces the followinglogical output calculations:

$$P = A \tag{1}$$

$$Q = B \tag{2}$$

$$R = A \oplus B \oplus C \tag{3}$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \tag{4}$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 8.

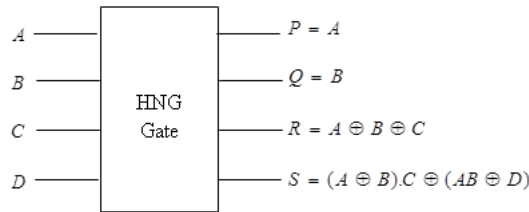


Figure 8: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \tag{5}$$

$$Q = A \oplus B \tag{6}$$

$$R = AB \oplus C \tag{7}$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \tag{8}$$

Fig. 9 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

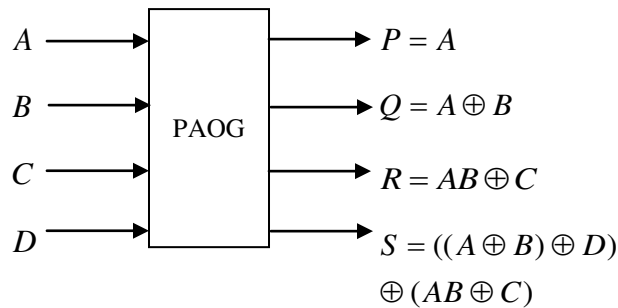


Figure 9: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the following logical output calculations:

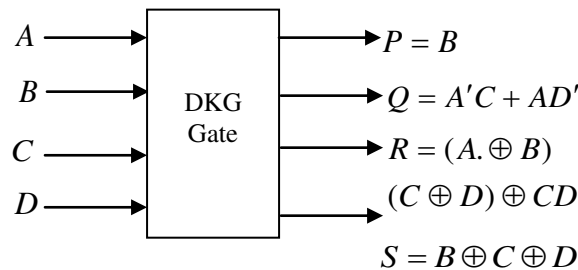


Figure 10: DKG Gate

$$P = B \tag{9}$$

$$Q = A'C + AD' \tag{10}$$

$$R = (A \oplus B)(C \oplus D) \oplus CD \tag{11}$$



$$S = B \oplus C \oplus D \quad (12)$$

VI. EXPECTED RESULT

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

- Design 4-bit, 8-bit, 16-bit, 32-bit and 64-bit register with the help of logic gate and flip flop.
- All design are implemented using Xilinx Software for different device family and calculate various parameter i.e.
- Number of Slice
- Number of LUTs
- Number of Flip Flop Pair
- Number of Input Output
- Delay

All design will be compared with the previous base paper (2020) in different device family and achieved good result.

VII. EVALUATION PARAMETERS

Number 4-input LUTs:-LUT stands for look up table that “reduces the complex mathematics calculations and provide the reduced processing time”.

Number of Slices:-“How many areas are used in this circuit” is called number of slices.

Number of IOBs:-“All input output port used in this circuit are combined” called number of input output buffer switch.

Maximum Combinational Path Delay:- “How many time of the result is the output of the digital circuit should from level 0 to level 1” are called maximum combinational path delay (MCPD).

VIII. CONCLUSION

In this paper, reversible logic synthesis was carried out for SISO shift register. Efficiency of the proposed design was clearly highlighted by means of comparison table which proves that the new design is clearly better than the existing one in every aspect. The key contribution of this paper is the efficient reversible realization of SIPO, PISO, PIPO and universal shift registers which are the first ever proposed in the literature of reversible logic. Lower bounds of the proposed designs were established by providing relevant theorems and lemmas. The proposed designs have the applications to perform serial-to-parallel and parallel-to serial conversions. This work forms an important step in the building of complex reversible sequential circuits for quantum computers. An interesting future work could be to develop efficient reversible counter and barrel shifter circuits.

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