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Department of ECE, Adhiyamaan College of Engineering, Hosur, Tamilnadu, India

Design and Implementation of High-Throughput and Low Power Efficient Pipeline FFT Processor for OFDM Systems

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ABSTRACT: This paper comprises of an investigation of Fast Fourier Transform (FFT) designs which are the foundation of any OFDM based remote organizations. By utilizing the FFT ideas we are in fact in building up an effective structures for remote organizations which are normal in all over .This paper will explicitly address the force proficient plan of a FFT processor as it identifies with arising OFDM correspondences, for example, intellectual radio .Increasing paces and unpredictability of remote correspondence frameworks have required the advancement and progression of superior sign handling components, Our ideas are simply founded on being developed we need by utilizing (FPGA), These assets incorporate force, memory, and chip region. Progressing research looks to enhance asset utilization just as execution. Configuration turns into an equilibrium and bargain of adaptability, execution, multifacetednature and cost.

KEYWORDS: OFDM,FFT processor, Fault-tolerant, Pipelining

I. INTRODUCTION

In OFDM means orthogonal frequency-division multiplexing (OFDM) is a type of digital transmission and a method of encoding digital data on multiple carrier frequencies. In OFDM, multiple closely spaced orthogonal subcarrier signals with overlapping spectra are transmitted to carry data in parallel.

Cognitive radio is a strategy for remote correspondence via powerfully adjusting the various subcarriers to transmission changing conditions in the correspondence channels. The subcarriers are empowered by a balance plot referred to as orthogonal frequency division multiplexing (OFDM). OFDM changes over a high information rate signal into various lower information rate signals for concurrent transmission through various channels. The Fast Fourier Transform processor is the core of OFDM that empowers its quick and productive adjustment of signs. The FFT calculation is a quick calculation of the Discrete Fourier Transform which is a fundamental part of the balance plot utilized in OFDM. As the FFT processor is the most computationally escalated segment in OFDM correspondence, an improvement in the force productivity of this segment can impactly affect the general framework. These effects are huge considering the quantity of portable and far off specialized gadgets that depend on restricted battery-fueled activity. This undertaking will fill in as an investigation of current FFT processor calculations and models just as improvement methods that mean to decrease the force utilization of these gadgets. Super Wideband (UWB) Technology brings the accommodation and portability of remote correspondences to rapid interconnects in gadgets all through the computerized home and office. Instead of wired connection, this technology enables wireless connection for transmitting video, audio, and other data with high data speed and low power consumption. After IEEE 802.15.3a was withdrawn in the Spring of 2006,

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Multiband-OFDM has been controlled by ECMA International. However, some key issues need to be solved for designing CMOS based Multiband- OFDM UWB solution in support of the low power requirement. One of the issues focuses on its FFT (Fast Fourier Transform) block, which takes 25% design complexity of the total digital baseband transceiver.

Although many results have already been published in this research area in the past few years, some key problems still exist and need to be improved for the speed, area and power consumption consideration. In light of ECMA-368, for the necessity of Multiband-OFDM framework, this FFT processor should deal with a couple hundred MHz, which makes it hard to execute. Furthermore, since this framework focuses for the remote convenient gadgets, little territory and low force utilization are likewise basic. Hence, this theory centers around the region and force utilization improvement under the ECMA-368 standard necessities. To achieve this goal, a couple of stages should be followed. The underlying advance is to find the points of interest for this FFT processor, which is directed by the Multiband OFDM UWB standard. The movement requires the examination on OFDM and UWB development and the goals of its FFT processor. Resulting to describing the points of interest, overhauled FFT count and configuration should be used for these subtleties. There are an enormous number of FFT calculations and structures in the sign preparing writing.

Subsequently, the condition of workmanship calculations and structures should be broke down and analyzed. In view of various calculations and designs, diverse force utilizations, zone and speed of the processor will be accomplished. So their ASIC appropriateness should be examined and the exertion should be centered around the picking calculations and structures and improvement. Besides, the improvement space should be investigated and the engineering should be additionally upgraded. The proposed calculation and design should be approved by reenactment before usage. After that, this circuit needs to be implemented with VHDL. The synthesis step is followed by using both Simplify Pro targeted for FPGA and style Compiler for ASIC. For this, each carrier may use one among the several available digital modulation techniques..

II. RELATED WORK

FFT pruning calculations and structures [9] are intended for figuring specific recurrence receptacles on the range however not for mirroring the asset designation conspire in the OFDMA framework. Subsequently in this concise, we propose the unfinished stored FFT calculation for common asset block (RB) dispersions within the OFDMA framework. Besides, we design a mixed pipelined/cached-FFT processor with constellation and power awareness. Finally, we implement and measure the FFT processor chip to point out its energy efficiency.

We use two cache sets to facilitate the data transfers between butterfly processor and the cache sets and between the caches and the main memory. The cache sets must perform two write operations and two read operations in one clock cycle for the dual-stream processing. To avoid the utilization of the write-port cache and simplify the control complexity, we divide each cache set into two banks for even and odd addresses.

III. METHODOLOGY

The proposed FFT system comprises of one pre-stage, $\log_2 N - 1$ SDC stages, one post-stage, one SDF stage, and the slightest bit reverser, The pre-stage rearranges the Complex information to another arrangement that comprises of genuine part followed by the comparing nonexistent part, appeared in Table 1.

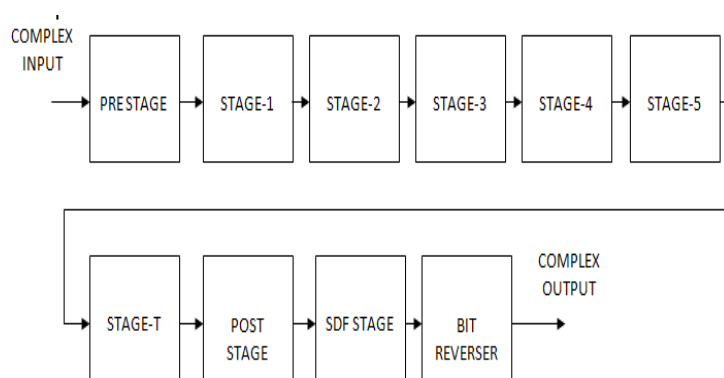
The contrasting post-stage modifies back the new progression to the unpredictable arrangement. The SDC stage ($t = 1, 2$)

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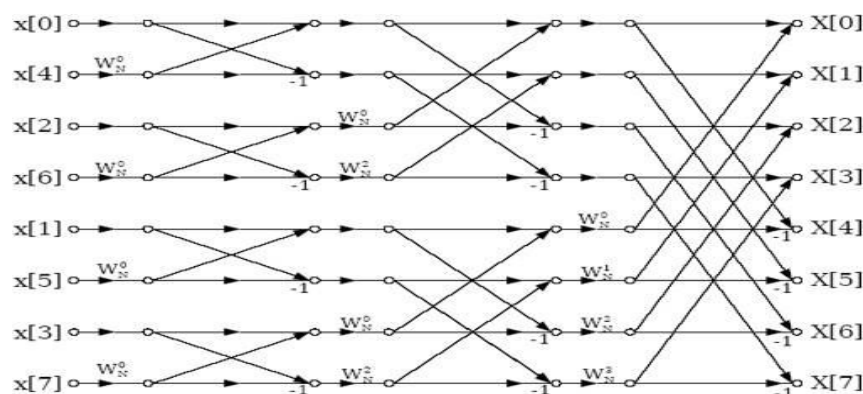
comprises of genuine part followed by the comparing nonexistent part, appeared in Table 1



The contrasting post-stage revamps back the new progression to the mind boggling setup. The SDC stage ($t = 1, 2,$

..., $\log 2N - 1$) contains a SDC PE, which may accomplish 100% math asset usage of both complex adders and sophisticated multipliers. Last, the even information are recovered in ordinary request. Along these lines, the touch reverser requires just $N/2$ information support. The last phase of Single Delay Feedback (SDF) is indistinguishable from the radix-2 Single Delay Feedback (SDF), containing a perplexing snake and a complex subtractor. By utilizing the altered tending to method12, the information with an even file are composed into memory in typical request, and they are then recovered from memory in bit turned around request while the ones with an odd file are reversed order.

Normally the Fast Fourier Transform architectures are working based upon the parallel architectures, so FFT's are consume large area and latency, in order to perform low area and latency we are in deed in developing the pruning the FFT's with help of Pipelining Data path, feed forward, feed backward. And some various architectures for reducing the area and delay of the FFT processors, there are various radix-2 based architectures such as R2MDC, R2SDF, R2SDC; these architectures are very useful in making the pipelined operation of FFT's.



The proposed system consists of the architecture that can be have the stage-1, stage-2, stage-3, stage-4, stage-5 all are designed for 64-point FFT architectures, as shown in the Figure Block diagram showing pipelined based radix-2 FFT for 8-point

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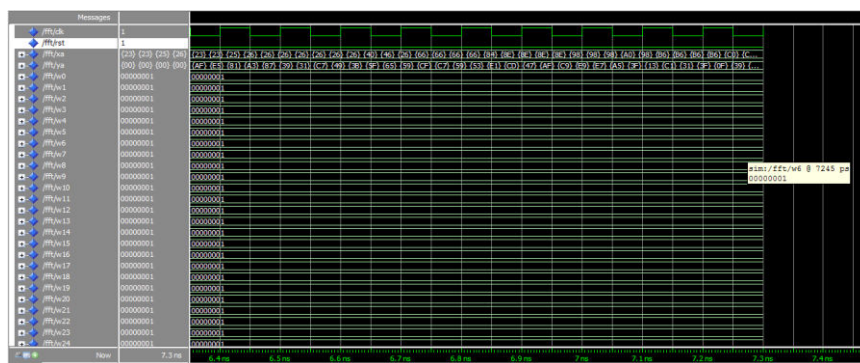
The proposed system consists of five stages and the stage-t which is also present in 64-point FFT architecture, All FFT based architectures are Operating based upon the parallel architectures, so we are proposing a Pipelined operation of FFT radix-2 architectures with combination of SDF-SDC architectures in order to achieve higher data rate. $\log_2(N - 1)$ contains a SDC PE, which may accomplish 100% math asset usage of both complex adders and sophisticated multipliers

four 8×13 caches, and four 128×13 ROMs. The function of the chip is verified, and its performance is measured using a digital test station. This chip can operate at maximum 51 MHz with 33.3 mw. We use the worst and best-case patterns for measuring the energy- saving capability of different RB allocation schemes, as shown in Fig. 4. Each curve represents a series of $\{1, 3/4, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64\}$ computed RBs in the whole OFDMA spectrum. We can see that the energy dissipation scales to the modulation order and the amount of the allocated resource.

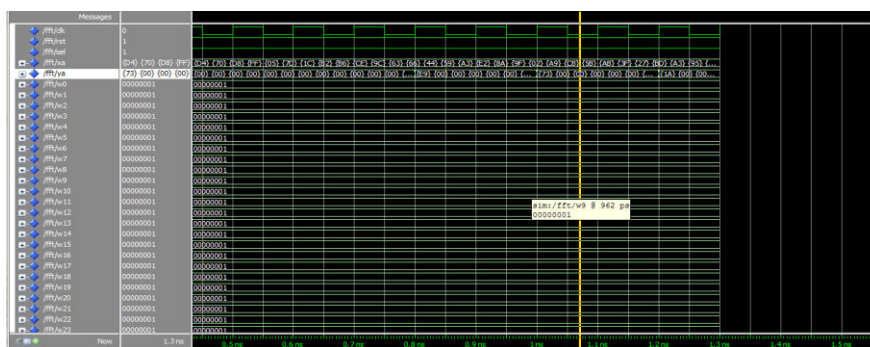
The comb-distributed scheme has the best performance, whereas the localized scheme has the worst performance. Note that the RB- level distributed scheme is a compromise between localized and comb-distributed schemes. Thus, its energy dissipation also lies between them. The energy scaling ranges from 1.90 to 0.64 nJ/FFT point for the 1024-point FFT, i.e., 67% energy can be saved in the FFT processor for minimal RB transmission. This result outperforms other cached- memory-based FFT chips. The latency for processing 1024-point full FFT is 61 μ s, which meets the 66.7- and 91.5- μ s OFDM symbol durations of the 3GPP-LTE and Mobile Wi MAX standards, respectively.

IV. RESULTS

The output show in the figure



Output screenshot showing simulation waveform for optimum multiplier based FFT.

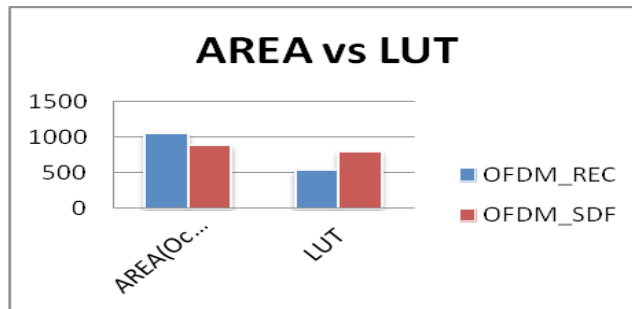


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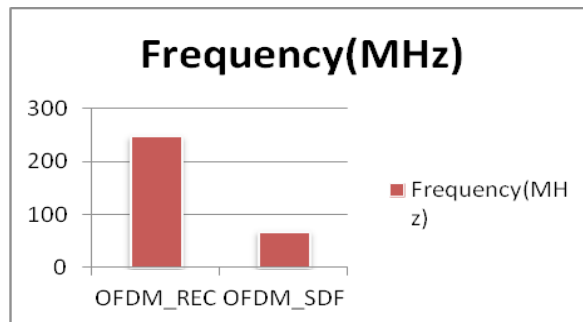
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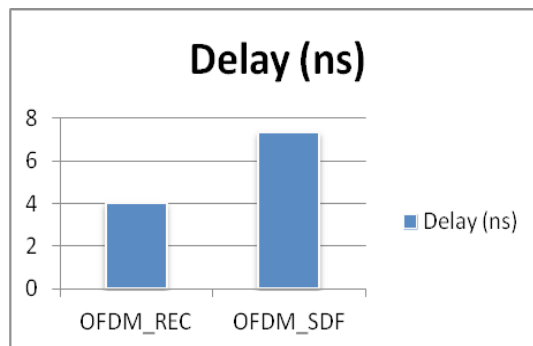
Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their AREA (slices) and LUT



Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their Frequency



Comparison chart showing OFDM with Radix-2 based FFT with OFDM based optimum multiplier and their Delay.



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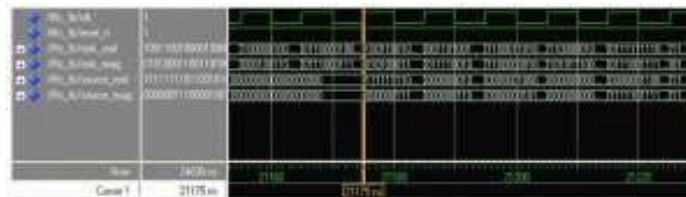
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.Table .Comparison table showing OFDM Radix-2 based FFT with OFDM based optimum multiplier

	AREA (Occupied Slices)	LUT	Delay (ns)	Frequency (MHz)	Power (W)
OFDM_REC	1053	539	4.014 ns	248.128	2.772
OFDM_SDF	890	797	7.340 ns	68.120	0.295

V. CONCLUSION

The input file length of our proposed pipeline FFT processor may be a parameter which may be decided at the range of 128, 512, 1024 and 2048 Take 1024 points FFT as an example. At first, the 1024 points FFT is coded using MATLAB software. After the chosen FFT algorithm is valid, the architecture of the processor was modeled in VHDL language and functionally verified using Xilinx 12.3i software and timing simulation using ISIM SE software. During the timing simulation, a test bench file included the TEXTIO package was written to read input data and write FFT result. The behavioral simulation waveforms for the Processor are shown in figure



REFERENCES

- [1] Cimini LJ. Analysis and simulation of a digital mobile channel using orthogonal frequency division multiplexing. *IEEE Trans Commun.* 1985; 665–75.
- [2] Lin YW, Liu HY, Lee CY. A 1 -GS/s FFT/IFFT processor for UWB applications. *IEEE J Sol-State Circ.* 2005; 40(8):1726– 35.
- [3] Cheng C, Parhi KK. High throughput VLSI architecture for FFT computation. *IEEE Trans. Circuits System II, Exp Briefs.* 2007 Oct; 54(10):339–44.
- Tang SN, Tsai JW, Chang TY. A 2.4-GS/s FFT Processor for OFDM-Based WPAN Applications. *IEEE Trans Circuits System II, Exp Briefs.* 2010 Jun; 57(6):451–5.
- [4] Jung Y, Yoon H, Kim J. New efficient FFT algorithm and pipeline implementation results for OFDM/DMT applications. *IEEE Trans Consume Electron.* 2005; 49:14–20.
- [5] ShinM, Lee H. A high-speed, four-parallel radix- 24 FFT processor for UWB applications. *Proceeding of IEEE ISCAS;* 2008. p. 960–3.
- [6] Y. W. Lin, H. Y. Liu, and C. Y. Lee, “A dynamic scaling FFT processor for DVB-T applications,” *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2005–2013, Nov. 2004.
- [7] T. H. Yu, C. Z. Zhan, Y. J. Cho, C. L. Yu, and A. Y. Wu, “Efficient fast Fourier transform processor design for DVB-H system,” in *Proc. 18th VLSI/CAD Symp.*,
- [8] C. P. Fan and G. A. Su, “A grouped fast Fourier transform algorithm design for selective transformed outputs,” in *Proc. IEEE APCCAS*, 2006, pp. 1939–1950
- [9] C80216m-08_503, Motorola IEEE

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