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# Review Paper of Binary Coders for Error Correction for Digital Converter using Wallace Tree Encoder

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**ABSTRACT:** Power consumption of analog and digital circuit design is will play major role in the world. Many researchers involved in designing the low power analog and digital circuits. The nature of signal is generated in real time is analog. Nowadays signal analyzes is done in digital for only to achieve low power, high accuracy, speed and less area. In the work, the VLSI architecture design for Wallace tree encoder with full adder is studied. In analog to digital conversion process, Wallace tree encoder is utilized in the process of converting the thermometer code to binary. This can be termed to be a high speed application and a flash type of flash ADC, which is a resistor ladder, encoder and comparator circuit. A suitable encoder is required for getting binary code from comparator output. In this paper is the studied of error correction and detection for digital converter. Different types of paper are survey and find the best technique for digital converter.

**KEYWORDS:** Decoder, Encoder, Wallace Tree Encoder, Digital Converter

## I. INTRODUCTION

Power consumption of analog and digital circuit design is will play major role in the world. Many researchers involved in designing the low power analog and digital circuits. The nature of signal is generated in real time is analog. Nowadays signal analyzes is done in digital for only to achieve low power, high accuracy, speed and less area [1-5]. So, the conversion of Analog to Digital is very important and also it is implemented in all real time signals processing analysis. The conventional analog to digital converter will consume more power. Some of the ADC developed in the last decade . High speed traditional to modernized converters is formulated and evaluated. A parallel structure of flash ADC will reduce the delay of the ADC when compared with conventional ADC [6]. Various low powers Wallace tree multipliers are designed [7]. Each reference voltage is connected to comparators in the architecture. The comparator compares and produces the output in the type of modern 0's and 1's when reference ladder generates the reference voltage. Then the binary value is converted into thermo code. The binary conversion is done by Wallace Tree encoder utilizing bubble error logic [8]. To synchronize the binary values each output comparator output is to make high conversion. Area, power increases and component number enhances exponentially. In order to generate a reference voltage for the  $2N - 1$  comparators are required  $N$ -bit flash ADC  $2N$  resistors. Thermometer code is nothing but the collection of comparator output. In order to change the code of thermometer to the code of binary is with the assistance of the simplified  $2N - 1 : N$  encoder.

Communication system transmits data from source to transmitter through a channel or medium such as wired or wireless. The reliability of received data depends on the channel medium and external noise and this noise creates interference to the signal and introduces errors in transmitted data. Shannon through his coding theorem showed that reliable transmission could be achieved only if data rate is less than that of channel capacity. The theorem shows that a sequence of codes of rate less than the channel capacity have the capability as the code length goes to infinity [1]. Error detection and correction can be achieved by adding redundant symbols to the original data called as error correction and correction codes (ECCs). Without ECCs data need to retransmit if it could detect there is an error in the received data. ECC are also called as for error correction (FEC) as we can correct bits without retransmission. Retransmission



adds delay, cost and wastes system throughput. ECCs is really helpful for long distance one way communications such as deep space communication or satellite communication. They also have application in wireless communication and storage devices [2].

Error detection and correction helps in transmitting data in a noisy channel to transmit data without errors. Error detection refers to detect errors if any received by the receiver and correction is to correct errors received by the receiver. Different errors correcting codes are there and can be used depending on the properties of the system and the application in which the error correcting is to be introduced. Generally error correcting codes have been classified into block codes, convolutional codes, LDPC Code and Goley Code [3, 4].

**Error-Detecting codes**

Whenever a message is transmitted, it may get scrambled by noise or data may get corrupted. To avoid this, we use error-detecting codes which are additional data added to a given digital message to help us detect if an error occurred during transmission of the message. A simple example of error-detecting code is parity check [5].

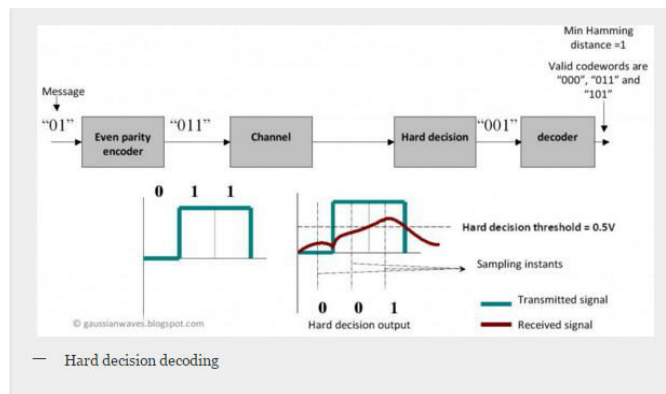


Figure 1: Block Diagram of Error Detecting Codes

**Error-Correcting codes:-**

Along with error-detecting code, we can also pass some data to figure out the original message from the corrupt message that we received. This type of code is called an error-correcting code. Error-correcting codes also deploy the same strategy as error-detecting codes but additionally, such codes also detect the exact location of the corrupt bit [6]. In error-correcting codes, parity check has a simple way to detect errors along with a sophisticated mechanism to determine the corrupt bit location. Once the corrupt bit is located, its value is reverted (from 0 to 1 or 1 to 0) to get the original message [7].

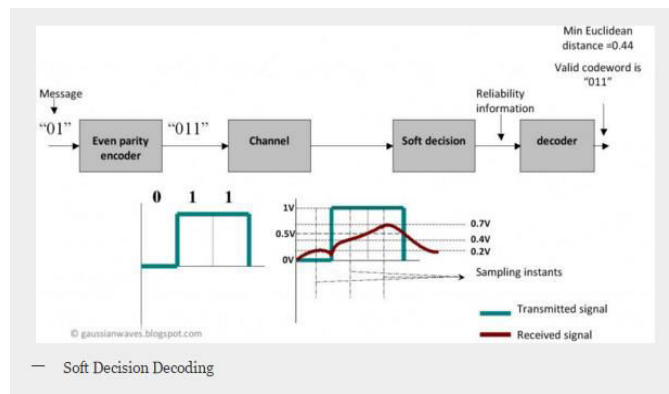


Figure 2: Block Diagram of Error Correction Code

Voltage levels of the received signal at each sampling instant are shown in the figure. The soft decision block calculates the Euclidean distance between the received signal and the all possible codewords [8].



The minimum Euclidean distance is “0.49” corresponding to “0 1 1” codeword (which is what we transmitted). The decoder selects this codeword as the output. Even though the parity encoder cannot correct errors, the soft decision scheme helped in recovering the data in this case. This fact delineates the improvement that will be seen when this soft decision scheme is used in combination with forward error correcting (FEC) schemes like convolution codes, Goley Code etc.

## II. LITERATURE REVIEW

**J. M. Mathana et al. [1]**, the study proposes a modified full adder VLSI architecture design for a Wallace tree encoder. Wallace tree encoder is used to convert thermometer code to binary during the analog to digital conversion process. This is a flash-type flash ADC with a resistor ladder, encoder, and comparator circuit, making it a high-speed application. In order to extract binary code from comparator output, a suitable encoder is required. When designing the low-power flash form ADC, one of the most important considerations is reducing the encoder's energy. There are zeroes in the sequence of the once presence to the series of zeroes in a comparator output, so Wallace tree encoders reduce the error, but they use more power. Consequently, a pass transistor logic (PTL) full adder is used to design a low-power Wallace tree encoder in the proposed work. Only 74.15 nW of power is lost through the proposed design, and the delay is also reduced to 0.0495 ns. The circuit is planned utilizing Rhythm 5.1.0 EDA furnished and reproduced with the utilization of phantom virtuoso.

**Tsounis et al. [2]**, assess the mistake flexibility of a picture information pressure IP center, a FPGA-based gas pedal of the CCSDS 121.0-B-2 calculation used to pack the ESA PROBA-3 ASPIICS Coronagraph Framework Payload picture information. We have improved an issue infusion stage recently proposed for the SEU assessment of FPGA delicate processor centers to connect with the objective picture information pressure IP center and work out the expected for disappointment investigation picture quality measurements. We examine the image compression core's vulnerability to SEU in a SRAM FPGA configuration memory through a comprehensive fault injection campaign. Based on the structural similarity index metric (SSIM), the soft errors are categorized and evaluated according to their effects on the compression core's operation and the quality of the reconstructed images. Using selective protection of the compression core modules, the experimental fault injection results demonstrate that error resiliency inherent in the implementation of the image compression algorithm can be exploited to trade off an acceptable lossless compression performance degradation or a negligible effect on compression fidelity for significant savings in FPGA resource utilization (23 percent LUTs and 17 percent FFs).

**IS Morina et al. [3]**, have compared to files in text format, the size of audio files is somewhat larger. In addition to requiring a significant amount of storage space and taking an excessive amount of time to ship, large files can present a number of challenges. One approach that can be taken to address the issue of large file sizes is file compression. One method that can be used to compress audio files is arithmetic coding. The audio file is encoded using an arithmetic coding algorithm that uses a floating point number to change one row of input symbols. The result of the encoding is a number of values that are greater than or equal to 1 and less than 0. This study compares several wave files to the process of compressing and decompressing audio files. PCM (Pulse Code Modulation) coding is used in the storage of wave files, which are standard audio file formats developed by Microsoft and IBM. The study's wave file compression ratio was 16.12 percent, with an average process time of 45.89 seconds for compression and 0.32 seconds for decompression.

**Jiajia Chen et al. [4]**, With the presentation of high productivity video coding (HEVC) standard which gives super pressure effectiveness, there has been a great deal of exploration chips away at whole number change networks that can give great estimate to the discrete cosine change (DCT) utilized in HEVC. The hardware and power required to implement the derived integer DCT (Int-DCT) must be minimized in order to maintain coding performance. This paper proposes a novel multi-objective optimization algorithm to find an effective Int-DCT matrix with coding performance as close to that of the HEVC transform but implemented with less hardware and power to address these multiple design considerations. According to the findings of the experiments, the proposed algorithm's approximated Int-DCT matrix has a coding performance that is nearly identical to that of the HEVC transforms when measured in terms of Bjntegaard Delta rate. In contrast to other state-of-the-art Int-DCT realizations that can offer similar coding performance, the experiments demonstrate that the proposed 16-point Int-DCT can produce at least 15.5% and 26.8% lower circuit area in FPGA and ASIC, respectively.





S. U. Uvaysov et al. [5], in the paper, the idea of data lossless compression combined with real-time preliminary sorting is looked at. The pressure technique depends on the investigation of the recurrence dissemination of the approaching information stream, the determination of the steady by arranging and, based on this, resulting pressure. The article proposes using sorting and data compression together to reduce processing time and dynamically manage the load on network controllers. During information stream processing, the hardware algorithm for sorting and compressing data on an FPGA is looked at. The solution makes it possible to put an algorithm into an IP core that can be adapted to solve the problem of compressing data, which improves system performance. When developing embedded applications with time-sensitive requirements and limited computing resources, this algorithm can be used. Problems related to the development of telecommunications networks for distributed control systems, data processing subsystems for the Internet of Things, and the Internet of Robotic Things can all be solved using this algorithm.

Linbin Chen et al. [6], A brand-new approximation scheme for the design of a coordinate rotation digital computer (CORDIC) is presented in this paper. An approximation that is inserted into multiple parts of the existing Para-CORDIC architecture and made possible by relaxing the CORDIC algorithm itself is the foundation of this plan. It is suggested to use a fully parallel approximate CORDIC (FPAX-CORDIC) scheme. The generation of the rotation direction is made entirely parallel by this plan, which avoids the memory register of Para-CORDIC. Using HSPICE as the simulation tool, a comprehensive analysis and evaluation of the approximation's error, as well as various circuit-related metrics, are pursued. This error analysis also combines CORDIC-specific parameters with existing figures of merit for approximate computing, such as the Mean Error Distance (MED) and MED Power Product (MPP). It is demonstrated that the expected and simulated error values are in good agreement. The proposed approximate FPAX-CORDIC architecture is used to investigate the Discrete Cosine Transformation (DCT) and the Inverse DCT (IDCT) transformations as a case study of approximate computing applied to image processing. The outcomes confirm the proposed scheme's viability.

Mamatha et al. [7], the spectral analysis, filtering, image enhancement, OFDM, and other aspects of signal processing all make extensive use of the Discrete Fourier Transform. One method for calculating DFT is the cyclic convolution based approach. Four pairs of  $[(M-1)/2]$ -point cyclic convolution can be used to compute an N-point DFT, where M is an odd number and  $N=4M$ . This work proposes an architecture for convolution-based DFT and its FPGA implementation. A pre-processing component, a systolic array, and a post-processing stage make up the proposed architecture. A tag bit is used by the processing element of a systolic array to choose whether to add or subtract from the input signals. ModelSim 6.5 is used to simulate the proposed architecture for 28-point DFT, and Xilinx ISE10.1 is used to synthesize it. The target device is a Vertex 5 xc5vfx100t-3ff1738 FPGA that can operate at a maximum frequency of 224.9 MHz. Hardware utilization and computation time are used in the performance analysis, which is then compared to other architectures that are similar to this one. Further, as the convolution based DCT has two systolic clusters like that of DFT, a brought together engineering is proposed for 1D DFT/1D DCT.

L. Chen et al. [8], Several designs of approximate restoration dividers are presented in this paper; Both the cell and array levels of approximation are utilized. For the fundamental division step of integer subtraction, three approximate subtractor cells are used; Other metrics, like circuit complexity and power loss, tend to reduce subtraction accuracy for these cells. In the approximate divider designs, exact cells are either replaced or truncated at the array level. Error analysis and HSPICE simulation are used to conduct a comprehensive analysis of approximation at the cell and array (divider) levels; The evaluation of various circuit metrics includes power dissipation and complexity. The proposed approximate arithmetic circuits are used to investigate various applications. The simulation results indicate that the proposed designs offer better error-tolerant capabilities for quotient-oriented applications (such as image processing) than for remainder-oriented applications (such as modulo operations), with significant reductions in power dissipation and circuit complexity. The approximate non-restoring scheme in the technical literature is significantly inferior to the proposed approximate restoring divider.

### III. BINARY CODES

Block codes are referred to as  $(n, k)$  codes. A block of  $k$  information bits are coded to become a block of  $n$  bits.  $n=k + r$ , where  $r$  is the number of parity bits and  $k$  is the number of information bits.

The more commonly employed Block codes are:



1. Single Parity-Check Bit Code
2. Repeated Codes
3. Hadamard Code
4. Hamming Code
5. Convolution Code Codes
6. Cyclic Codes
7. Golay Code
8. Extended Golay Codes

Marcel Golay was born in Neuchatel, Switzerland in 1902. He was a successful mathematician and information theorist who was better known for his contribution to real world applications of mathematics than any theoretical work he may have done [9, 10]. Golay’s sought the perfect code. Perfect codes are considered the best codes and are of much interest to mathematicians. They play an important role in coding theory for theoretical and practical reasons. The following is a definition of a perfect code:

A code C consisting of N codewords of length N containing letters from an alphabet of length q, where the minimum distance  $d=2e+1$  is said to be perfect if:

$$\sum_{i=0}^e \binom{n}{i} (q-1)^i = \frac{q^n}{N} \quad (1)$$

There are two closely related binary Golay codes. The extended binary Golay code G24 encodes 12 bits of data in a 24-bit word in such a way that any 3-bit errors can be corrected or any 7-bit errors can be detected. The other, the perfect binary Golay code G23 has codewords of length 23 and is obtained from the extended binary Golay code by deleting one co-ordinate position. In standard code notation the codes have parameters [24, 12, 8] and [23, 12, 7] corresponding to the length of the codewords, the dimension of the code and the minimum Hamming distance between two codewords respectively. In mathematical terms, the extended binary Golay code, G24 consists of a 12-dimensional subspace W of the space  $V=F_2^{24}$  of 24-bit words such that any two distinct elements of W differ in at least eight coordinates. By linearity, the distance statement is equivalent to any non-zero element of W having at least eight non-zero coordinates. The possible sets of non-zero coordinates as w ranges over W are called code words. In the extended binary Golay code, all code words have the Hamming weights of 0, 8, 12, 16, or 24. Up to relabeling coordinates, W is unique. The perfect binary Golay code, G23 is a perfect code. That is the spheres of radius three around code words form a partition of the vector space.

**Codeword Structure:** A codeword is formed by taking 12 information bits and appending 11 check bits which are derived from a modulo-2 division, as with the CRC. Golay [23, 12] Codeword. The common notation for this structure is Golay [23, 12], indicating that the code has 23 total bits, 12 information bits, and 23- 12=11 check bits. Since each codeword is 23 bits long, there are 2<sup>23</sup>, or 8,388,608 possible binary values. However, since each of the 12-bit information fields has only one corresponding set of 11 check bits, there are only 2<sup>12</sup>, or 4096, valid Golay code words.

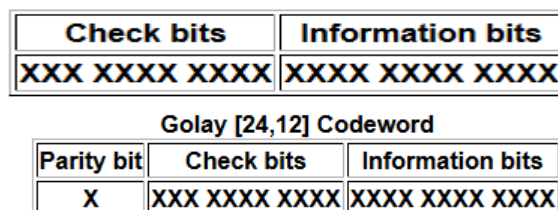


Figure 3: Block Diagram of Golay Code

The binary Golay code leads us to the extended Golay code. Codes can be easily extended by adding an overall parity check to the end of each code word.



This extended Golay Code can be generated by the  $12 \times 24$  matrix  $G = [I_{12} | A]$ , where  $I_{12}$  is the  $12 \times 12$  identity matrix and  $A$  is the  $12 \times 12$  matrix

$$A = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (2)$$

The binary linear code with generator matrix  $G$  is called the extended binary Golay code and will be denoted by  $G_{24}$ . The extended Golay code has a minimum distance of 8. Unlike the  $(23, 12)$  code, the extended Golay code is not perfect, but simply quasi perfect.

Properties of the extended binary Golay code

- The length of  $G_{24}$  is 24 and its dimension is 12.
- A parity-check matrix for  $G_{24}$  is the  $12 \times 24$  matrix  $H = [A | I_{12}]$ .
- The code  $G_{24}$  is self-dual, i.e.,  $G \perp 24 = G_{24}$ .
- Another parity-check matrix for  $G_{24}$  is the  $12 \times 24$  matrix  $H_0 = [I_{12} | A] (= G)$ .
- Another generator matrix for  $G_{24}$  is the  $12 \times 24$  matrix  $G_0 = [A | I_{12}] (= H)$ .
- The weight of every codeword in  $G_{24}$  is a multiple of 4.
- The code  $G_{24}$  has no codeword of weight 4, so the minimum distance of  $G_{24}$  is  $d = 8$ .
- The code  $G_{24}$  is an exactly three-error-correcting code.

### Wallace Tree

The Wallace tree encoder also called as ones counter is built with full adder cells. It counts the number of ones present at the output of comparator and represents them as binary code. Fig. 3 shows a 3 bit Wallace tree encoder with full adder as its basic cell. The full adders count the number of logic “1” at their input to give final binary output. The full adders are arranged to sum the inputs so as to form Wallace tree.

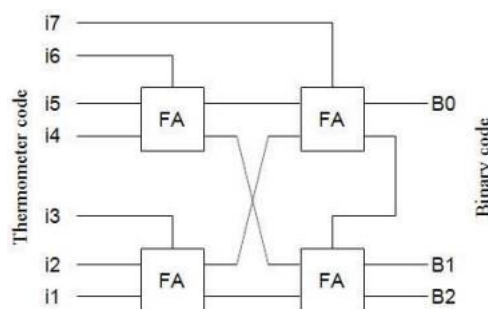


Figure 4: 3-bit Wallace tree encoder



Even when bubble errors are present, this encoder converts output of comparator into correct binary output. Another advantage of this encoder is flexibility such that suitable topology can be selected according to speed and power requirements [5]-[7]. The number of full adder cells needed to implement an N bit encoder is given by the equation,

$$X_N = \sum_{i=1}^N (i - 1) \cdot 2^{(N - i)} \quad (3)$$

#### IV. CONCLUSION

It can be concluded from the above encoder shows drastic improvement, thus making it suitable to use in low power and high speed applications with a sampling rate of 1GHz. The PDP is calculated to be 0.28 fJ and the EDP is calculated to be  $0.83 \times 10^{-26}$  Js. The Wallace tree encoder is advantageous in terms of correcting a bubble error without the requirement of additional circuitry. On the other hand, the new encoders like Fat-tree and MUX based encoder still holds better performance for low power consumption and high sampling rates. The drawback of modern encoders is the additional circuit required for bubble error correction. Thus, Wallace tree encoder excels the chart in terms of bubble error correction.

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