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Survey on Digital Filters using Different Multiplier and Adder

Sudha Kumari¹, Dr. Anuj Garg²

M. Tech. Scholar, Department of Electronics and Communication, LNCT, Bhopal, India¹

Associate Professor, Department of Electronics and Communication, LNCT, Bhopal, India²

ABSTRACT- Several VLSI architectures have been suggested for the parallel FIR Filter in last decade to meet space and time requirement of real-time application. All these designs differ by arithmetic complexity, cycle period, throughput rate and they use almost same amount of on-chip memory words and equal amount of frame buffer words. The mainly digital signal processing system depends on the multiplier. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have studied 2x2 parallel FIR filter with different multiplier and adder. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. All the design is implemented Xilinx software with different device family.

KEYWORDS: - Kogge Stone Adder, Vedic Multiplier, 2x2 Parallel FIR Filter

I. INTRODUCTION

A finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is limited because it settles to zero in finite time. This contrasts with infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely [1]. The communication system model describes a communication exchange between transmitter and receiver. Signals or information passes from source to destination through a channel [2]. Mainly FIR filters are using windowing based methods and optimization-based methods [3]. To design a Finite Impulse Response (FIR) filter with the desired frequency response, window functions to achieve a trade-off between ripples in the passband and the transition band's sharpness [4]. Digital filters form an important part of today's expanding field of Digital Signal Processing (DSP). Among them, the most used filter is Finite impulse response. FIR filters. FIR filters are used extensively to filter images, modulate frequency, precision arithmetic, and various other purposes. Thus, various optimization methods are employed for the designing of optimal digital FIR filters [5]. Various optimization techniques provide better results for different filter coefficients for control parameter, dependence, premature convergence, etc. They have many advantages, like simple design implementation, minimized error function, superior search capability, and fast convergence. This paper has reviewed the basic of the frequency sampling method for designing Finite Impulse Response (FIR) filters in a communication system. Moreover, FIR architecture, prototype for optimization techniques, hardware-based 2D FIR filter models are highlighted.

Due to the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. Finite-impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing [6]. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable. For example, a 27-tap digital filter is used in a video ghost canceller for broadcast television, which reduces the effect of multipath signal echoes [7]. On the other hand, parallel and pipelining processing are two techniques used in DSP applications, which can both be exploited to reduce the power consumption. Pipelining shortens the critical path by interleaving pipelining latches along the data path, at the price of increasing the number of latches and the system latency, whereas parallel processing increase the sampling rate by replicating hardware so that multiple inputs can be processed in parallel and multiple outputs are generated at the same time, at the expense of increased area [8]. Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed.



II. LITERATURE REVIEW

S Narendran et al. [1], a definitive objective of the examination work is to dissect the exhibition of FIR channel planned in view of FFA calculation. The proposed structure focuses on region improved adders which are intended for symmetric coefficient that diminishes equipment cost in the plan with an oblige that the channel tap is of even request. Region investigation of silicon chip is performed utilizing various adders like Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA) and Conditional Sum Adder (COS). Execution examination report for a 3 equal 96-tap channel is viewed as founded on the above viper, where the RCA requires less region use contrasted with other three adders. The symmetric convolution-based RCA Fast FIR Algorithm (FFA) structure requires just 896 cuts while COS requires 1024 cuts and CLA requires 960 cuts. For higher-request, FIR channel design of 1024 or higher taps, the reserve funds in the space usage for RCA based FFA is roughly 10% and 15% contrasted with CLA and COS based FFA separately in light of the fact that COS requires more equipment building blocks. The RCA based FFA expands the idleness by around 9% and 7% contrasted with CLA and COS based FFA separately, and there will be a compromise.

K. Anjali Rao et al. [2], in this paper, we propose 3-equal limited motivation reaction (FIR) structures with the use of polyphase coefficient evenness and quick FIR calculations (FFAs). For symmetric convolution of odd length channel The proposed structures are advantageous as far as the quantity of multipliers which can lessen the execution intricacy of the equal FIR channels. At first, 3-equal customary FIR structures are reconfigured so that the polyphase coefficient evenness of odd length FIR channels can be applied for the decrease of the half number of multipliers, from there on, FFAs are utilized for bringing down the equal subfilter parts of a polyphase channel. On contrasting the presentation and existing comparative designs the proposed FFA based structure is tracked down unrivaled concerning diminished number of required multipliers.

Yi Zheng et al. [3], to make students ace an equipment execution of computerized channels, we take the plan of an equal FIR advanced low-pass channel as a showing case, which can introduce the execution strategy for computerized channels joining Matlab and an equipment portrayal language together. In the first place, as per the undertaking of the showing case, the coefficients of FIR advanced not entirely settled by a FDATool utilization of Matlab. By standardization and quantization, the channel coefficients and examined information are both changed over from the drifting point information to the fixed-point information. The digit width of substantial information pieces of FIR channel still up in the air as per the standard of increase gather activity of FPGAs. Then, at that point, we use Verilog HDL to execute a quick multiplier and the equal FIR computerized low-pass channel. At long last, we contrast the channel results of FPGAs and the ones of Matlab, and investigate the explanation. The case showing technique, which consolidates Matlab and FPGAs, is useful to foster the equipment execution capacity of computerized signal handling of students.

S. Sreekanth et al. [4], in this paper, Polyphase Finite Impulse Response (FIR) computerized channel is planned and carried out by utilizing 40 nm LP CMOS TSMC Library. For some advanced channelized collectors and transmitters in computerized correspondence frameworks the speed of FIR channel and idleness are significant elements. Polyphase channel is executed with equal methodology in which equal multipliers, adders and FFT block utilizing the Radix-2² calculation are utilized. Radix-2² purposes not many multipliers contrasted with Radix-2 calculation. In this work elite execution is accomplished contrasted with ordinary direct structure plan and different plans.

Qiaoyu Tian et al. [5], the Cook-Toom calculation is generally utilized in short-length direct convolution, which is the structure square of enormous focuses convolution calculations. This paper proposes further developed equal limited motivation reaction (FIR) channel structures for direct stage FIR channel, which depends on the Cook-Toom calculation. In the proposed structures, Cook-Toom calculation is utilized to diminish the quantity of sub-channels, and the symmetric properties of the straight stage FIR channel's coefficients is utilized to additionally lessen the quantity of multipliers in sub-channels. Contrasted and the announced FFA and ISCA equal FIR channel structures, the proposed technique can significantly decrease the computational intricacy. In particular, for a 8-equal 144-tap channel, the proposed plan saves 18 multipliers (5%), 45 adders (7.9%) contrasted and the construction in light of Winograd convolution calculation.

Payal Paliwal et al. [6], equal FIR channel is the need of many low power and rapid DSP applications. In this paper, quick FIR calculation based equal symmetric FIR channel utilizing Han-Carlson snake based vedic multiplier is proposed. FFA calculation lessens the multiplier consider contrasted with the conventional equal plan. To work on the



presentation of the proposed channel, as of late evolved Han-Carlson viper based Vedic multiplier is utilized. In the proposed plan the viper unit is additionally carried out utilizing Han-Carlson snake. In the proposed plan two and three equal FIR channels of request 24 and 72 are executed utilizing VHDL. The execution results show that the proposed engineering gives low basic way deferral and power dispersal when contrasted with the regular one. With the upside of low postponement and power, proposed design is valuable in present day signal handling and correspondence applications.

Swetha Annangi et al. [7], in this paper, a 144-tap 16-equal Fast Finite Impulse Response (FIR) Algorithm (FFA) channel structure is planned utilizing verilog HDL. The planned channel structure is mimicked utilizing XILINX ISE 14.7. The planned module is combined utilizing CADENCE RTL Compiler and the application explicit incorporated circuit (ASIC) plan of the proposed channel structure is executed utilizing CADENCE apparatus set on CADENCE GPDK45nm innovation. By applying Fast FIR Algorithm, 65% of multipliers are diminished and the quantity of adders are expanded. The adders possess less silicon region than multipliers. Subsequently, the decrease in region is accomplished by supplanting the multipliers with adders. Further, the proposed 16 equal FFA channel structure lessens the postpone when contrasted with 16 equal FIR channel structure without applying Fast FIR Algorithm. The proposed channel engineering involves an area of 79220 sq. μm and consumes a force of 20mW at 333MHz when integrated.

Shalina Percy et al. [8], have the requirement for productive Finite Impulse Response (FIR) channels in fast applications targets Field Programmable Gate Arrays (FPGAs) as a powerful and adaptable stage for computerized execution. In spite of the fact that FIR channel offer benefits like direct stage trademark, no criticism circles and great framework strength, its convolution nature balances a test in parallelization because of information reliance and computational intricacy. To determine this, we propose a clever FPGA-based reconfigurable channel engineering, which processes a few information tests in equal and separates information interdependency in a twisting design. This conventional pipelined-equal channel is parameterizable as far as channel request and level of parallelization. Exploratory outcomes show a throughput of 7.2 GSPS with a working recurrence of just 450 MHz for a channel length of 11 with 16 equal sources of info. With parallelization of 4, it is 4.64 times quicker than the best in class answer for a channel length of 16 and a promising 41% expansion in throughput is accomplished for a higher request of 61.

III. 2x2 PARALLEL FIR FILTER

In general, two parallel FIR filter can be expressed as traditional two parallel digital filters is shown in figure 1. For this two parallel FIR filter $L=2$. This will require three FIR sub-filter blocks of length $N/2$, one pre-processing adder and three post-processing adders. Total number of multiplier and adders required are $3N/2$ and $3(N/2-1) + 4$ respectively.

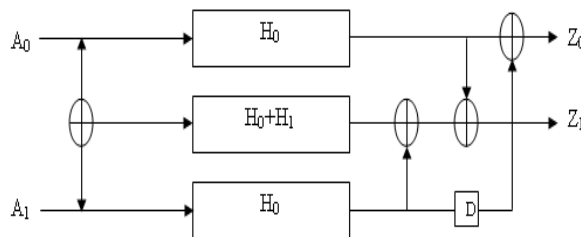


Figure 1: Parallel 2x2 FIR Filter

Following are the equations used to design the two parallel FIR filter with two inputs A_0 , A_1 and two outputs Z_0 , Z_1 . For implementing this filter three FIR sub-filter blocks has been used as compare to traditional two FIRs sub-block filter, having length $N/3$. Two of three sub-filters H_0+H_1 and H_0-H_1 are having symmetric coefficient which reduces the number of multiplier and adders. Here two preprocessing and four post-processing adders have been used along with delay equipment. The symmetric sub-filter block has been implemented at the cost of two additional adders among those one is pre-processing and other one is post-processing for $L=2$. Following are the equations used to design the filter:

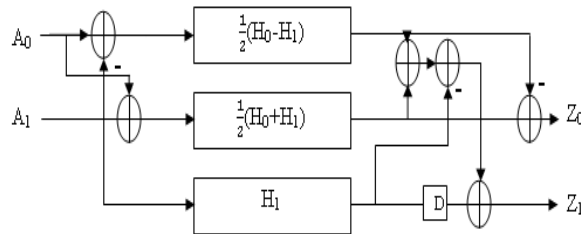


Figure 2: Proposed Parallel 2x2 FIR Filter

This same process is used for the n number of bits and thus we get the final sum and carry as output.

Example 1: Consider a 33-tap FIR filter with a set of symmetric coefficient as follows:

{h(0), h(1), h(2), h(3), h(4),.....h(29), h(30), h(31)}

Where

- h(0) = h(32),
- h(1) = h(31),
- h(2) = h(29),
- h(3) = h(28)

.....

h(12) = h(20)

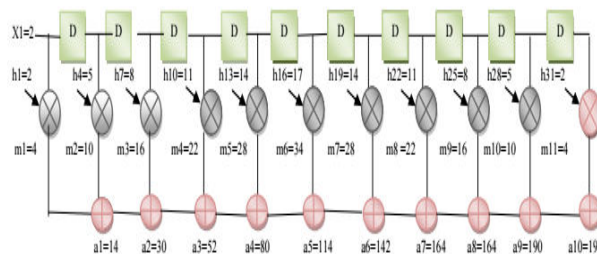


Figure 3: Internal Structure of H1

The symmetric parallel FIR filter is shown in Figure 3. The three parallel FIR filter consists of filter blocks. The input to the system is represented as A0, A1 and the response of the system as Z0 and Z1. Let X0=5, X1= 2, X2=3. The filter blocks H1 with its mod 3 coefficients are shown in Figure 3.

IV. ADDER AND MULTIPLIER

Parallel Adder:-

Parallel adder can add all bits in parallel manner i.e. simultaneously hence increased the addition speed. In this adder multiple full adders are used to add the two corresponding bits of two binary numbers and carry bit of the previous adder. It produces sum bits and carry bit for the next stage adder. In this adder multiple carry produced by multiple adders are rippled, i.e. carry bit produced from an adder works as one of the input for the adder in its succeeding stage. Hence sometimes it is also known as Ripple Carry Adder (RCA). Generalized diagram of parallel adder is shown in figure 4.

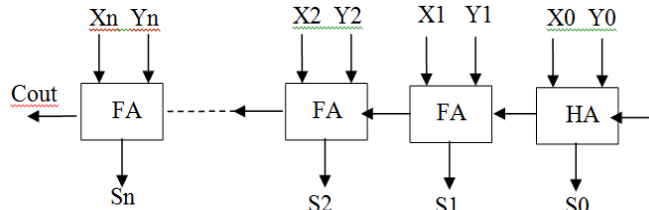


Figure 4: Parallel Adder (n=7 for SPFP and n=10 for DPFP)

Carry Skip Adder:-

This adder gives the advantage of less delay over Ripple carry adder. It uses the logic of carry skip, i.e. any desired carry can skip any number of adder stages. Here carry skip logic circuitry uses two gates namely “and gate” and “or gate”. Due to this fact that carry need not to ripple through each stage. It gives improved delay parameter. It is also known as Carry bypass adder. Generalized figure of Carry Skip Adder is shown in figure 5.

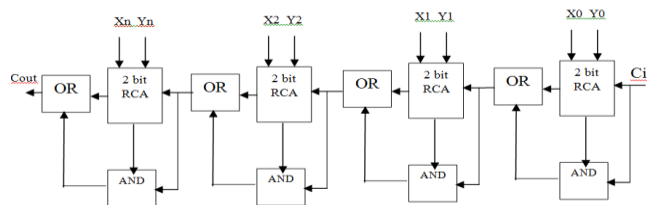


Figure 5: Carry Skip Adder

Carry Select Adder:-

Carry select adder uses multiplexer along with RCAs in which the carry is used as a select input to choose the correct output sum bits as well as carry bit. Due to this, it is called Carry select adder. In this adder two RCAs are used to calculate the sum bits simultaneously for the same bits assuming two different carry inputs i.e. ‘1’ and ‘0’. It is the responsibility of multiplexer to choose correct output bits out of the two, once the correct carry input is known to it. Multiplexer delay is included in this adder. Generalized figure of Carry select adder is shown in figure 6. Adders are the basic building blocks of most of the ALUs (Arithmetic logic units) used in Digital signal processing and various other applications. Many types of adders are available in today’s scenario and many more are developing day by day. Half adder and Full adder are the two basic types of adders. Almost all other adders are made with the different arrangements of these two basic adders only. Half adder is used to add two bits and produce sum and carry bits whereas full adder can add three bits simultaneously and produces sum and carry bits.

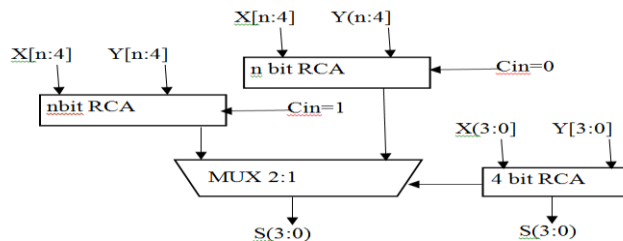


Figure 6: Carry Select Adder

Multiplier:-

All the parallel, the pipeline and the high performance multipliers implemented in hardware is illustrated in the block diagram of Figure 7. It consists of three phases as follows.

- Partial Product Generator (PPG)
- Partial Product Reduction Tree (PPRT)
- Carry Propagate adder (CPA)



The PPG creates fractional items either utilizing two info OR door or by utilizing MBE strategy. The PPRT is utilized to pack the few varieties of halfway item pushes into a variety of two lines. The CSA and different kinds of blowers can be utilized as the PPRT. At last the CPA is utilized for the expansion of a variety of two lines to get the result of augmentation. The fastest CPA is the CLA).

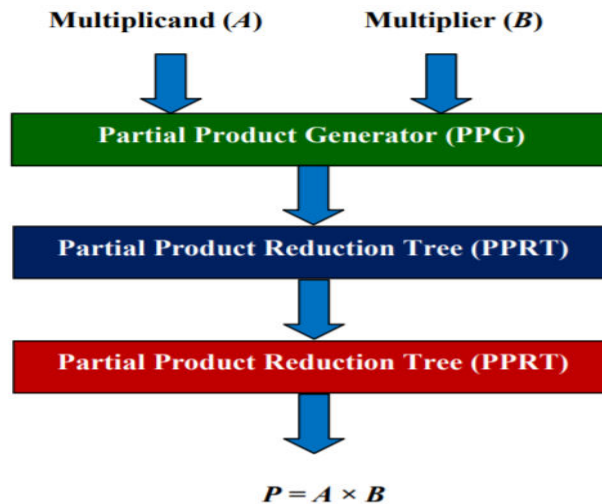


Figure 7: Block diagram of Multiplier

The non-pipeline multiplier can be changed over into the pipeline multiplier by embedding register between the phases of combinational rationale circuits.

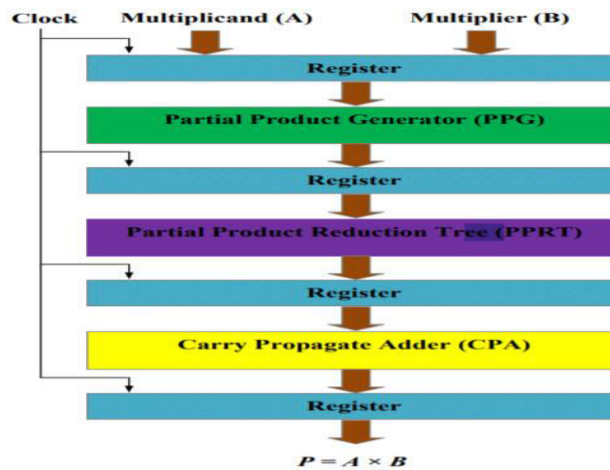


Figure 8: Block diagram of Pipeline Multiplier

Figure 8 shows the square outline of the pipeline multiplier. All the pipeline stages are worked with the synchronous clock signal. Each clock cycle, two new operands (An) and (B) is gotten by the pipeline and handled in the progressive phases of the pipeline. When the pipelines arrange is topped off, at that point each clock cycle another result of duplication activity is produced.

V. CONCLUSION

The proposed 16x16 Vedic multiplier architecture has been designed and synthesized using on Spartan 3 XC3S400 board and is used in parallel FIR filter design. The proposed Vedic Multiplier with carry select adder is compared with the existing Vedic multiplier using Carry select adder along with Common Boolean Logic and can be inferred that proposed architecture is faster compared to existing Vedic multiplier. In future the proposed multiplier performance



parameters can be improved by high level pipelining operations and applied in signal processing applications like image processing and video processing.

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