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VLSI Architecture for Discrete Hartley Transform using Pipeline Structure Based on Brent Kung Adder

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ABSTRACT: A discrete Hartley transform (DHT) algorithm can be efficiently implemented on a highly modular and pipeline architecture having a regular structure consisting of multiplier and adder. Discrete Hartley Transform (DHT) is one of the transforms used for converting data in time domain into frequency domain using only real values. We have proposed a new algorithm for calculating DHT of length 2^N , where $N=3$ and 4 . We have implemented pipeline structure based on Brent Kung adder as an improvement in place of simple adder used in conventional DHT. This paper gives a comparison between conventional DHT algorithm and proposed DHT algorithm in terms of delays and area.

KEYWORDS: Discrete Hartley Transform (DHT), Brent Kung Adder, Pipeline Structure, Xilinx Vertex family.

I. INTRODUCTION

Digital Signal Processing (DSP) is a term that refers to data processing in numerous domains depending on its applications. DSP is used in various sectors, including space, medical, economic, industrial, and scientific [1]. Each one necessitates the analysis of large amounts of data to gather relevant information. Transform is indeed a DSP approach for transforming one data type into another. In DSP, there is a transformed family for data processing. One of several oldest techniques within that family includes Fourier analysis [2]. The Fourier transform is indeed an integral-based mathematical technique. On the other hand, the Fourier transform is ineffective for non-stationary waveforms. Because neither the Fourier series nor the Fourier transform applies to discrete signals, a unique discrete spectrum transform is required. Regarding signals that range from positive to negative infinity and are not periodic, the discrete-time Fourier transform (DTFT) is utilized [3]. Because DTFT isn't suitable for periodic discrete signals, the discrete Fourier transform (DFT) was created. DFT is still a discrete numerical version of FT that uses accumulation rather than integrals. Signals which repeat consecutively in a periodic pattern ranging from positive to negative infinity are treated with DFT. FFT is a DFT upgrade in which the calculation is faster [4]. For a long time, discrete transformations with low multiplicative complexity have attracted the curiosity of researchers [5]. DHT is an acronym for Discrete Hartley Transform, which R. V. L. Hartley introduced in 1942. Discrete Hartley Transform is invented to reduce this hardware complexity. It seems to be a Radix-2 method that is particularly effective in Signal processing applications, including image compression, signal shrinkage, filter banks, signalling representation, including harmonic analysis, among others [6]. The usage of DHT is primarily intended to simplify the intricacy of the VLSI hardware platform. Although DHT computing has also advanced in hardware complexity, it is becoming less. It is because the forward and inverse of DHT are identical except for the scaling factor, or even that DHT is indeed the inverse of itself. Both forward and inverse measurements will be performed on the same hardware. In other words, researchers can presume that both forward and inverse implementations have the same number of adders, multipliers, and other components. The Discrete Fourier Transform (DFT) is comparable to DHT, or DHT is developed from DFT. This DFT contains both real and imaginary components, whereas the DHT only contains real components. Because the computation of imaginary portions is trivial, difficult arithmetic is eliminated. Whenever the input sequence is real, discrete Hartley transform (DHT) would be applied to substitute the DFT [7] efficiently. There are already various low-arithmetic-cost split-radix techniques for computing DHT.



II. DISCRETE HARTLEY TRANSFORM

Discrete Hartley Transform is abbreviated for DHT and this transform was proposed by R. V. L. Hartley in 1942. DHT is the analogous to Fast Fourier transform which provides the only real value at any cost. The main difference from the DFT is that it transforms the real inputs to real outputs with no intrinsic involvement of complex value. DFT can be used to compute the DHT, and vice versa.



Figure 1: Block Diagram of DHT

In other words, Discrete Hartley transform is used to convert real values into real ones. It requires decomposition of data into stages using butterfly similar to FFT. But the butterfly used in DHT is quite different in terms of coefficients or multipliers. With the increase in number of DHT sequence length the number of coefficients is also increased simultaneously.

Let $N \geq 4$ be a power of two. For any real input sequence $\{x(i) : i = 0, 1, 2, \dots, N - 1\}$

$$X(k) = DHT(N)\{x(i)\}$$

$$= \sum_{i=0}^{N-1} x(i) \cdot cas[2ki\pi / N] \quad \text{for } k = 0, 1, \dots, N - 1$$

Where $cas(x) = \cos(x) + \sin(x)$

• Algorithm for 16-Point DHT-

We present an implementation of fast DHT algorithm for a length $N=16$. There are six stages required to complete the butterfly design of $N=16$ length DHT. These stages include summing stages and coefficient multiplying stages. Before first stage the data sequence are arranged in bit reversed pattern by using any method like permutation. Then in the first stage the pairs of bit reversed patterns are added to form eight terms. In the second stage, one third of the terms are again added and subtracted to form further three terms.

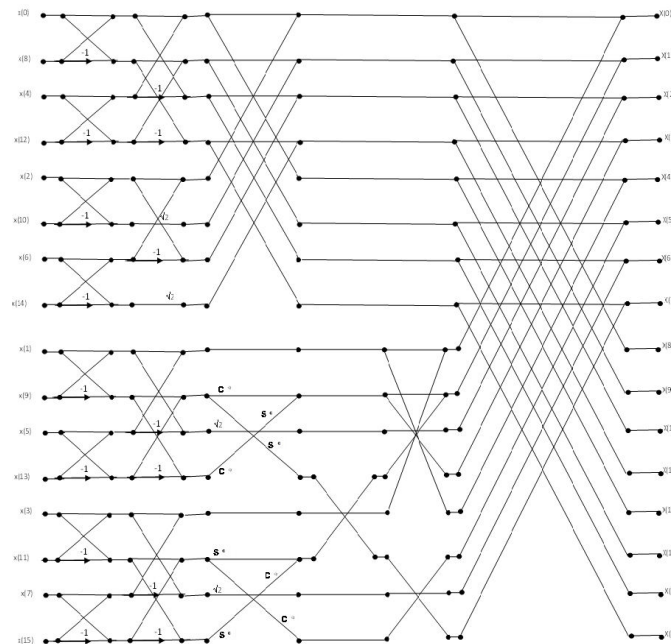


Figure 2: 16-point DHT Butterfly



- Mathematical calculation for N=16

First two stages do not include any multiplication. Remaining terms are multiplied by the first coefficient. In the next stage again two new coefficients are introduced which is multiplied by the lower half of the third stage. In each stage multiplying of coefficients stage precedes its summing stage. After coefficient multiplication it is preceded by its summing stage to form the common terms used in the final stage. Last stage includes only summing of terms. Finally we get the transformed data sequence in order and do not need any permutation.

$$X(0) = (x(0) + x(8)) + (x(4) + x(12)) + (x(2) + x(10)) + (x(6) + x(14)) + (x(1) + x(9)) \\ + (x(5) + x(13)) + (x(3) + x(11)) + (x(7) + x(15))$$

$$X(1) = (x(0) + x(8)) + (x(4) - x(12)) + c_1(x(2) - x(10)) + (x(5) + x(13)) + \\ c_3\{(x(3) - x(11)) + (x(7) - x(15))\} + c_2\{(x(3) - x(11)) - (x(7) - x(15))\}$$

$$X(2) = (x(0) + x(8)) - \{(x(4) + x(12)) + (x(6) + x(14))\} + c_1\{(x(1) + x(9)) - (x(5) + x(13))\} \\ + (x(2) + x(10))(x(3) + x(11)) + (x(7) + x(15))$$

$$X(3) = (x(0) - x(8)) - (x(4) - x(12)) + c_1(x(6) - x(14)) + (x(5) + x(13)) + \\ c_3\{(x(3) + x(11)) + (x(7) - x(15))\} + c_2\{(x(3) - x(11)) - (x(7) - x(15))\}$$

$$X(4) = (x(0) + x(8)) + (x(4) + x(12)) + (x(2) + x(10)) + (x(6) + x(14)) + (x(1) + x(9)) \\ + (x(5) + x(13)) - \{(x(3) + x(11)) + (x(7) + x(15))\}$$

$$X(5) = (x(0) + x(8)) + (x(4) - x(12)) + c_1(x(2) - x(10)) + (x(5) + x(13)) + \\ c_3\{(x(3) - x(11)) + (x(7) - x(15))\} - c_2\{(x(5) - x(13)) - (x(1) - x(9))\}$$

$$X(6) = (x(0) + x(8)) + (x(6) + x(14)) - \{(x(2) + x(10)) \\ + (x(4) + x(12))\} + c_1\{(x(3) - x(11)) + (x(7) - x(15))\}$$

$$X(7) = (x(0) + x(8)) - (x(4) - x(12)) + c_1(x(6) - x(14)) - c_3\{(x(5) + x(13)) - (x(1) - x(9))\} \\ + c_2\{(x(5) - x(13)) + (x(1) - x(9))\}$$

$$X(8) = (x(0) + x(8)) + (x(4) + x(12)) + (x(2) + x(10)) + (x(6) + x(14)) - \\ (x(1) + x(9)) - (x(5) + x(13)) - (x(3) + x(11)) - (x(7) + x(15))$$

$$X(9) = (x(0) - x(8)) + (x(4) - x(12)) + c_1(x(2) - x(10)) + (x(5) + x(13)) - \\ c_3\{(x(3) - x(11)) + (x(7) - x(15))\} + c_2\{(x(3) - x(11)) - (x(7) - x(15))\}$$

$$X(10) = (x(0) + x(8)) - \{(x(4) + x(12)) + (x(6) + x(14))\} \\ - c_1\{(x(1) + x(9)) - (x(5) + x(13))\}$$

$$X(11) = (x(0) - x(8)) - (x(4) - x(12)) + c_1(x(6) - x(14)) + c_3\{(x(3) - x(11)) \\ + (x(7) - x(15))\} + c_2\{(x(3) - x(11)) - (x(7) - x(15))\}$$

$$X(12) = (x(0) + x(8)) + (x(4) + x(12)) + (x(2) + x(10)) + (x(6) + x(14)) - \\ \{(x(1) + x(9)) + (x(5) + x(13))\} + (x(3) + x(11)) + (x(7) + x(15))$$

$$X(13) = (x(0) - x(8)) + (x(4) - x(12)) - c_1(x(2) - x(10)) - c_3\{(x(3) - x(11)) + (x(7) - x(15))\} \\ + c_2\{(x(1) - x(9)) - (x(5) - x(13))\}$$

$$X(14) = (x(0) + x(8)) - (x(4) + x(12)) - (x(2) + x(10)) + c_1(x(3) + x(11)) - (x(7) + x(15))$$

$$X(15) = (x(0) - x(8)) - (x(4) - x(12)) - c_1(x(6) - x(14)) - c_3\{(x(13) - x(5)) - (x(1) - x(9))\} \\ + c_2\{(x(1) - x(9)) - (x(5) - x(13))\}$$



III. PROPOSED TECHNOLOGY

Here, the DHT of length N=16 point requires 67 additions and 12 multiplications. We have used a different technique called Urdhwa tiryakbhyam of ancient Vedic times for multiplication. This multiplication technique reduces the delay and complexity. It converts multiplication into simple logical AND operation using associated circuits of full, half adders and AND gate. Further, the area is reduced by using various compressors for adding the partial products of multiplication.

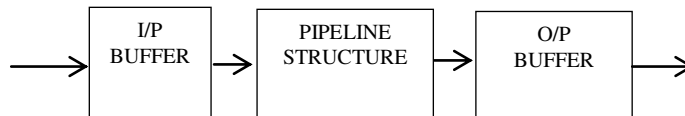


Figure 3: Proposed Architecture

Parallel and Pipeline Structure

The proposed DHT algorithm has been designed in parallel as well as pipelined structure. In parallel structure, 4 such units as shown in Fig. 3 are implemented in parallel such that 4 Hartley's coefficients are obtained simultaneously. The hardware circuit obtained for 1 unit of the parallel structure is given in Fig. 4.

On the other hand, in case of the pipeline structure, there are registers incorporated between multiple stages of the structure. To implement the pipeline structure, only 1 such unit is required which gives all Hartley's coefficients at output in subsequent clock cycles, one by one. The hardware circuit for the same is given in Fig. 4. In above figure, the dotted blocks denote the registers between multiple stages.

However, it must be noted that word format taken for both the structures are different. Since in pipeline structure, values in previous stages are updated in every clock cycle, we need to transmit additional information along with the data. The information related to p, and q are also added to the transmitted data so that we can retain these information in every upcoming stage of the pipeline. Word format for parallel structure is given as: 1 sign bit, 10 integer bits and 20 fraction bits. While, word format for pipeline structure is given as: first few bits (4-6 bits) to transmit additional information, then 1 sign bit, 10 integer bits and 20 fraction bits. Therefore, at every stage, the values of p and q are read first to identify the coefficient and then the required computations are done. These units are replicated four times (for q=0,1,2,3) and then added together to get one Hartley's coefficient at the output.

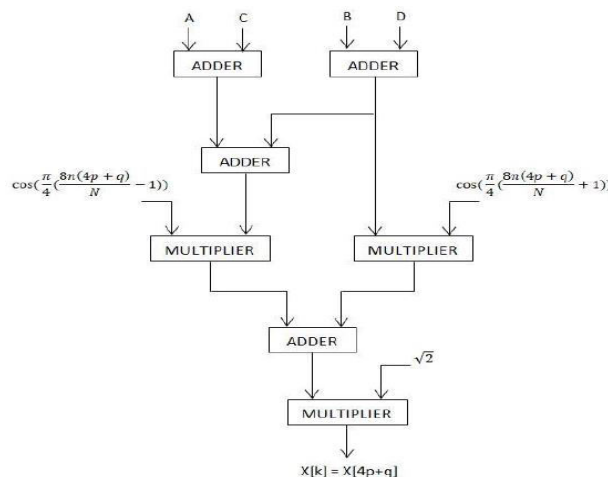


Figure 4: Hardware Circuit for parallel structure

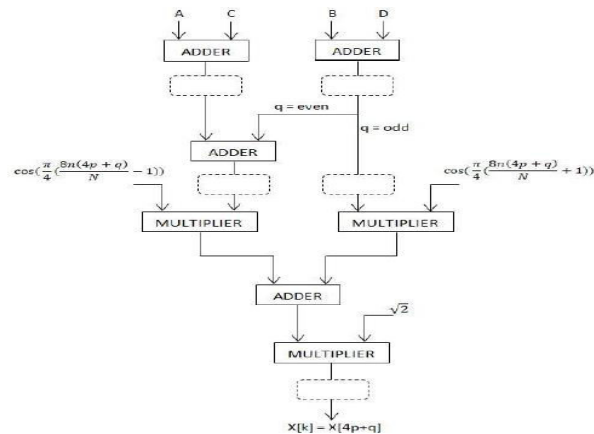


Figure 5: Hardware Circuit for pipeline structure

Brent Kung Adder

The Brent–Kung adder is a parallel prefix adder (PPA) and is modified form of carry-look ahead adder (CLA). Proposed by Richard Peirce Brent and Hsiang Te Kung in 1982 it acquainted higher normality with the structure of the adder and has less wiring issues, reduces complexities, provides better execution and less chip region which is not the case with the Kogge–Stone adder (KSA). It is also very faster than ripple-carry adders (RCA).

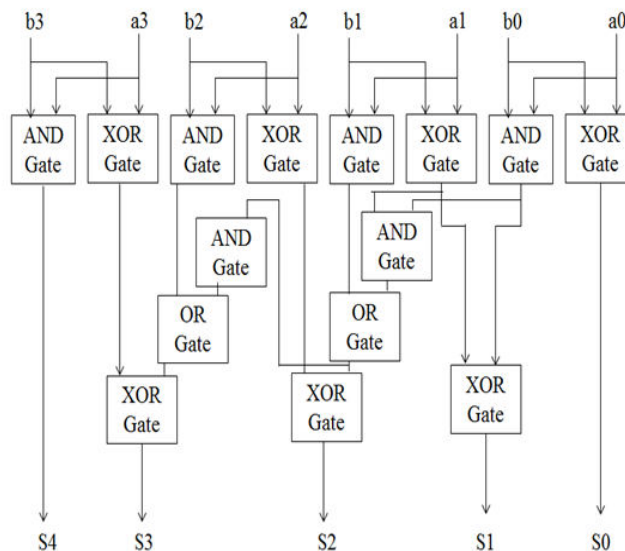


Figure 6: Block Diagram of Brent Kung Adder

IV. SIMULATION RESULT

All three architecture are designed by using Xilinx 14.2i. The simulated results are displayed in table 1 & table 2. In the simulation results proposed DHT gives the best performance.

Table I: Comparisons Result for 8-point Discrete Hartley Transform (DHT) with word length 16.

Parameter	Previous Technique	Modified DHT	Proposed DHT
No. of Slices	601	553	548
No. of 4 input LUTs	1125	1032	1029
No. of bounded IOBs	256	256	256
Maximum combinational path delay(in ns)	29.62	24.97	21.96

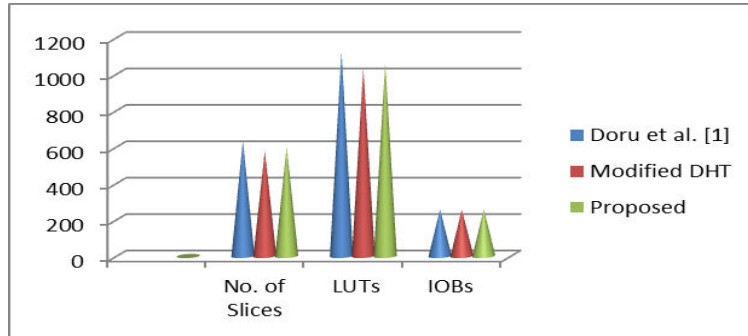


Figure 7: Show the bar graph of 8-bit DHT with word length 16

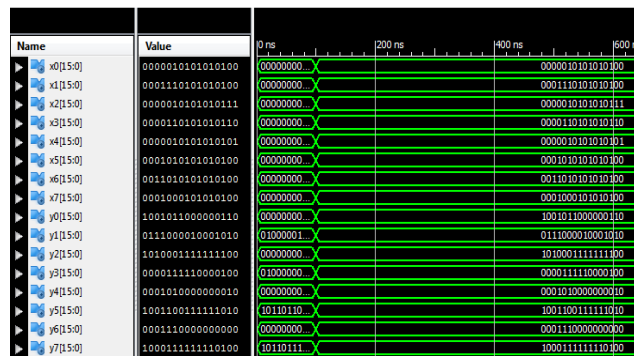


Figure 8: Output Waveform of 8-bit DHT with word length 16

V. CONCLUSION

DHT is a new transform used for real value to real value conversion. Pipeline is an ancient technique for multiplication. DHT is used in various fields such as image processing, space science, scientific applications etc. Delay provided and area required by hardware are the two key factors which are need to be consider.

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