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Optimization Delay of BCD Adders/ Sub-tractor using Modified Carry Select Adder

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ABSTRACT: The demand for massive computation increases day by day. It leads to the requirement of high-speed adders for arithmetic operations. We have modified the current adder designs and proposed modified carry select adders (CSLAs). A CSLA was proposed with a modified XOR gate in AND, OR and Inverter (AOI) logic. The modified XOR gate is expressed as $(A \cdot B) \cdot (A|B)$ instead of $(A \cdot B)|(A \cdot B)$. As a result, the half adder and the full adder of the CSLA are done with only four and nine gates respectively, but six and thirteen gates are used in the existing CSLAs. This area reduction in half adders and full adders decreases the overall area and power of the CSLA. Binary code decimal (BCD) is a special bit patterns are sometimes used for a sign or for other indications i.e. calculated error and overflow condition. In this paper, we has design is implementation based on MCLSA.

KEYWORDS: Binary Coded Decimal (BCD), Delay, Area, MCLSA

I. INTRODUCTION

CMOS technology plays a major role on the performance of VLSI circuits. The timing performance of the microprocessor can be improved by using dynamic circuits in microprocessors. However the usage of dynamic circuits in microprocessors is limited due to many challenges including transistor sizing, charge sharing, leakage current, noise immunity etc. Timing optimization of dynamic circuits can be achieved through several methods such as transistor sizing, using multiple threshold voltages etc. The aggressive scaling of transistors and interconnect dimensions has caused noise to become an increasingly important issue in integrated circuit design [1, 2]. A number of design techniques have been proposed to enhance the noise tolerance of domino logic circuit. The delay of the dynamic circuits can be controlled by varying the sizes of transistors in the circuit [3]. The circuit delay can be reduced by increasing the transistor sizes in the circuit. This means that high speed circuits require larger area. So for dynamic circuits, there is a tradeoff exist between speed and area. Domino logic circuits are the most widely used dynamic logic style. Domino logic circuits have two phases of operations-first phase called precharge phase and second phase called evaluation phase. During the precharge phase of the domino logic circuits, the clock remains low and the dynamic node is precharged to V_{DD} through a p-type pull up transistor. The evaluation phase starts when the clock transit from low to high and during this phase the pull down network evaluates the logic function. The important considerations in domino circuit design technique are charge sharing, leakage current, noise immunity and reliability. To improve the reliability and performance of domino logic circuits, a number of circuit techniques have been developed in the past three decades such as: 1) using a simple keeper 2) precharging the internal nodes 3) raising the source voltage 4) leakage current replica technique 5) conditional keeper technique 6) current comparison domino method etc. A domino logic circuit is inherently susceptible to noise due to floating nodes that may occur in the evaluation phase [4, 5]. The rate sensing keeper (RSK) technique based full adder circuit work based on the difference in the rate of change of voltage at the dynamic node of the gate during the ON and the leakage condition. The state of the keeper is controlled by a reference rate which is the average of the rate of change of voltage at the dynamic node of the gate during the ON and the leakage condition. One method to reduce the sub threshold leakage current in domino circuits is the usage of diode footer. The diode footer reduces the sub threshold leakage current in the domino circuit due to a phenomenon called the stacking effect.



II. BCD ADDERS

BCD viper involves BCD numbers as info and result [8]. Since a 4-cycle paired code has 16 unique twofold mixes, the expansion of two BCD digits might deliver inaccurate outcome that surpasses the biggest BCD digit (9)10 = (1001)BCD [8] [9] [10]. In such cases, the outcome should be rectified by add (6)10 = (0110)BCD to ensure that the outcome is a BCD digit. The resultant decimal convey yield produced by the remedy process is added to the following higher digit of the BCD addends.

Creators in paper [9] proposed an immediate execution of BCD viper circuit. They had proposed two unique designs for the development of LUT-based BCD viper circuit. A reality table had been shaped for each info/yield blend and the comparing circuit was proposed in first design. It consumed eleven 6-input LUTs. Two level of deliberation was performed for the subsequent engineering.

First least two huge info pieces were taken care of into the first level of circuits though the rest input bits alongside the result of the primary level were given to the second degree of the circuits. The subsequent methodology required seven number of 6-input LUTs with a much deferral. The immediate execution experiences a critical LUT-defer item.

The BCD viper proposed in [10] utilized Virtex-6 stage to execute their circuit design which had been proposed prior in [11]. Gao et al. proposed a BCD viper, where the first piece of the addends are added utilizing a full viper and the most huge three pieces are added utilizing 6-input LUTs [11].

A revision is guaranteed in 6-input LUTs by adding (3)10 to the aggregate assuming the amount of the main three pieces is more noteworthy than or on the other hand equivalents to (5)10. Additionally, additional circuits are required, when the amount of the main three pieces is (4)10 and the convey produced from the full viper is one. The circuit being sequential in design aside from the LUTs segments, calls for much time intricacy and defer which impedes quicker yield age [11]. Bioul et al. proposed a BCD snake, where increases were acted in a convey chain type design and hence, endured from a lot of deferral [12]. They utilized Virtex4 and Virtex-5 stage to show that the region upward (in terms of required number of LUTs) as for paired calculation isn't unimportant and it is multiple times in Virtex-4 and almost multiple times in Virtex-5. The principal reason of such distinction is because of the more mind boggling meaning of the convey spread and convey produce capacities. Creators in [13] proposed a BCD expansion strategy, where six is added as a remedy factor, when the amount of AU I +BU I approaches or more prominent than 8, where AU I also, BU I address the most huge three pieces of the info operands An and B, individually.

$$\begin{aligned}
 A &= 15.375 \text{ (Decimal)} = 0000\ 1111.0110 \text{ (Binary)} \\
 B &= 05.500 \text{ (Decimal)} = 0000\ 0101.1000 \text{ (Binary)} \\
 \text{Result} &= 20.875 \text{ (Decimal)} = 0001\ 0100.1110 \text{ (Binary)} \\
 &\text{(Obtained)} \\
 \text{Result} &= 20.9 \text{ (Decimal)} \\
 &\text{(Expected)}
 \end{aligned}$$

(a)

$$\begin{aligned}
 A &= 15.4 \text{ (Decimal)} = 0001\ 0101.0100 \text{ (BCD)} \\
 B &= 05.5 \text{ (Decimal)} = 0000\ 0101.0101 \text{ (BCD)} \\
 \text{Result} &= 20.9 \text{ (Decimal)} = 0010\ 0000.1001 \text{ (BCD)} \\
 &\text{(Obtained)} \\
 \text{Result} &= 20.9 \text{ (Decimal)} \\
 &\text{(Expected)}
 \end{aligned}$$

(b)

Fig. 1: Addition of fixed point decimal numbers: (a)using binary adders (b)using BCD adder

III. PROPOSED TECHNOLOGY

BCD binary numbers represent Decimal digits 0 to 9. A 4-bit BCD code is used to represent the ten numbers 0 to 9. Since the 4-bit Code allows 16 possibilities, therefore the first 10 4-bit combinations are considered to be valid BCD



combinations. The latter six combinations are invalid and do not occur BCD Code has applications in Decimal Number display System such as counters and digital clock. BCD numbers can be added together using BCD addition. BCD addition is similar to normal binary addition except for the case when sum of two BCD digits exceeds 9 or a carry is generated. When the sum of two BCD numbers exceeds 9 or a carry is generated a 6 is added to convert the invalid number into a valid number. The carry generated by adding a 6 to the invalid BCD digit is passed on to the next BCD digit.

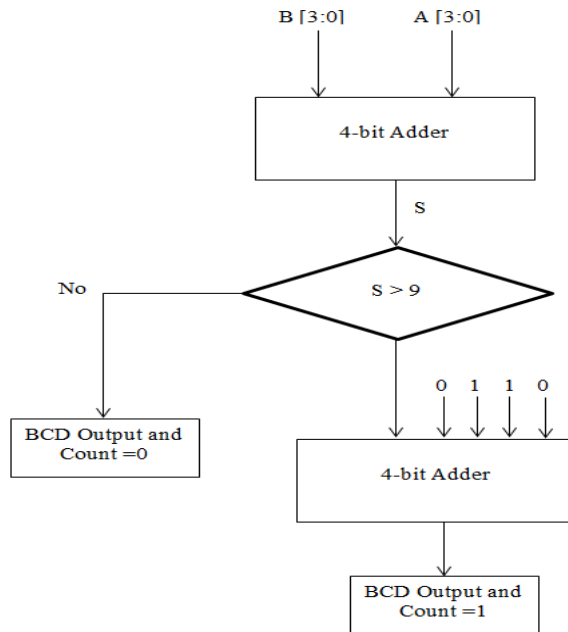


Fig. 2 (a): Flow Chart of BCD Adder

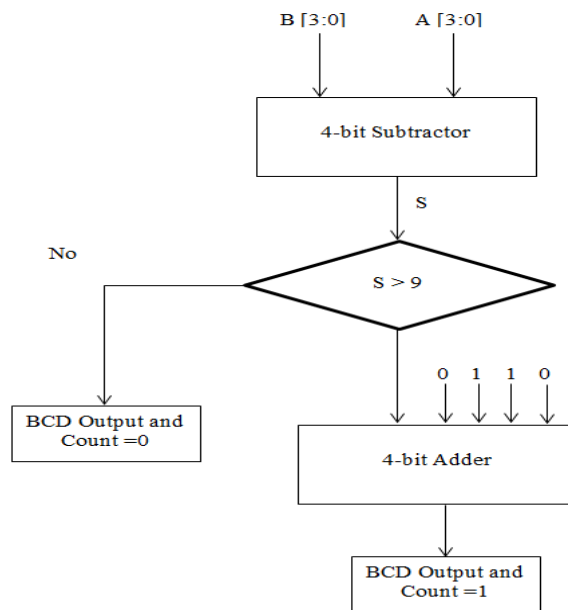


Fig. 2 (b): Flow Chart of BCD Sub-tractor

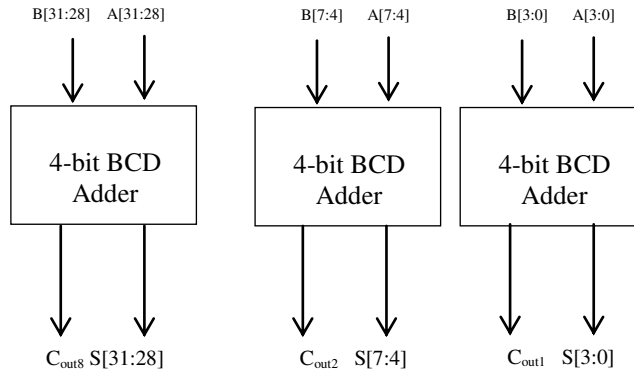


Fig. 3: Flow Chart of 32-bit Reversible BCD Adder

Carry Select Adder

If a XOR gate is realized with less number of gates in AOI logic, then there is a chance for reduction in the area and power consumption. Hence, we used alternative expression/approach for the XOR gate which is shown in equation 1.

$$A \oplus B = (\overline{A \cdot B}) \cdot (A|B)$$

Table 1: The size of RCA and CSLA groups are used in 4-, 8-, 16-, 32- and 64-bit conventional sqrt CSLA adder

Size of the CSLA Adder(bit)	RCA (bit)	CSLA (bit)
4	2	2
8	2	2 and 4
16	2	2, 3, 4 and 5
32	2	2, 3, 4, 6, 7 and 8
64	2	2, 3, 4, 5, 6, 7, 8, 8, 9 and 10

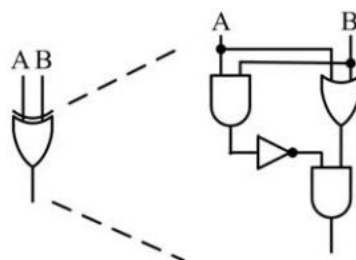


Fig. 4: A 2-input Modified XOR

The XOR gate is shown in Fig. 4, we call it as modified XOR gate. The advantage of the modified XOR gate is needed only four and nine gates for implementing HA and FA respectively. Furthermore, a modified XOR can act as HA. The HA using modified XOR gate is shown in Fig.3.2.b which is the same as Fig.3.4. In the conventional XOR gate, NOT gates are followed by AND gates and, finally, OR gate is presented but in the modified XOR gate AND and OR gates are presented in the first stage. Consequently, an additional AND gate is not required to find carry of HA. Further, only four gates are needed to implement the modified XOR gate. This modified XOR gate was used inside RCA and CSLA to reduce the gate count which leads to reduction in area as well as reduction in the power consumption of the CSLA. Moreover, the design is quite easy because the conventional XOR gate is replaced by the modified XOR gate.



IV. SIMULATION RESULT

VHDL is a standard hardware description language, which offers many useful features for hardware designing. It is a general purpose hardware description language that is easy to use and learn. It allows different levels of abstraction to be mixed in the same model. The level of abstraction used in terms of RTL, Behavioral, switches, gates code. VTS and RTL of 32-bit BCD adder/subtractor is shown in fig. 5 & 6.

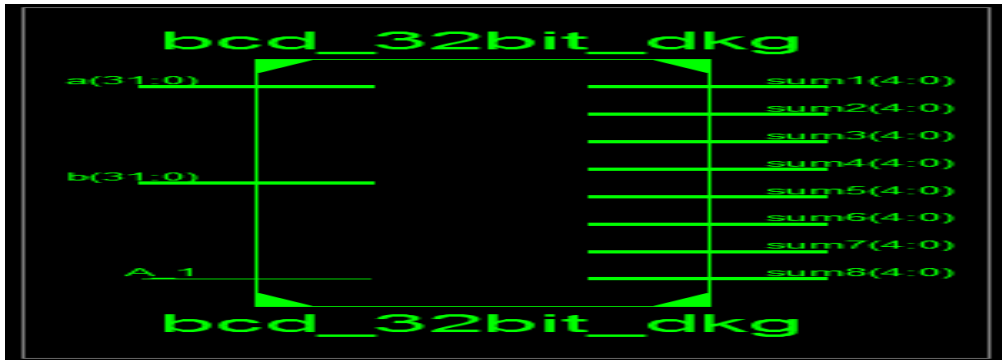


Fig. 5: VTS of 32-bit Adder/Subtractor using DKG Gate based on MCSLA

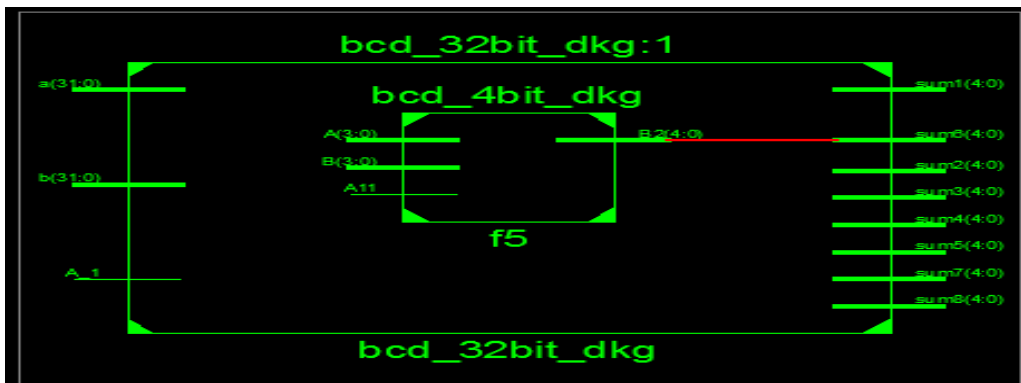


Fig. 6: RTL View of 32-bit BCD Adder/Subtractor using DKG Gate based on MCSLA

DUS and TS of 4-bit BCD adder/subtractor using MCSLA is shown in Table 7 & fig. 7. OW of 32-bit BCD adder/subtractor is represent in fig. 8.

Table 7: DUS of 32-bit BCD Adder/ Subtractor

bcd_64bit_peres Project Status (06/20/2017 - 17:48:11)			
Project File:	BCD_adder_subtractor.xise	Parser Errors:	No Errors
Module Name:	bcd_32bit_dkg	Implementation State:	Synthesized
Target Device:	xc6sxlx4-3tqg144	• Errors:	No Errors
Product Version:	ISE 14.1	• Warnings:	3 Warnings (1 new)
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)				[1]
Logic Utilization	Used	Available	Utilization	
Number of Slice LUTs	72	2400		3%
Number of fully used LUT-FF pairs	0	72		0%
Number of bonded IOBs	105	102		102%

Timing Summary:

Speed Grade: -3

Minimum period: No path found
 Minimum input arrival time before clock: No path found
 Maximum output required time after clock: No path found
 Maximum combinational path delay: 8.525ns

Fig. 7: TS of 32-bit BCD Adder/Subtractor using DKG Gate

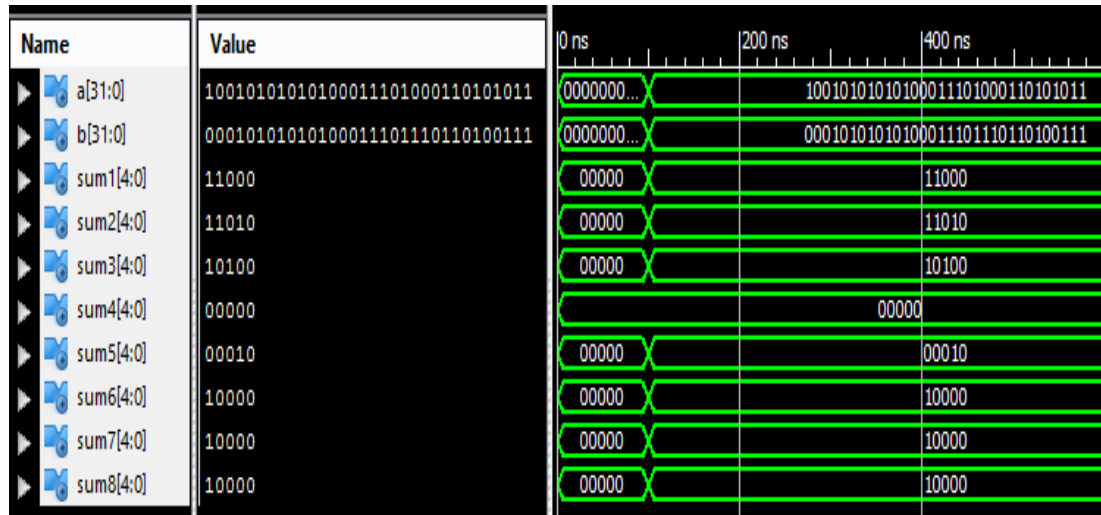


Fig. 8: OW of 4-bit BCD Adder/Subtractor using DKG Gate

V. CONCLUSION

Though we focused on BCD adder, we consider the binary adder also because a binary adder is a part of a BCD adder. One can boost the performance of a BCD adder by optimizing the binary adder used in it. Not only in a BCD adder, but a High speed and low power binary adder is also a need in many applications like Filter design, transform.

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