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RTL Design and Verification of Asynchronous SRAM

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ABSTRACT: The relentless demand for memory-intensive applications necessitates the development of efficient and high-capacity memory subsystems. Asynchronous Static Random Access Memory (SRAM) presents an attractive solution due to its potential for reducing power consumption, Re-configurable and improving performance. This study delves into the RTL (Register-Transfer Level) design and verification of a 1MB asynchronous SRAM, focusing on intricate aspects of its architecture, circuitry, and functionality. The key objectives of this work involve designing a robust RTL representation of the asynchronous SRAM, implementing its memory cell array, and addressing critical design challenges such as timing, power consumption, and reliability. Additionally, a thorough verification process is undertaken to validate the functionality, correctness, and performance of the designed SRAM. The results of this study aim to contribute to the advancements in asynchronous memory design, fostering innovation in high-capacity memory solutions for contemporary computing systems with Low power.

KEYWORDS: RTL (Register Transfer Level) Design , SRAM(Static Random access memory) , Asynchronous , Re-configurable.

I. INTRODUCTION

RTL (Register Transfer Level) design involves describing the behaviour of a digital circuit using registers, combinational logic and data flow. It's a level of abstraction used in digital design before actual circuit implementation. For the design of 1MB asynchronous SRAM (Static Random Access Memory), the RTL design would involve describing the behaviour of the memory cells, address decoding logic, read and write control, and any other necessary components at the register transfer level. Verification of such a design entails ensuring that the RTL description accurately represents the desired functionality of the SRAM. This includes verifying timing constraints, addressing conflicts, read and write operations, and power consumption. Asynchronous SRAMs also require careful consideration of timing hazards and race conditions due to their asynchronous nature.

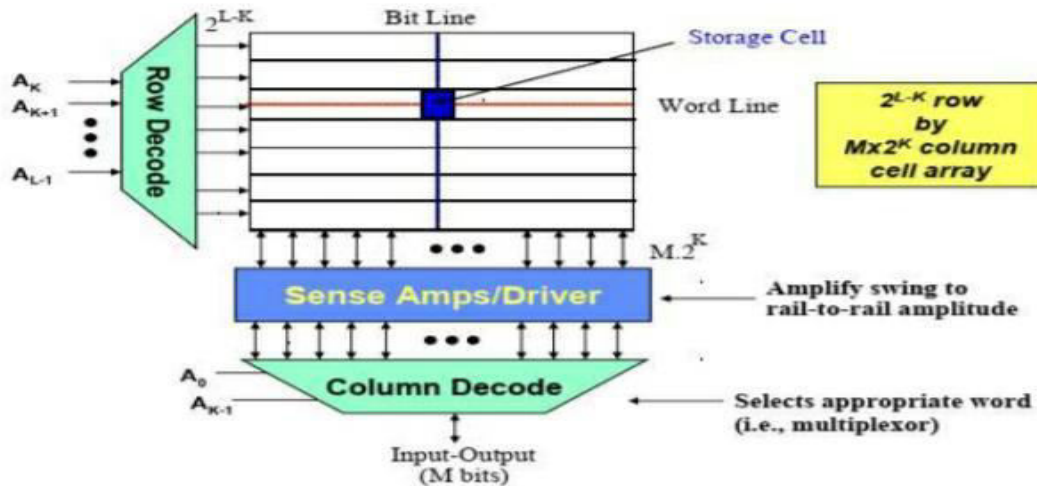
II. RTL DESIGN

The architecture of 1MB asynchronous SRAM involves several key components and organization principles to enable efficient storage and retrieval of data:

Array Organization : The SRAM comprises an array of memory cells arranged in rows and columns. Each memory cell stores a single bit of data. The total number of memory cells is determined by the size of the SRAM (1MB in this case)

Word line and Bit line Structure : Word lines (WL) are horizontal lines that connect to the gates of memory cells in each row. Bit lines (BL and BLB) are vertical lines that connect to the sources/drains of memory cells in each column. Each intersection of a word line and a bit line represents a memory cell.

Sense Amplifiers : Sense amplifiers are used to amplify the small voltage differentials on the bit lines during read operations. They enable the SRAM to accurately detect the stored data in the memory cells.



Address Decoding Logic : Decodes the input address to select the appropriate row and column of memory cells for read or write operations. Typically implemented using a combination of multiplexers, decoders, and logic gates.

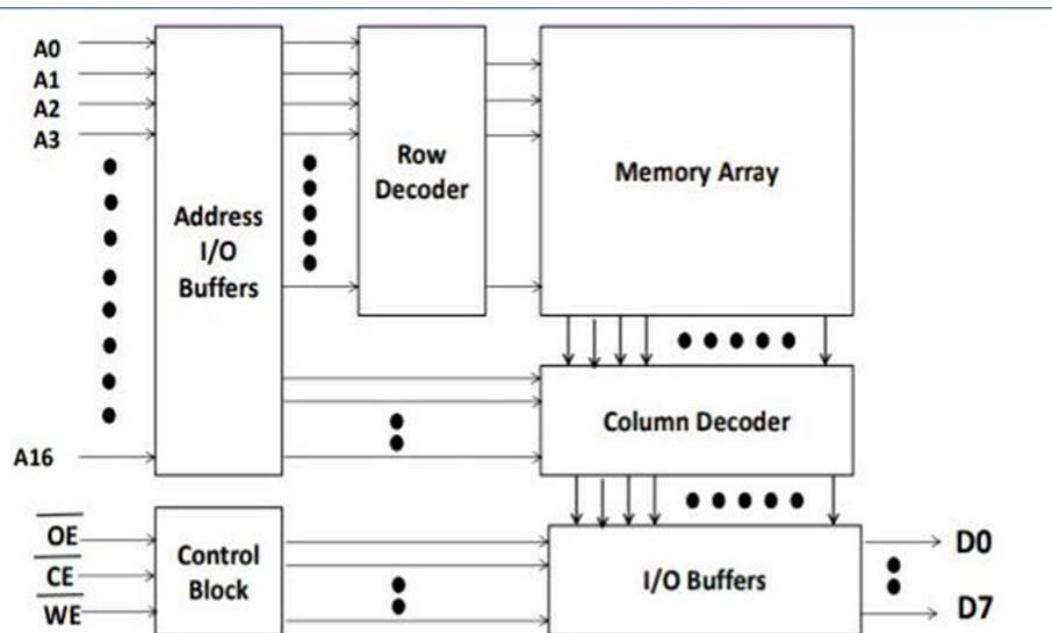
- **Row decoder :** Row decoders are typically implemented using a combination of logic gates, such as NOR or NAND gates, along with multiplexers and inverters. The number of address lines determines the size and complexity of the row decoder.
- **Column decoder :** Column decoders are similar to row decoders. The number of address lines determines the size and complexity of the column decoder. Each column decoder output corresponds to a specific column within the activated row of the memory array.
- **Row Multiplexer :** Row Multiplexer is going to receive input signals from the row decoder, which indicate the desired row address, and generate corresponding control signals to activate the selected word line. The number of input lines and selection lines in the multiplexer depends on the size of the memory array and the number of rows.
- **Column Demultiplexers :** Column Demultiplexers are receive input signals from the column decoder, which indicate the selected column address, and generate control signals to route the data from the selected memory cells to the appropriate output lines.

Control Logic : Generates control signals to coordinate read and write operations. Includes signals such as Write Enable (WE), Chip Enable (CE), Output Enable (OE), and Read/Write .

Write Drivers : Amplify and drive the data to be written into the selected memory cells during write operations. Ensure that the data is reliably stored in the memory array.

Power Management : Implements techniques such as power gating to manage power consumption during standby and active modes. Ensures that power is supplied to the necessary components only when needed to conserve energy.

Timing Control : Generates timing signals to synchronize the operation of various components. Ensures proper sequencing of read and write operations and timing margins to account for process variations and environmental conditions.



The architecture of a 1MB asynchronous SRAM is designed to provide fast, reliable, and low-power storage of data in digital systems. It leverages the organization of memory cells into arrays, along with control logic and timing control, to enable efficient access to stored data.

III. VERIFICATION METHODOLOGY

Study of an outline outlining the verification plan, simulation environment, tools used, and testbench development process for RTL design and verification of a 1MB asynchronous SRAM:

1. Verification Plan and Goals :Introduction to the importance of verification in RTL design and its role in ensuring the correctness and reliability of the 1MB asynchronous SRAM. Definition of verification objectives, including functional correctness, timing compliance, power consumption and scalability Explanation of verification methodologies, such as simulation-based verification, formal verification, analysis. Establishment of verification metrics and target coverage goals to measure the completeness of effectiveness of the verification process.

2. Simulation Environment : Description of the simulation environment used for RTL verification, including hardware and software components. Specification of the computing resources required for running simulation tests and executing verification methodologies. Explanation of the RTL simulator(s) utilized, such as Model Sim, VCS, or Questa, and their capabilities in handling large-scale designs.

3. Verification Tools : Overview of the verification tools employed for RTL design and verification of the 1MB asynchronous SRAM. Explanation of the functionalities and features of the tools, including simulation, formal verification, and timing analysis capabilities. Examples of industry-standard tools like Synopsys VCS, Cadence Incisive, and Mentor Graphics Questa used for RTL verification.

4. Testbench Development Process : Definition of the testbench development process and its importance in verifying the functionality and performance of the RTL design. Explanation of the components of a testbench, including stimulus generation, response checking, and coverage tracking. Description of the methodology for developing comprehensive test cases covering all aspects of SRAM operation, including read, write, power-up, and power-down sequences. Implementation of self-checking mechanisms within the testbench to automatically verify test results and detect errors.

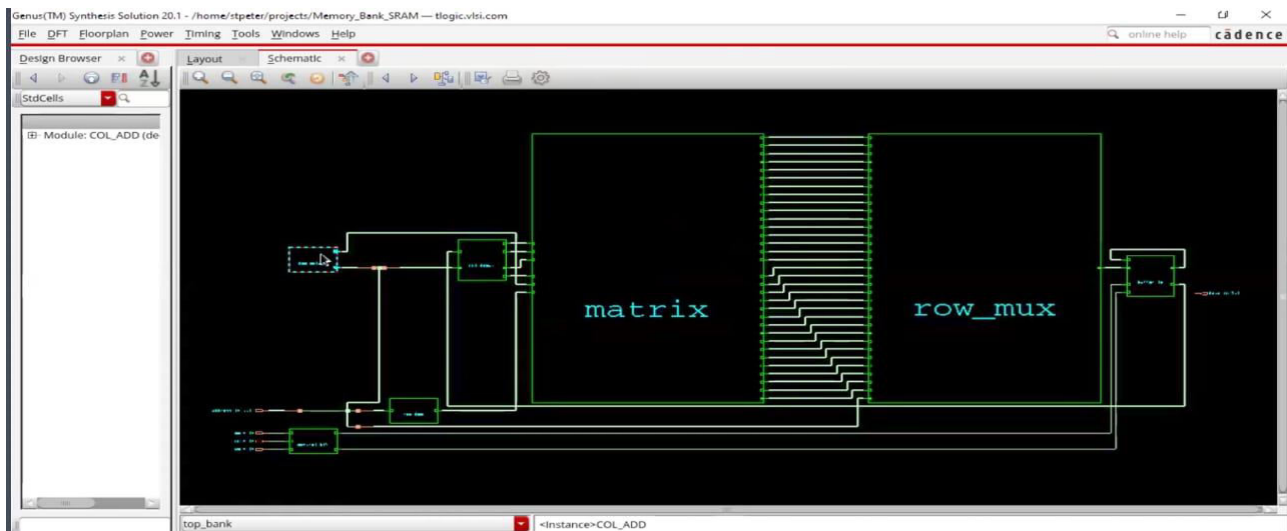
5. Verification Flow : Outline of the verification flow followed during the RTL design and verification of the 1MB asynchronous SRAM. Step-by-step explanation of the verification process, including simulation runs, formal



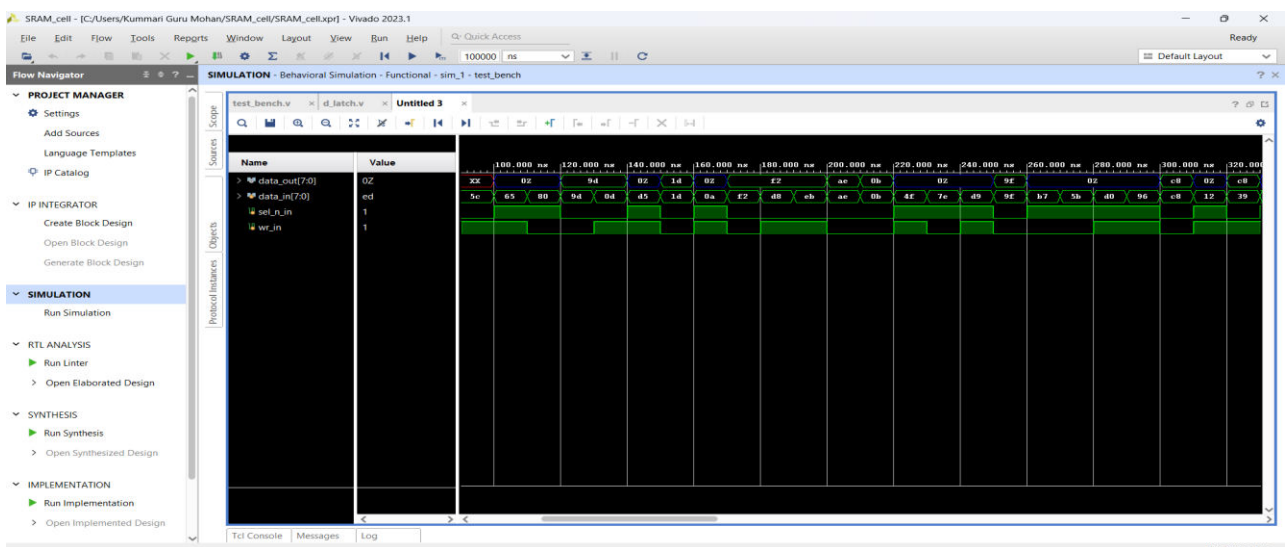
verification checks, timing analysis, and debug activities. Discussion of the integration of testbenches with verification tools and simulation environments to execute verification tests efficiently.

IV. RESULT AND DISCUSSION

1. Functional Correctness Verification : Presentation of simulation results showing the functional correctness of the 1MB asynchronous SRAM design. Discussion of how the SRAM performs read and write operations correctly under various test scenarios. Analysis of any discrepancies or errors encountered during functional verification and their resolutions.



2. Timing Verification : Presentation of timing analysis results demonstrating that read and write operations meet specified timing constraints. Discussion of how the SRAM design achieves desired access times and cycle times, ensuring reliable operation in practical applications. Analysis of any timing violations or margin issues identified during timing verification and their mitigation strategies.



3. Power Consumption Verification : Presentation of power analysis results showing the power consumption profile of the 1MB asynchronous SRAM design. Discussion of power-saving features implemented in the design and their effectiveness in reducing power consumption during different operating modes. Analysis of power hotspots or areas of high power consumption and potential optimizations to mitigate them.



Power Details Report — tlogic.vlsi.com
 Generated by: Genus(TM) Synthesis Solution 20.12-s150_1 (Oct 14 2021 10:38:13)
 Generated on: Apr 08 2024 16:30:43
 Module: design_top_bank
 Technology library: fast_ddd1v0 1.0
 Operating conditions: PVT_1P1V_0C (balanced_tree)
 Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
top_bank/BANK/ 18	34.098	249.127	0.000	249.127	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BANK/ 18	34.098	250.659	0.000	250.659	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BANK/ 18	34.098	250.659	0.000	250.659	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BANK/ 18	34.098	250.659	0.000	250.659	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BANK/ 18	34.098	250.659	0.000	250.659	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BANK/ 18	34.098	250.659	0.000	250.659	
top_bank/BANK/ 8	21.437	133.333	0.000	133.333	
top_bank/BIO 16	23.827	231.315	0.000	231.315	
top_b...L_ADD 0	0.000	0.000	0.000	0.000	
top_bank/CONT 5	2.472	65.557	0.000	65.557	
top_ba...UX_COL 38	24.697	280.751	0.000	280.751	
top_b...X_ROW 57	118.112	1276.914	0.000	1276.914	
top_b...W_ADD 49	18.965	352.798	0.000	352.798	
top_bank	2469	4552.614	36391.327	0.000	36391.327

4. Scalability and Performance : Discussion of how the RTL design scales with increasing memory size and complexity. Presentation of performance metrics such as area utilization, access time, and operating frequency, demonstrating the scalability of the design. Comparison of the performance of the 1MB asynchronous SRAM design with similar designs or industry standards.

Gate Count Report — tlogic.vlsi.com
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 Generated on: Apr 08 2024 16:27:15
 Module: design_top_bank
 Technology library: fast_ddd1v0 1.0
 Operating conditions: PVT_1P1V_0C (balanced_tree)
 Wireload mode: enclosed

Instance	Cells	Cell Area	Net Area	Total Area	Wireload	WL Flag
top_bank/BANK/ 8	42.709	0.000	42.709			(3)
top_bank/BANK/ 18	68.067	0.000	68.067			(5)
top_bank/BANK/ 8	42.709	0.000	42.709			(5)
top_bank/BANK/ 18	68.067	0.000	68.067			(5)
top_bank/BANK/ 8	42.709	0.000	42.709			(5)
top_bank/BANK/ 18	68.067	0.000	68.067			(5)
top_bank/BANK/ 8	42.709	0.000	42.709			(5)
top_bank/BANK/ 18	68.067	0.000	68.067			(5)
top_bank/BANK/ 8	42.709	0.000	42.709			(5)
top_bank/BANK/ 18	68.067	0.000	68.067			(5)
top_bank/BANK/ 8	42.709	0.000	42.709			(5)
top_bank/BIO 16	42.709	0.000	42.709			(5)
top_b...L_ADD 0	0.000	0.000	0.000			(5)
top_bank/CONT 5	9.343	0.000	9.343			(5)
top_ba...UX_COL 38	98.764	0.000	98.764			(5)
top_b...X_ROW 57	818.140	0.000	818.140			(5)
top_b...W_ADD 49	134.800	0.000	134.800			(5)
top_bank	2469	9816.351	0.000	9816.351		(5)

Filtering: 9816.35

V. CONCLUSION

This verification plan outlines the objectives, methodologies, metrics, and flow for verifying the RTL design of a 1MB SRAM. It provides a structured approach to ensuring the correctness and reliability of the RTL implementation before fabrication and integration into larger digital systems. This outline provides a structured approach to developing a verification plan, setting up a simulation environment, selecting appropriate tools, and developing testbenches for verifying the RTL design of a 1MB asynchronous SRAM. It emphasizes the importance of thorough verification to ensure the functionality, timing compliance, and power efficiency of the SRAM design.



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