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[ijrset@gmail.com](mailto:ijrset@gmail.com)

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# Field Programmable Gate Array Based Vehicle Collision Avoidance System

R.JeevaRekha<sup>1</sup>, S.Suriya<sup>2</sup>, M.Thanush<sup>3</sup>, R.Viveka<sup>4</sup>

Assistant Professor, Department of Electronics and Communication Engineering, Muthayammal Engineering College,  
Tamil Nadu, India.<sup>1</sup>

UG Students, Department of Electronics and Communication Engineering, Muthayammal Engineering College,  
Tamil Nadu, India.<sup>2,3,4</sup>

**ABSTRACT:** A collision avoidance system, also known as a pre-crash system, forward collision warning system, or collision mitigation system, is a sophisticated driver-assistance system that aims to avoid or mitigate the severity of a collision. For this research, collision avoidance system will be fabricating to show that this system can detect avoidance range before apply the braking action to prevent collision. The ultrasonic sensor will be used in this system to detect the avoidance range. In this collision avoidance system, there will be uses of Field Programmable Gate Array (FPGA) and Complex Programmable Logic Device (CPLD). This research will observe how to implement FPGA and CPLD in the collision avoidance system using Verilog Hardware Description Language (HDL). The VHDL will be done in Xilinx ISE Software. In this research, Xilinx Spartan 6 Standard board has been used.

**KEYWORDS:** Live box, GSM module, GPS, Panic switch

## I. INTRODUCTION

The FPGA is called 'fine-grain' because it consists of numerous small logic blocks, possibly numbering in the thousands. It includes flip-flops, combination logic, and memory. Accidents result in severe damage, significant injuries, and even fatalities. These incidents are often due to drivers delaying braking. Preventative measures like enhancing visibility, automatic headlights, windshield wipers, tire traction, etc., have been implemented to decrease the likelihood of accidents. Presently, efforts are focused on actively evading accidents and enhancing protection for vehicle occupants and pedestrians. Therefore, this paper proposes a new automated vehicle collision avoidance system. This initiative aims to create a system that can automatically stop vehicles when obstacles are detected by sensors, eliminating the need for manual braking by drivers. The focus of this paper is on developing a sensor-based embedded system that aids drivers in avoiding collisions on the road to save lives and prevent financial losses.

## II. REVIEW OF LITERATURE

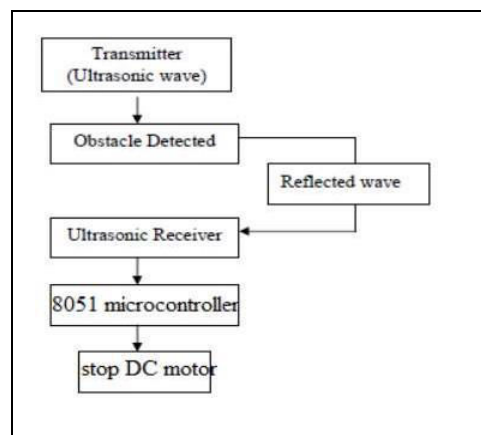
**Antora, S.S., Chang, Y.K., Nguyen-Quang, T. and Heung, B., 2023. Development and Assessment of a Field-Programmable Gate Array (FPGA)-Based Image Processing (FIP) System for Agricultural Field Monitoring Applications. AgriEngineering, 5(2),pp.886-904.**

Field imagery is an effective way to capture the state of the entire field; yet, current field inspection approaches, when accounting for image resolution and processing speed, using existent imaging systems, do not always enable real-time field inspection. This project involves the innovation of novel technologies by using an FPGA-based image processing (FIP) device that eliminates the technical limitations of the current agricultural imaging services available in the market and will lead to the development of a market-ready service solution. The FIP prototype developed in this study was tested in both a laboratory and outdoor environment by using a digital single-lens reflex (DSLR) camera and web camera, respectively, as the reference system. The FIP system had a high accuracy with a Lin's concordance correlation coefficient of 0.99 and 0.91 for the DSLR and web camera reference system, respectively. The proposed technology has the potential to provide on-the-spot decisions, which in turn, will improve the compatibility and sustainability of different land-based systems.

**Majoral, M., Fernández-Prades, C. and Arribas, J., 2023. A Flexible System-on-Chip Field-Programmable Gate Array Architecture for Prototyping Experimental Global Navigation Satellite System Receivers. Sensors, 23(23), p.9483.**

Global navigation satellite system (GNSS) technology is evolving at a rapid pace. The rapid advancement demands rapid prototyping tools to conduct research on new and innovative signals and systems. However, researchers need to deal with the increasing complexity and integration level of GNSS integrated circuits (IC), resulting in limited access to modify or inspect any internal aspect of the receiver. To address these limitations, the authors designed a low-cost System-on-Chip Field-Programmable Gate Array (SoC-FPGA) architecture for prototyping experimental GNSS receivers. The proposed architecture combines the flexibility of software-defined radio (SDR) techniques and the energy efficiency of FPGAs, enabling the development of compact, portable, multi-channel, multi-constellation GNSS receivers for testing novel and non-standard GNSS features with live signals. This paper presents the proposed architecture and design methodology, reviewing the practical application of a spaceborne GNSS receiver and a GNSS rebroadcaster, and introducing the design and initial performance evaluation of a general purpose GNSS receiver serving as a testbed for future research. The receiver is tested, demonstrating the ability of the receiver to acquire and track GNSS signals using static and low Earth orbit (LEO)-scenarios, assessing the observables' quality and the accuracy of the navigation solutions.

### III. METHODOLOGY



Utilizing an ultrasonic sensor for collision detection. Alert beep sound notification on the system for collision indication distance. Implementation of braking through a servomotor linked to the rear drum brake parking cable to ensure optimal braking force and minimize braking distance. A notable speed difference may signal a possible collision, prompting the vehicle collision avoidance system to calculate potential obstacles. If the speed difference between the vehicle and any front-end object is significant, the system may execute various actions. Basic collision avoidance systems will produce a warning beep sound, giving the driver time to brake or steer away. In certain scenarios, the system may pre-charge the brakes in conjunction with automatic braking for added assistance. This can provide the driver with significant braking power upon pedal depression, potentially reducing accident severity. If the vehicle ahead is too close, the system alerts the driver with audio and visual warnings to take preventive measures. As the distance between the two vehicles decreases further, the system issues a tactile warning beep and applies light braking. In situations where an accident seems imminent, the system engages the brakes to avert a collision.

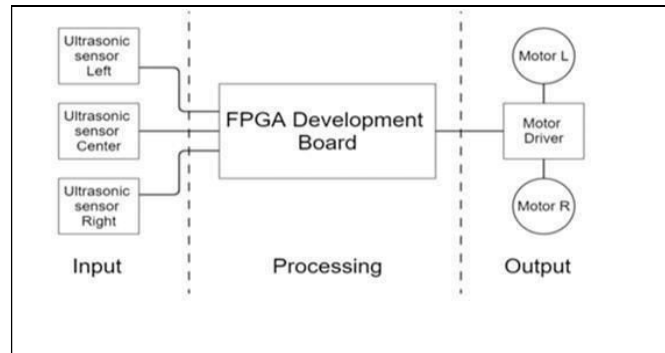
#### 3.1 EXISTING SYSTEM

Their research about technology to allow to detect an impending collision with another vehicle an obstacle and automatically the brakes. Using a ultrasonic sensor and an 8051 microcontroller the system flow is. In the existing system the systems sound an to notify drivers that collision may be imminent a sound to alert driver and get him or ready to take every action. The accidents mostly caused by a delay of the driver to hit the brake. There have been suggestions for an automated anti-collision system that uses a sharp distance sensor to identify only impediments, sends out alerts when the car is about to collide, and tries to stop the car on its own without the driver's assistance.

#### 3.2 PROPOSED SYSTEM

Three subsystems make up the mobile robot obstacle avoidance system.

1. A 120° range of ultrasonic sensors for obstacle detection
2. XILINX SPARTAN 6 Mini FPGA Development Board, a tiny FPGA board
3. An H-bridge motor driver is used to power two DC motors.



**BLOCK DIAGRAM**

### 3.3 Working Principle:

The ultrasonic sensor operates at 5V, while the FPGA board operates at 3.3V. Providing a trigger signal of 3.3V is sufficient for the ultrasonic sensor, but the 5V echo signal it produces could harm the FPGA board. To address this issue, a voltage divider is utilized to adjust the echo signal level. In terms of programming the FPGA development board for the HC-SR04 ultrasonic sensor module, two essential components are required: a trigger generator and a counter. The trigger generator produces a 10uS pulse every 100ms, triggering the ultrasonic sensor to emit an echo pulse proportional to the distance. This echo pulse is then sent to the counter as the enable input, which in turn produces a numerical value corresponding to the distance. The counter resets its value to '0' with each trigger, and to achieve a quicker response, reducing the time between triggers is crucial. The datasheet specifies that the minimum time between pulses should be at least 60ms.

### 3.4 Hardware Description:

- Xilinx Spartan 6 FPGA board.
- DC motor controller
- Ultra Sonic Sensors
- DC motor

#### 1.Xilinx Spartan 6 FPGA board

The FPGA development board used in this mini project is the Xilinx Spartan FPGA. The FPGA development board is responsible for generating the PWM signal, taking readings from the ultrasonic sensor and movement of the motors. According to the VHDL program the FPGA chip takes input from the ultrasonic sensor and detect obstacles. Then according to a rule base the movement of the motors are controlled in order to get away from the obstacle and move forward.

#### 2.DC motor controller

Motor driver is used to control motion of a motor and its direction by feeding current accordingly. Output of a motor driver is in digital form so it uses PWM (Pulse Width Modulation) to control speed of a motor. Motor Driver are basically current amplifiers followed by input signals.

#### 3.Ultrasonic Sensor:

Ultrasonic Sensor module is low cost, high performance sensor and provides stable and high ranging accuracy. The module includes ultrasonic transmitter, receiver and control circuit. The module is relatively controller. Its ranging distance is 2cm to 350cm with 3mm accuracy.

#### 4.DC motor:

To move the mobile platform forward, backward, turn left right two 12V 300rpm geared motors are used. In order to operate the motors L298N motor driver was used. The PWM signal generation is done by the FPGA development board. For this two VHDL entities are needed. When a PWM pulse is supplied to the motor driver it controls the speed of the motors accordingly. There are two pins for each motor for direction control.

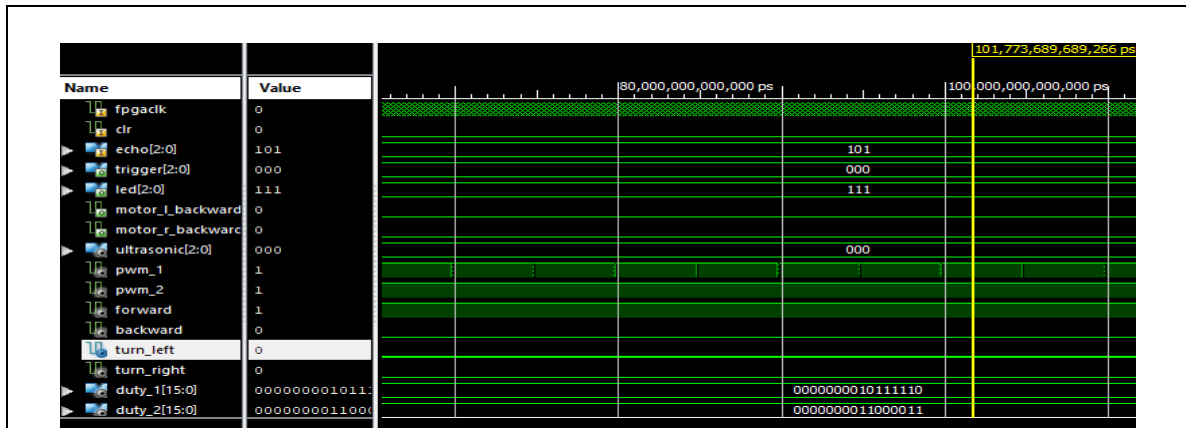
### 3.5 Processing FPGA Development Board:

It could be a improvement board without coordinates peripherals. It is worked from a 50MHz



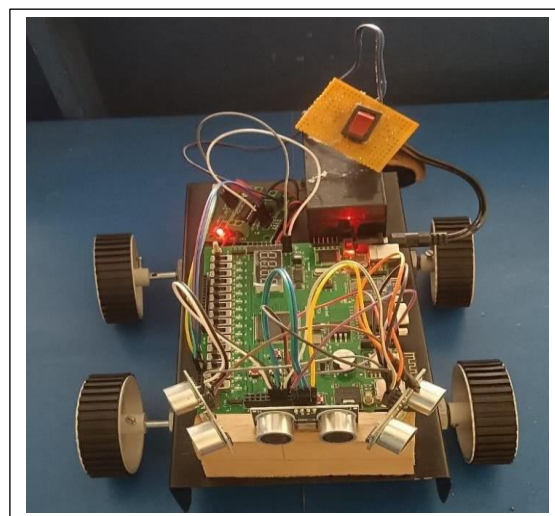
precious stone oscillator. There are 89 I/O pins. The FPGA change board is careful for making the PWM hail, taking readings from the ultrasonic sensor and advancement of the motors. The VHDL programs were composed from Xilinx ISE computer program. According to the VHDL program the FPGA chip takes input from the ultrasonic sensor and identify obstacles. At that point agreeing to a run the show base the development of the engines are controlled in arrange to urge absent from the impediment and move forward. The separate to keep absent is defined by the designer. This separate is set as 20cm. This esteem isn't taken from an experimental procedure. So that, it might not be the leading esteem for the versatile robot to function efficiently. As there's an cluster of three ultrasonic sensors, three inputs are fed into the best level substance. Then concurring to the run the show base appeared in table 2, the motors are worked. The PWM changes powerfully in arrange to urge the specified development. For illustration, to move in reverse in right course a moo PWM esteem is set for the proper engine wheel and a tall PWM value is set for the cleared out engine.

IV. RESULT



The software Stimulation was shown that vehicle can move and avoid the obstacle in vivado by using Verilog HDL

Here shown that Hardware output of vehicle collision avoidance by using Ultrasonic Sensor with FPGA spartan 6 board .



## V. CONCLUSION

FPGA is the processing unit, the robot's size, cost, and execution time are all reduced. FPGAs are very dependable in terms of speed and accuracy since they enable the construction of gate-level architecture. They have an edge over current microcontrollers because of this. Because only the shortest path is implemented while using FPGA, power dissipation is decreased. In order to ensure quick computing with the least amount of hardware, the system can accomplish parallelism by creating numerous instantiations of the same elementary level modules and using them in parallel. Power dissipation is observed to be significantly reduced when a network of many robots is installed.

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