

A Proposed 0.4V Bulk Driven CMOS Inverter

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ABSTRACT:The last few decades, a great deal of attention has been paid to low-voltage (LV) low-power (LP) integrated circuits design since the power consumption has become a critical issue. The low power design can utilize a smaller size and lighter-weight battery. A lot of research has been done on several LV and LP complementary metal oxide- semiconductor (CMOS) integrated circuit design techniques. Among many techniques used for the design of LV LP integrated circuits, the Bulk-driven (BD) principle offers a promising route towards this design for many aspects mainly the simplicity. In this paper the advantages of the proposed 0.4V BD-CMOS inverter compared to the conventional Gate-Driven (GD) CMOS inverter with 180nm technology in Cadence Virtuoso is presented.

KEYWORDS:Bulk-Driven, CMOS Inverter, Low voltage, Low power, MOST.

I. INTRODUCTION

The proliferation of portable and wireless electronic systems has made low power a key requirement in CMOS very large scale integrated (VLSI) circuit and system designs. For CMOS digital circuits, the dynamic power and static powers are directly proportional to the square of the supply voltage and supply voltage respectively. Hence, reducing the supply voltage is the most efficient method to reduce dissipation of power of digital circuits. However, for digital circuits, there are several problems associated with lowering the supply voltage such as decreased MOS Transistor (MOST) drivability, reduced signal swings and increased threshold variations [1]. Another related issue of scaling down the power supply voltage is threshold voltage restriction. The threshold voltage scaling, however, has the limitations that the components of threshold voltage due to built-in-junction potential and bulk charge in the channel do not scale down as desired. There also exists a lower limit in scaling down the threshold voltage because of problems such as increased parasitic effects, short channel effects and leakage current in the scaled down devices and these problems are much more severe in this case than in large feature - size devices [2].

Increased integration in portable applications creates wide demand for ICs that can process both analog signal and digital logic on a single chip. Although, different supply voltages can be used for the analog and digital parts in a mixed-signal design, this is not an appropriate solution, as special interface circuits are required between them, which complicate the design of the supply sources. This has forced mixed-signal circuit designers to divert from conventional circuit architectures to new low-voltage transistor implementation techniques as they become nonfunctional and inefficient in a reduced supply environment. Some of the low-voltage transistor implementation techniques used to reduce supply voltages are bulk-driven MOSTs, self-cascode MOSTs, floating-gate MOSTs (FG-MOST), level shifter techniques and sub-threshold MOSTs [3].

II. BULK DRIVEN PRINCIPLE

The An important factor concerning analog and digital circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. The equation of threshold voltage is

$$V_T = V_{T0} + \gamma \left(\sqrt{2|\varphi_F| + V_{SB}} - \sqrt{2|\varphi_F|} \right) \quad (1)$$

Where,

V_{T0} is the threshold voltage at zero bulk source voltage, φ_F is the Fermi potential, γ is the body effect coefficient.

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A bulk-driven MOST has been used to reduce the threshold voltage, it is well known that reverse bias voltage on the well-source junction will cause to increase the threshold voltage. Similarly, a forward bias on well-source junction will cause decrease the threshold voltage. The bulk-driven transistor technique is a better solution to reduce the limitation of threshold voltage [4]. Because the bulk-driven transistor is work like a depletion type device, it can operate under zero, negative or even slightly positive biasing condition as shown in fig. 1. Where v_{in} representing the input at the bulk of MOST and v_b representing the biasing at the gate of MOST.

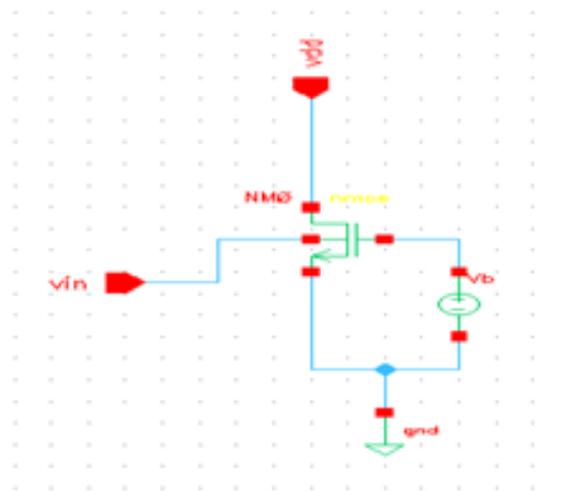


Fig 1.BD-MOS transistor.

The bulk-driven MOST operation is much like a JFET. To operate bulk-driven MOST, firstly bias the gate to create a conduction channel (inversion layer) by biasing the gate terminal to a fixed voltage that is sufficient to create an inversion layer (e.g., $V_{GS} > V_T$ in case of NMOS). This inversion layer will very much like a JFET conduction channel by applying a potential difference between drain and source. Since the thickness of the depletion region associated with the conduction channel (inversion layer) affects by the bulk voltage, so by varying the bulk voltage through the body effect of the MOST can be modulated the drain current.

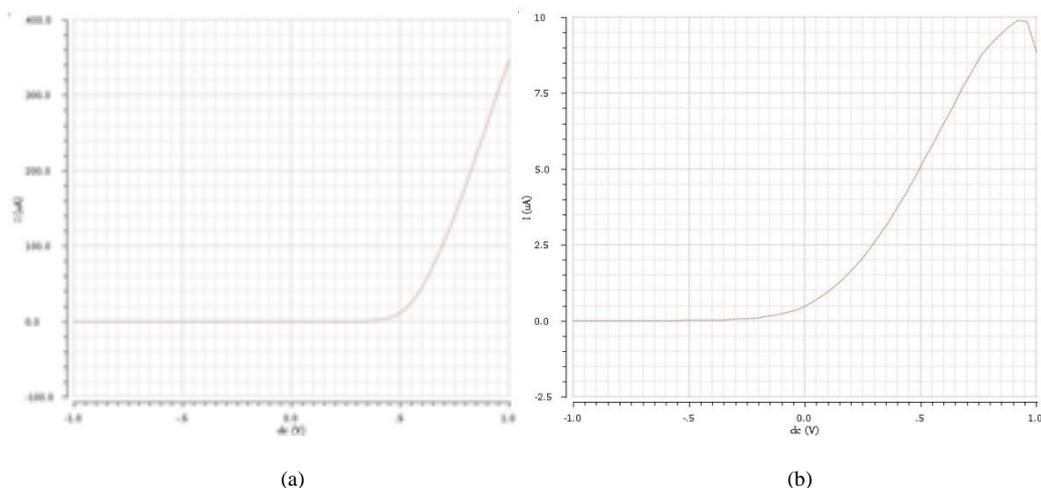


Fig 2. Drain currents versus: a) gate-source voltage of GD-MOST b) bulk-source voltage of BD-MOST.

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From the drain current versus voltage characteristics as shown in Fig. 2, we can consider from the graph that the threshold voltage of NMOS using BD-MOS transistor technique becomes negligible or removed as compare to the GD-MOS transistor i.e. Transistor is operating at less than 0V threshold voltage.

III. GATE DRIVEN CMOS INVERTER

As inverter is truly the nucleus of all digital designs. The electrical behaviour of complex circuits can be almost completely derived by extrapolating the results obtained for inverters. Fig. 3(a).a static CMOS inverter, when the input voltage is low (0V), NMOST is off and PMOST on. A path exists between vdd and vout, yielding a high output voltage. On the other hand, When Vin is high and equal to vdd, the NMOST is on, while the PMOST is off. A direct path exists between vout and the ground node, resulting in a steady-state value of 0V [4]. This functionality shows fig. 3(a) work as an inverter.

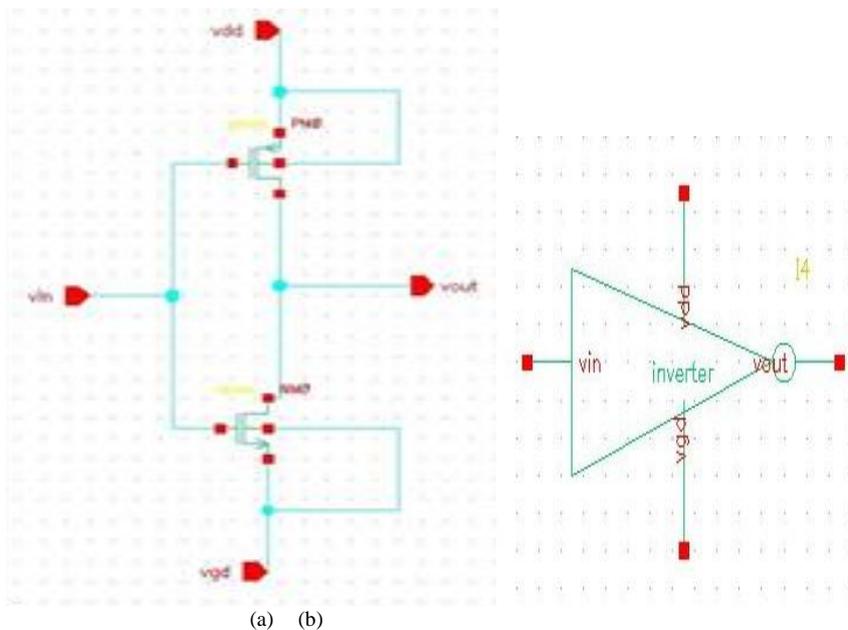


Fig 3.a) CMOS inverterb) symbol.

IV. A PROPOSED BD-CMOS INVERTER

Fig. 4(a) shows a CMOS inverter where the MOST (NMOST and PMOST) is used as a four terminal device under forward body-bias condition. The back gate forward body-bias method shown in fig. 1 is compatible with CMOS processes. Without any technology modification, the threshold voltage can be removed electrically. When fixed the gate to source voltage ($V_{in} > V_T$) to off the PMOST and to sufficiently create conducting channel of NMOST and apply signal to the bulk of NMOST (v_{bn}) this will affect thickness of depletion region associated with inversion layer. Due to this technique it will reduce the operating time of NMOST i.e. reduces the threshold voltage of NMOST and produces the output at low supply voltage (i.e.0.4V). Similarly, fixed the gate to source voltage ($V_{in} < V_T$) to off the NMOST and to sufficiently create conducting channel of PMOST and apply signal to the bulk of PMOST (v_{bp}) this will affect thickness of depletion region associated with inversion layer. Due to this technique it will reduce the operating time of PMOST i.e. reduces the threshold voltage of PMOST and produces the output at low supply voltage (i.e.0.4V). So bulk driven technique reduces the supply voltage power dissipation of CMOS inverter.

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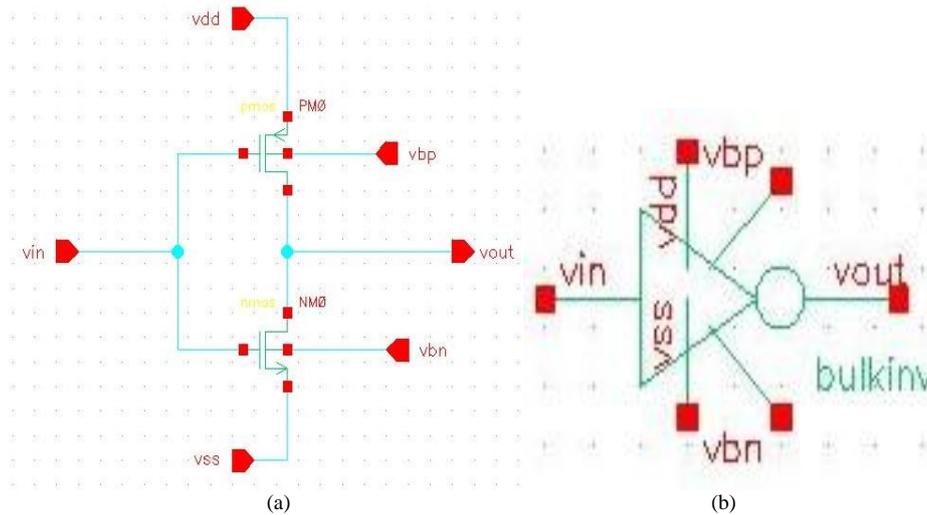


Figure 4.a) BD-CMOS inverter b) symbol.

The drawback of this implementation is that transconductance (g_{mb}) of the bulk-driven MOSFET is considerably less than the transconductance (g_m) of the conventional MOSFET (factor of 0.1 to 0.3) [5]. This results in lower gain-bandwidth product and poor frequency response as compared to conventional MOSFET. The bulk-driven MOSFETs also have a technology limitation, i.e. n-type bulk-driven MOSFETs can only be implemented in p-well process technology and vice versa. These disadvantages of bulk-driven MOSFETs limit their use in low-voltage circuits.

V. EXPERIMENTAL RESULTS

As power dissipation and supply voltage are the two main factors for implementation of digital circuits. With the help of ‘CADENCE VIRTUOSO’ EDA tool using 180nm technology, comparison between the performance in term of supply voltage, power dissipation, delay, and threshold voltage of conventional Gate- Driven CMOS inverter and Bulk-Driven CMOS inverter are shown in Table 1 and Table 2 respectively.

Table 1.Observation of conventional GD-CMOS inverter.

Vdd (V)	Vdd (V)	Power dissipation (W)	Delay (s)	Vth (V)
1.8	1	35.60 μ	20.07 n	.72
1	1	160.20 n	20.15 n	.45
.7	.7	89.35 n	20.09 n	.32

Table 2.Observation of BD-CMOS inverter.

Vdd (V)	Vdd (V)	Vbn (V)	Vbp (V)	Power dissipation (W)	Delay (s)	Vth (V)
.8	.8	.4	0	37.9 m	20.16 n	.7
.4	.4	.4	0	55.25 n	20.32 n	.17
.4	.4	.2	0	53.86 n	20.30 n	.19
.4	.4	.4	.2	34.51 n	20.33 n	.17
.4	.4	.2	2	32.19 n	20.32 n	.17

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From the tables we can observe that the power dissipation and the supply voltage of BD-CMOS inverter becomes approximately half as comparison to conventional GD-CMOS inverter. Also the reduction in the threshold voltage (which is very critical to reduce its value) becomes approximately half. There is no much effect on the delay on the CMOS inverter using Bulk-Driven technique. If we connect the inverters in cascading then this techniques has major effect on the output of cascading CMOS inverter.

VI. SIMULATION RESULTS

The current through the NMOST and PMOST devices must be equal for valid dc operating point. Graphically, this means that the dc point must be located at the intersection of corresponding load lines.as can be observed, all operating points are located either at the high output levels or low output levels. A very narrow transition zone exhibit by the voltage transfer characteristic (VTC) of the inverter. When both NMOST and PMOST are simultaneously on and in saturation, this results from the high gain during switching transient. This shows a small change in the input voltage results in a large output variation operating in that region. The observations of all these translate into the VTC of GD-CMOS inverter and BD-CMOS inverter in fig. 5(a) and 5(b).

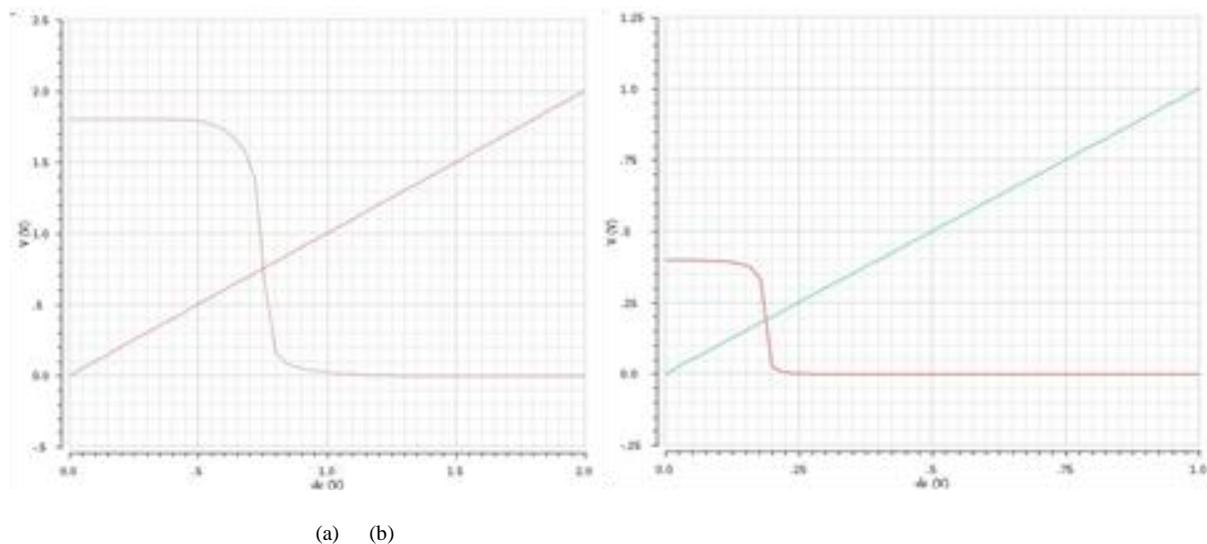
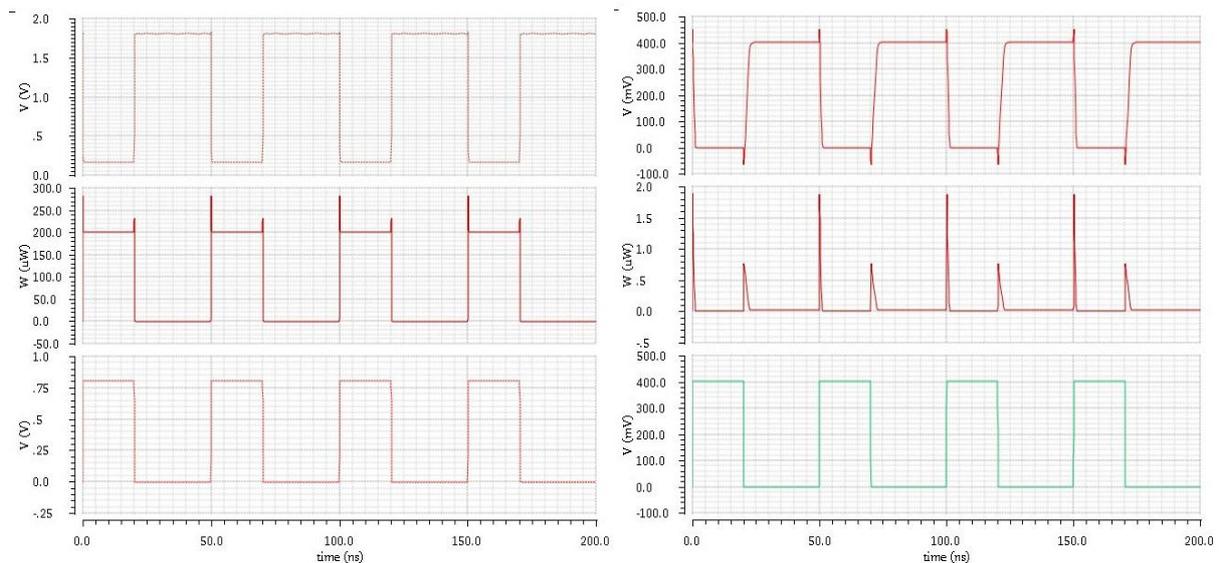


Fig. 5. VTC of: a) GD-CMOS inverter b) BD-CMOS inverter.

Transient response is dominated mainly by the output capacitance of the gate, which is composed of the drain diffusion capacitances of the NMOST and PMOST, the input capacitance of the fan-out gates and the capacitance of the connecting wires. Assuming temporarily that the transistors switch instantaneously, through this can get the idea of the transient response by using the simplified graphs (fig. 6).

Let us consider the low to high transition first. The gate response time is simply determined by the time it takes to charge the capacitor through the resistor. Similar considerations are valid for the high to low transition, which is dominated by the time constant. The on-resistance of the NMOST and PMOST transistor is not constant, but is a nonlinear function of the voltage across the transistor. This complicates the exact determination of the propagation delay.

Also from the figure 6 we can observe the very large power variation in between GD-CMOS inverter and BD-CMOS inverter i.e. GD-CMOS inverter consume more power as compare to BD-CMOS inverter. But from the transient characteristic of BD-CMOS inverter (fig. 6(b)) shows some glitches to the output. These occur glitches do not have much effect on the digital integrated circuits. So we can ignore glitches in BD-digital design.



(a)(b)

Figure 6. Transient Characteristics: a) GD-CMOS inverter b) BD-CMOS inverter.

VII. CONCLUSION

In this paper, 0.4 Bulk-Driven CMOS inverter is proposed. The design incorporates biasing the bulk of NMOST and PMOST using bulk driven technique which reduced the supply voltage, power dissipation and threshold voltage in a large variation as comparison to Gate-Driven CMOS inverter. The bulk driven digital circuits are suitable for few applications which require very low power consumption. The few applications of this ultra-low power and low supply voltage digital logic circuit is seen in biomedical devices such as pace maker, heart rate detector etc [11], self-powered devices, wrist watch computation and other different devices. Due to its reduction in transconductance, this bulk driven technique is also restricted to certain applications in which ultra-low power is mainly required.

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