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# High PSRR LDO Regulator by Varying Substrate Voltage on 90-nm CMOS Technology

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**ABSTRACT:** This paper presents a capacitor less LDO voltage regulator by varying the substrate voltage using IBM 90-nm technology which improves the performance of LDO voltage regulator by increasing the value of PSRR at high frequency and reducing the  $\Delta V_{out}$  by 76%. Smallest value of FOM is achieved which signifies better transient response. Low drop out regulator (LDO) is a regulator which provide the difference between unregulated input and regulated output voltage while driving the load to its require range and also provide the require load current. LDO is an essential part of the power management system that provides constant voltage supply with improved transient response i.e. they should be capable of responding quickly to changes in load current. Increased demands of LDO make it important part of various fields like portable devices, biomedical devices, MCUs etc. The problem encountered in some papers is of line and load regulations, high quiescent current, settling time, and load current. Generally, due to these parameters LDO suffers with low battery life. The LDO voltage regulator is used to protect the device from supply noise, so its PSRR must be high and for better transient response FOM should be low.

**KEYWORDS:** Capacitor-less LDO, low drop out voltage regulator, PSRR, FOM.

### I. INTRODUCTION

The LDO act as a variable resistor that is placed between input power source and the load in order to drop and control the voltage applied to the load. The low drop-out regulators are the essential building block of portable electronic devices such as laptops, mobile phone, biomedical implantable devices such as pacemaker, ECG, EEG and EMG etc. A series low-drop-out regulator provides a specified and stable dc voltage, whose input to output voltage difference is low. The drop-out voltage is defined as the value of the series voltage regulator. Low drop-out (LDO) regulators can be divided as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are mainly demanded by many automotive and industrial applications. Conventional LDOs are typically implemented with at least one feedback loop which is stabilized using a huge external capacitor. input/output differential voltage where the LDO stops regulating. A Power transistor (pass device) is connected in series between the input and the output terminals of the regulator that's why it termed as series voltage regulator. Low drop-out (LDO) regulators can be divided as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are mainly demanded by many automotive and industrial applications. Conventional LDOs are typically implemented with at least

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one feedback loop which is stabilized using a huge external capacitor. There are two types of LDOs based on capacitor as follows:

## 1.1) Low Drop Out Regulators with Capacitor

Reduces output noise, the output voltage variation and improves PSRR. But it also has some disadvantages that use of capacitor increases the chip area, affects the stability of LDO regulator, affects on a large load transient response, affect during shut-down, there is also low start-up issue.

## 1.2) LDO without capacitor

Present research in LDOs is focused on removing this external capacitor while maintaining stability, good transient response and high power supply rejection performance. Capacitor free low drop-out regulators have several advantages over the low drop-out regulators with capacitance on the basis of small size and portability.

## II. RELATED WORK

Lv Xiaopeng et al. (2011) presented a fully on-chip Low Drop-Out (LDO) voltage regulator with 150mA driving capability, which is implemented in 180 nm CMOS technology. This proposed LDO voltage regulator uses paralleled input differential pairs and current amplifiers to provide fast transient response, achieving 1.4 $\mu$ s settling time with transient variation less than 155mV, while consuming 90 $\mu$ A quiescent current [1]. A two stage cascoded operational transconductance amplifier is used to designed error amplifier by Herminio Martinez-Garcia et al. (2012) that achieve high DC gain and PSRR of 34.3 dB at 10 KHz [2]. Leo C. J. et al. (2013) proposed an ultra low power capacitor less low drop out voltage regulator with High PSR of -95dB at 5MHz which is integrated with medical body area network (MBAN) transceiver having drop of 300mV and implemented on 0.13  $\mu$ m CMOS IP6M process [3]. A slew rate enhancement circuit is proposed (Cheekala Lovaraju et al. (2013)) that improves the transient response and have high loop bandwidth with improvement in settling time by 61% [4]. Fan Yang et al.(2014) design LDO that enhance the transient response using active feedback and damping factor control technique which in turn use to drive 50mA load with dropout of 200mV on 65nm CMOS process [5]. Sau Siong Chong et al. (2014) proposed a capacitor-less low drop out regulator which enhance the transient response by using push pull composite power transistor with drop out of 700mV and implemented on UMC 65-nm CMOS technology. It consumes a very low quiescent current of 16.2  $\mu$ A [6]. Sreehari Rao Patri et al. (2014) presented a stable LDO voltage regulator with a novel Double Recycling Error Amplifier structure which enhance the slew rate and implemented on UMC 180-nm CMOS process [7]. Longjie Du et al. (2014) had make use of shunt feedback as a buffer stage and the LDO regulator becomes stable for all the load conditions. Author also employs a current boosting circuit to reduce the output voltage. This paper achieved a very low quiescent current with low output voltage variation [8]. Chang-Joon Park et al. (2014) introduce the concept of adaptive noise compensation scheme to improve the PSRR at high frequency. This paper also utilizes the concept of replica pass transistor [9]. Seong Jin Yun et al. (2015) presented a capacitor-less low dropout regulator for enhanced power supply rejection. The proposed scheme is implemented with 0.18  $\mu$ m CMOS technology by an additional capacitor at a gate node of a pass transistor. Simulation results show the optimum value of the capacitor gives a PSR better than -40 dB up to 5 MHz with a 50 mA load current [10]

## III PROBLEM FORMULATION AND OBJECTIVES

The problem encountered in the performance of LDO is that the low power devices such as laptop, smart phones, medical devices, micro-controller units etc. consume large load current and during working as well as sleep mode, they have been leaking large current which causes the low battery life. The objective of our paper is to increase the values of slew rate, PSR, load and line regulations and also decrease drop out voltage, quiescent current, settling time, area, and load current by using 90-nm technology.

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## IV. THE PROPOSED LDO STRUCTURE

The proposed design utilizes the concept of substrate bias effect to reduce the threshold voltage of pass transistor for any given load current. The threshold voltage  $V_{th}$  is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This is known as the substrate bias effect or body effect. The expression for the threshold voltage which is also used by [11] is:

$$|V_{th}| = |V_{th0}| + \gamma (\sqrt{|V_{SB} + 2|\phi_b|} - \sqrt{2|\phi_b|}) \quad \dots\dots\dots(1)$$

where  $V_{SB}$  is the substrate bias voltage,  $V_{th}$  is the threshold voltage of the device for  $V_{SB} \neq 0$ , and  $V_{th0}$  is the threshold voltage for  $V_{SB} = 0$ ,  $\gamma$  is the constant that describes the substrate bias effect. The term  $2|\phi_b|$  is the surface potential. It is clear from equation (1) that, if the bulk voltage in PMOS transistor is decreased then threshold voltage also decreases. For a fixed source to gate voltage, this change in the  $V_{th}$  will result in an increase in the drain source current ( $I_{DS}$ ) and vice versa. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a second gate, and is sometimes referred to as the “back gate”, (or body effect sometimes called the back gate effect). The small signal bulk transconductance of a PMOS transistor can be derived as:

$$g_{mb} = \partial I_D / \partial V_{SB} = \gamma g_m / (2[\sqrt{V_{SB} + 2|\phi_b|}]) \quad \dots\dots\dots(2)$$

where  $g_m$  is the small signal transconductance of the device.

In this design we have chosen the device geometry of  $(W/L) = (70 \text{ um}/90 \text{ nm})$  when its source is connected to 1 V and substrate is connected to 500 mV (or  $V_{bulk} = 500 \text{ mV}$ ), or equivalently  $V_{SB} = 500 \text{ mV}$ .

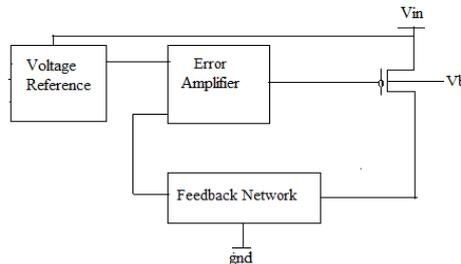


Fig. 1 Block diagram of proposed LDO voltage regulator

In this figure, the substrate of the pass transistor is connected to the voltage source of 0.5V and gate of the pass transistor is connected to the output of the error amplifier. Therefore, the error amplifier will provide the high DC gain for accurate regulation. Error amplifier is just an operational amplifier which is made up of folded cascade type because this amplifier provides high slew rate and power supply rejection ratio. It also solves the problem of limited bandwidth of conventional LDO.

## V. EXPERIMENTAL RESULTS

The proposed LDO regulator is simulated in the IBM 90-nm CMOS technology using Tanner Toll. The input, output and reference voltages are 1V, 0.9V and 0.5V respectively.

### A. Power supply rejection characteristics

Figure2 shows the PSRR response of proposed LDO regulator for 50 mA of load current and 100fF of load capacitor

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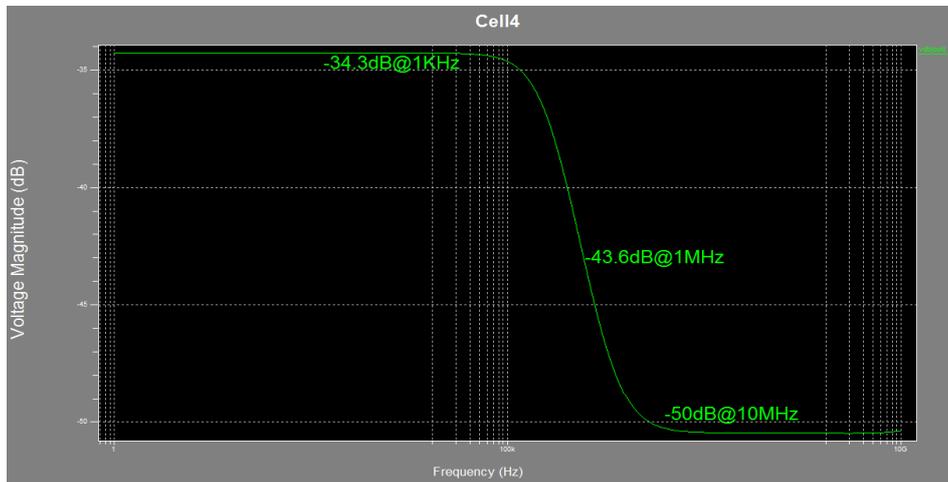


Fig. 2. PSRR response of proposed LDO regulator

The simulated result illustrates that the PSRR of LDO is around -34.3 dB at 1KHz, -43.6 dB at 1MHz, and -50 dB at 10MHz frequency.

## B. Static-state regulation characteristics

### • Line regulation

The output voltage of the proposed LDO voltage regulator with the input voltage swept from 1.3 V to 2.1V is given in figure 3.

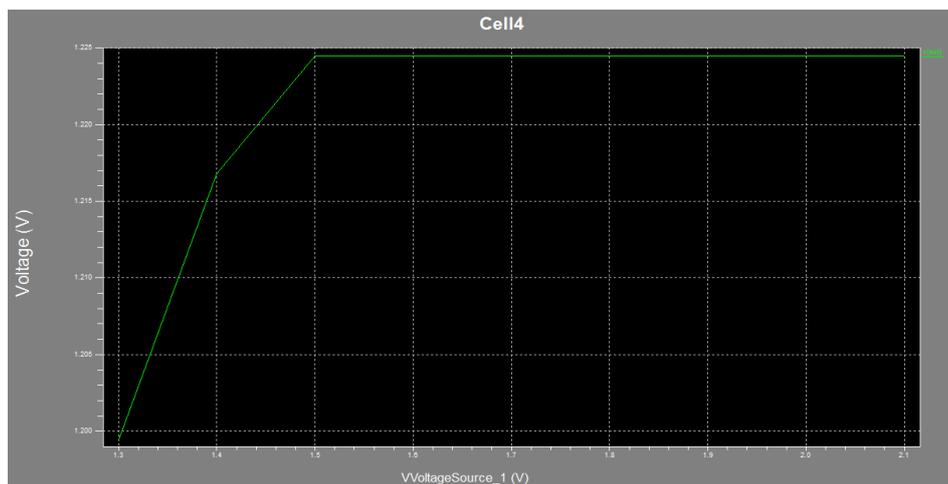


Fig. 3. Line Regulation

The simulation result illustrates that the output voltage variation is 25mV when the input voltage changes from 1.5V to 2.1V with the drop-out voltage higher than 900mV, resulting in the line regulation of 41 mV/V.

### • Load regulation

The output voltage of the proposed LDO voltage regulator with the load current swept from 0 to 1 mA is given in figure 4.

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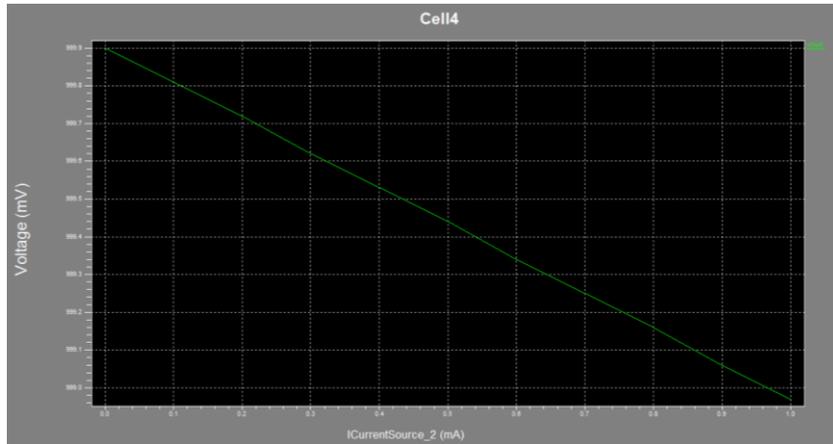
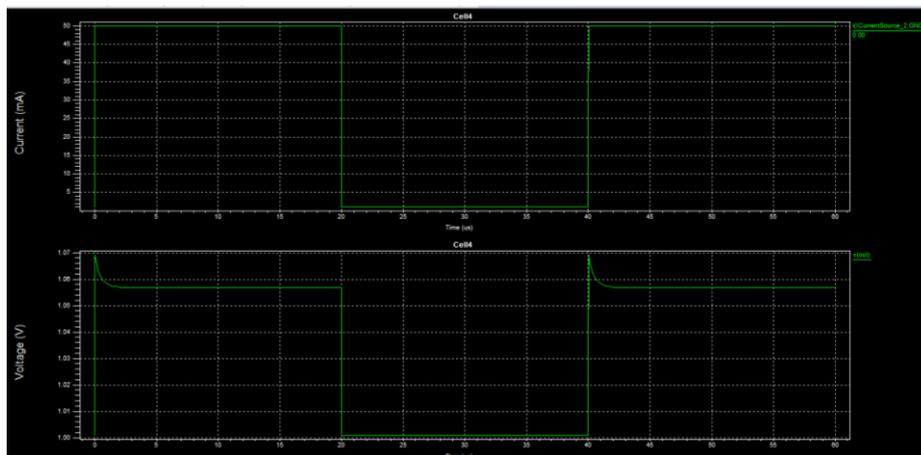


Fig. 4. Load Regulation

The simulation result illustrates that the output voltage variation is  $933\mu\text{V}$  with the load current changing from 0 to 1 mA, resulting in the load regulation of  $933\mu\text{V}/\text{mA}$ .

### C. Dynamic-state regulation characteristics

The load transient response of the proposed LDO voltage regulator with 100fF on-chip output capacitor is given by figure 5. Figure 5(a) shows the input waveform, figure 5(b) shows the output waveform for rising edge, figure 5(c) shows the output waveform for falling edge. The load current varies between 1mA and 50mA with rising and falling time of  $1\mu\text{s}$ .

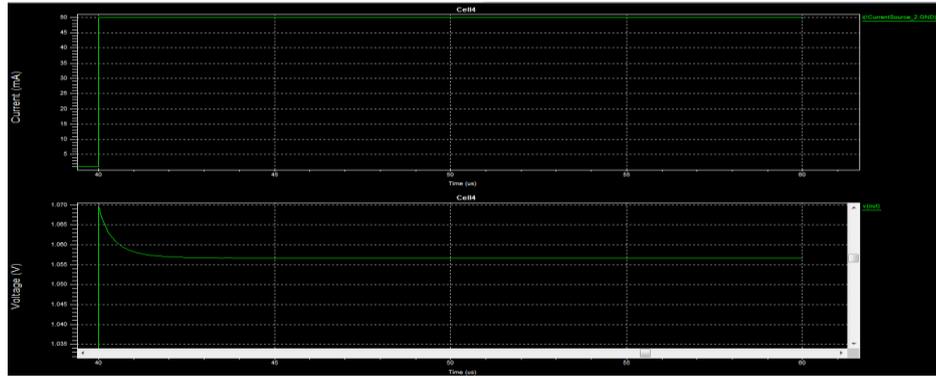


(a)

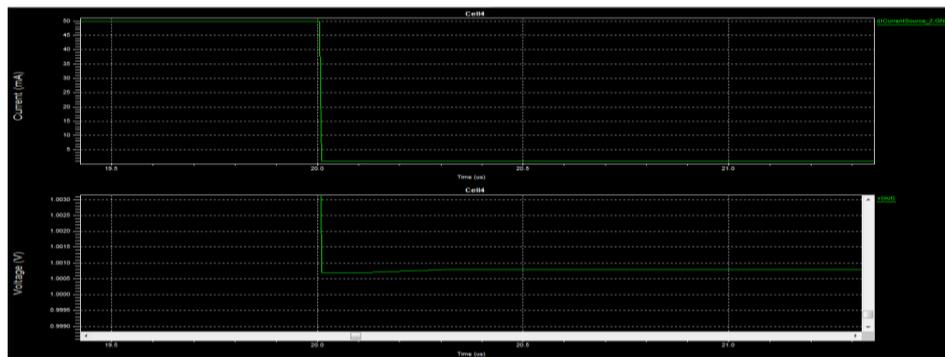
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(b)



(c)

Fig. 5. Load transient response

The simulation results illustrate that the output voltage variation is 11.98mV, 87uV respectively, with settling time of 1.77μs, 0.285us.

## D. Quiescent Current

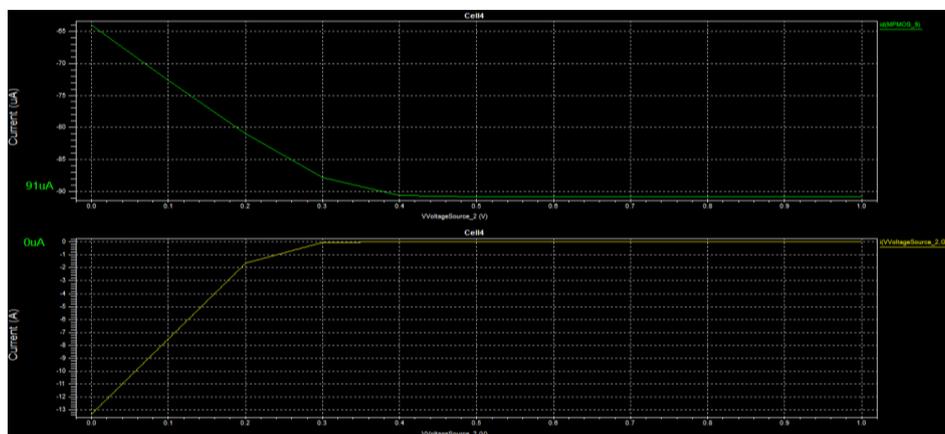


Fig. 6. Quiescent Current

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Fig. 6 presents the quiescent current  $I_Q$  against the output current. Simulated result illustrate that the LDO regulator consumes 91  $\mu A$  current.

### E. Summarized characteristics and comparisons

The characteristics of the proposed LDO voltage regulator is summarized in Table 1, and compared with references [1], [5], [6], [10] and [11].

**Table1. Comparison of the proposed LDO regulator with other LDOs**

Parameters	[1]	[5]	[6]	[10]	[11]	This work
<b>Year</b>	<b>2011</b>	<b>2014</b>	<b>2014</b>	<b>2015</b>	<b>2014</b>	2015
<b>Technology</b>	180nm	65 nm	65 nm	180 nm	130 nm	IBM 90 nm
<b>I<sub>load(max)</sub></b>	150 mA	50 mA	50 mA	50 mA	5 mA	50 mA
<b>I<sub>load(min)</sub></b>	-	0.01 mA	0	-		5mA
<b>V<sub>in(min)</sub></b>	3.3 V	1 V	.75-1.2V	1.8 V	1.2 V	1 V
<b>V<sub>out(max)</sub></b>	1.8 V	-	0.5V	1.6 V	1 V	0.9V
<b>V<sub>drop</sub></b>	1.5V	-	0.7V	0.2 V	0.2 V	0.1V
<b>Load Capacitor(C<sub>L</sub>)</b>	-	-	0-100 pF	20 pF		.1pF,1pF, 7pF
<b>Quiescent Current (I<sub>Q</sub>)</b>	90 $\mu A$	27.5 $\mu A$	16.2 $\mu A$	80 $\mu A$	99.04 $\mu A$	90 $\mu A$
<b><math>\Delta V_{out}</math></b>	155 mV	17.5 or 11 mV	103 mV	103 mV	50 mV	<12mV
<b><math>\Delta I_{load}</math></b>	-	-	50 mA	-		45mA
<b>Settling time</b>	1.4 $\mu s$	-	1.2 $\mu s$	-	0.16 $\mu s$	1.77 $\mu s$ /.28 $\mu s$
<b>Line Regulation</b>	13.75 $\mu V/mV$	4 mV/V	-	-		41mV/V
<b>Load Regulation</b>	51 $\mu V/mA$	0.028 mV/mA	-	-		933 $\mu V/mA$

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<b>PSR (dB)</b>	<b>@ 1 KHz</b>	-	-46 dB	-46 dB	-	-93.6 dB	-34.3 dB
	<b>@ 1 MHz</b>	-10 dB	-35 dB	-4 dB	-52 dB	-57.11 dB	-43.6 dB
	<b>@ 10 MHz</b>	-	-	-	-29 dB	-41.15 dB	-50 dB
<b>Edge Time</b>		-	200 ns	100 ns	-		5 ns
<b>FOM</b>		-	12.1 fs	33.4 mV	0.000066 ns		43.2 as

From above table we have analysed that bulk voltage of 500mV is good choice to obtain the high PSRR at 90-nm technology and at variable load capacitor and load current.

### VI. CONCLUSION

A low drop out voltage regulator has been designed on 90 nm and simulated in Tanner EDA software. To improve the performance of LDO voltage regulator, threshold voltage of pass transistor has been modulated by varying substrate voltage of 200 mV, which regulates the output voltage at 0.9 V from 1 V supply with minimum drop-out voltage of 100 mV and delivering maximum output current of 50 mA. The use of this technique allows us to achieve high PSRR, which has found out to be 50 dB at 10 MHz and low FOM of 43.2 as. Within the scope of power management system low quiescent current consumption is required which is 90  $\mu$ A and  $\Delta V_{out}$  is less than 12 mV.

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