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# **Design of Non-Volatile Memory Based On Improved Writing Circuit STT-MRAM Technique**

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**ABSTRACT:** Spin-transfer torque magnetic RAM (STT-MRAM) is a one of the memory application for next generation. It has many attractive features like high density and low leakage. However, it comes with high write power due to large current required to achieve fast switching speed. The STT-MRAM target mainly to replace SRAM or DRAM. It is used as a working memory in the cache, high access speed is one of the most critical performance. The objective of our project is to contribute one such storage device by making NVM based on Spin Transfer Torque Magnetic Random Access Memory (STT-MRAM). STT-MRAM based on resistive switching mechanism. In this proposed work we are reducing power and area. The NVM circuit has been implemented using Tanner Tools using 220nm technology and the responses are obtained. In this paper achieve the low power and sensing the each bit for reading.

**KEYWORDS:** MRAM, CMOS, Resistive Switching, Magnetic Tunnel Junction, Writing/Reading Circuit

## **I. INTRODUCTION**

Memory system is the heart of the processor. On-chip memory occupies a more portion of the over-all processor in a system. The last few years, advance improvements in memory density; this has also resulted in an increase of power dissipations, Energy for data transfer and read/write delay [2].

Volatile memory to non-volatile memory, is computer memory that requires power to maintain the stored information; it retains its contents while powered, but when power is interrupted stored data is immediately lost. Volatile memory has several uses, as a RAM drive. Non-volatile memory is typically used for the task of secondary storage, or long-term persistent storage. However, most forms of non-volatile memory have limitations that make them unsuitable for use as primary storage. Non-volatile memory costs are more. The memory is efficiently used for the processor. Computational complexity of memory usage becomes an important problem for all devices [8].

The development of new generation non-volatile memories, such as Phase Change Memories (PCMs) and Resistive-RAMs, calls for accurate and controllable programming pulses, which are fundamental to adequately characterize the memory cell [3]. Magnetic tunnel junction based logic has a great potential of the non-volatility, unlimited endurance, CMOS compatibility, and fast switching speed of the MTJ devices. MRAM cells integrate a magnetic tunnel junction (MTJ) consisting of a thin insulating barrier (i.e.,MgO) separating two ferromagnetic (FM) layers. SPIN-TRANSFER TORQUE (STT) magnetic tunnel junction (STT-MTJ) technology combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability, fast read/write [1],[3].

The RS-NVMs are derived from different physics, they hold many common features. For instance, they are two-terminal nanoscale devices and their resistances vary to present '0' and '1' NV states. Benefiting from these features, a number of innovative hybrid RS-NVM/CMOS circuit have been designed in the last few years such as NV look-up table (NV-LUT), NV Flip-Flop (NVFF) and NV Full Adder (NVFA). They show interesting performance in terms of power, area and speed. However there is no general design rule so far for these hybrid circuits and it is difficult to extend them for all types of RS-NVMs [2].

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In this paper presents a design of MRAM using STT-MRAM technique to improve writing/reading speed and sensing the data for the operation. Spin Transfer Torque Magnetic RAM (STT-MRAM) promises low power, great miniaturization prospective and easy integration with CMOS process.

## II. SYSTEM ARCHITECTURE

The MRAM design includes magnetic flip flop design, precharge sensing amplifier and writing/reading circuit. Fig 1.shows the block diagram of MRAM design.

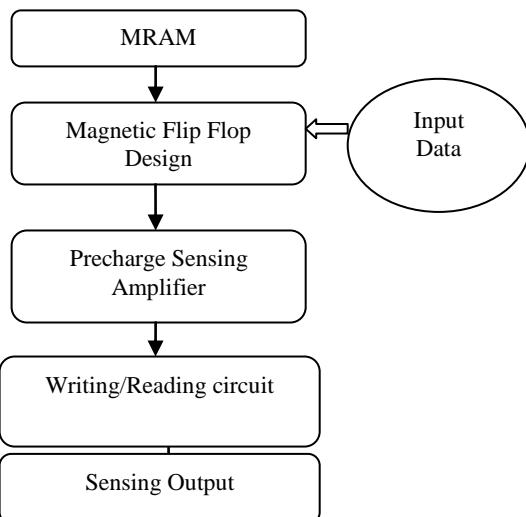


Fig. 1 Block diagram of MRAM design

### A. Magnetic Random Access Memory

Unlike conventional RAM chip technologies, data in MRAM is not stored as electric charge or current flows, but by magnetic storage elements. The elements are formed from two ferromagnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. One of the two plates is a permanent magnet set to a particular polarity; the other plate's field can be changed to match that of an external field to store memory. This configuration is known as a spin valve and is the simplest structure for an MRAM bit [5].

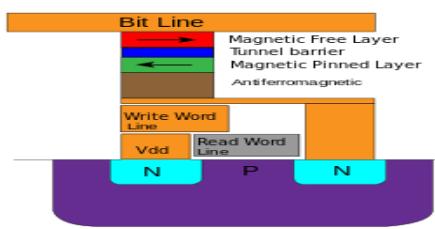


Fig. 2 Simplified structure of MRAM cell

In this structure have three layer free layer, fixed layer and tunnel barrier. The fixed layer is a permanent magnet and the free layer is magnetic effect at the current given time. The potential arrangements include "Thermal Assisted Switching" (TAS-MRAM), which briefly heats up (reminiscent of phase-change memory) the magnetic tunnel junctions during the write process and keeps the MTJs stable at a colder temperature the rest of the time; and "vertical

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transport MRAM" (VMRAM), which uses current through a vertical column to change magnetic orientation, a geometric arrangement that reduces the write disturb problem and so can be used at higher density [20].

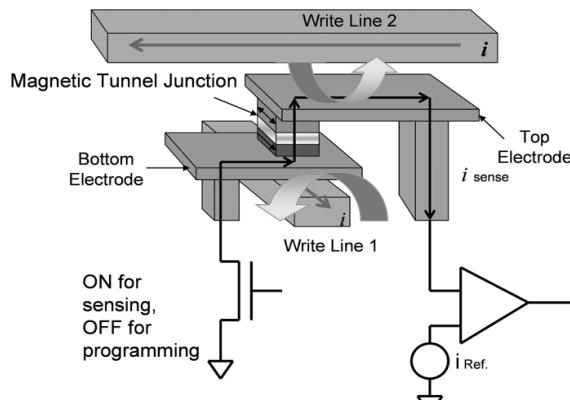


Fig. 3 MRAM cell structure, showing the sense path

The MRAM is composed of a thin oxide pass transistor, a single MTJ, top and bottom sense electrodes, and two orthogonal program lines, as shown in Fig. 3. A connection is made from the base contact of the bit to ground through a via stack connected to an isolation transistor in the underlying CMOS. Flowing current through the program conductors produces the magnetic fields necessary to switch the state of the bit. In this architecture, the program lines are physically separated from the MTJ, which reduces the parasitic delay.

The MTJ is composed of a pinned magnetic layer, a tunnel barrier, and a free magnetic layer. Electrons spin polarized by the magnetic layers traverse the tunnel barrier. A parallel alignment of the free layer with respect to the pinned layer results in a low resistance state, while an antiparallel alignment results in a high resistance state. The sense circuitry is composed of a thin oxide pass transistor, which is electrically connected to the MTJ by the bottom and top electrode conductors. In order to read the bit, the isolation transistor is turned on, and a small current of about 10 A (depending on the resistance of the material, size of the bit, and desired bias condition) is passed through the bit to sense the resistance. The MRAM module is inserted late in the CMOS process flow, making the MRAM module and the CMOS independent from one another [6].

### B. Magnetic Flip Flop Design

Magnetic flip-flop (MFF) design libraries has been developed using a unique MRAM process. This is comparable to that of a normal CMOS DFF. An MFF test chip was fabricated with the process. Which helps to reduce the power dissipation .Which performs; possible magnetic data store and restore operations. Non-volatile (of computer memory) having the property of retaining data when electrical power fails or is turned off. A flip-flop or latch is a circuit that has two stable states and can be used to store state information [4].

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal [10].

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered). Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called latches [11].

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## C. Precharge Sensing Amplifier

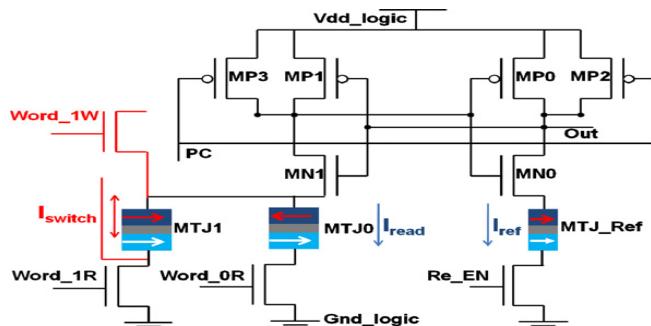


Fig. 4 Pre-Charge Sense Amplifier for STT-RAM

The PCSA for spin transfer torque random access memory which allows lower the current and shorting the delay. These circuits consist of two sub circuit one is precharge sub-circuit and another one is discharge sub-circuit. It operates at two phases; first apply input 0 PMOS transistor is ON to get a output for sensing data. And then apply input 1 the NMOS transistor is ON to get a sensing output. The pair of inverters acts like a amplifier. Using the resistance at the circuit it sensing the data at lower state and higher state. The resistance is higher state it sense the data to through the output [16].

A sensing amplifier is an amplifier that senses the output on the bit lines and amplifies it. The sense amplifier that is used in the design of sensing the write/reading data completely. This approach presents numerous advantages over it single ended counterpart. One of the advantage is the common mode rejection. It means that such an amplifier rejects noise that is equally injected in both inputs [2].

## D. Writing/Reading Circuit

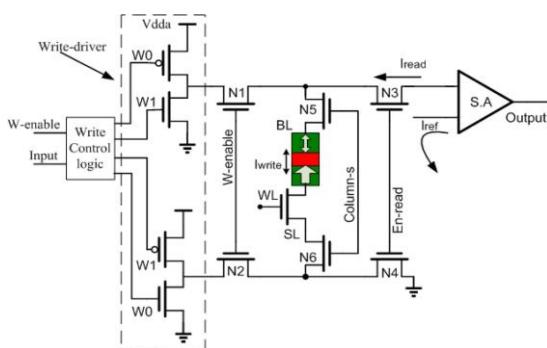


Fig. 5 Writing circuit

The conventional STT writing circuit is shown in Fig. 5. The W-enable signal controls the writing current to flow through the MTJ or not. Transistors (N1–N4) controlled by W-enable and En-read signals are used to avoid the interference between write/sense currents. Transistors (N5 and N6) controlled by column-s are used to select one column. The Write value depends deeply on both the transistor resistance and the supply voltage of the writing branch. All the column selected transistors and other transistors controlled by W-enable are in the writing branch, which make total resistance high. With (4) and (5), one low Write needs long switching time to ensure the desired data to be stored correctly, which lower the write speed of STT-MRAM. Using higher write current is a possible solution. To generate a high write current, it is necessary to decrease the resistance and increase the supply voltage value of writing branch. Therefore, the column selected logic composed of parallel connection of pMOS and nMOS with bigger size is used to

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obtain smaller resistance, and one high supply voltage in writing branch is used to generate a higher current, where  $V_{dd}$  is higher than the logic voltage  $V_{dd}$ . The calculated switching energy of one switching operation is up to 36 pJ/bit, which makes the writing power consumption high.

In the reading branch, there are also column selected transistors (N3 and N4). As these transistors are used to select one column, their size can be small, which makes total resistance large and reading current low. According to (1)–(3), this low reading current can reduce significantly the read disturbance probability [20]. The added logic increases the number of transistors in the proposed circuit. However, the total area is not larger than that of the conventional circuit, as the transistor size in the conventional circuit is larger to obtain small resistance in the writing circuit.

The sensing operation suffers from high sensitivity to process voltage temperature variations. Although the writing circuit with low supply voltage could further decrease power and area consumption, the Monte Carlo statistical analysis of sensing output is worse due to the high resistance in sensing circuit. To improve the reliability of reading circuit, we propose another novel circuit, shows Fig as shown in Fig. 6.

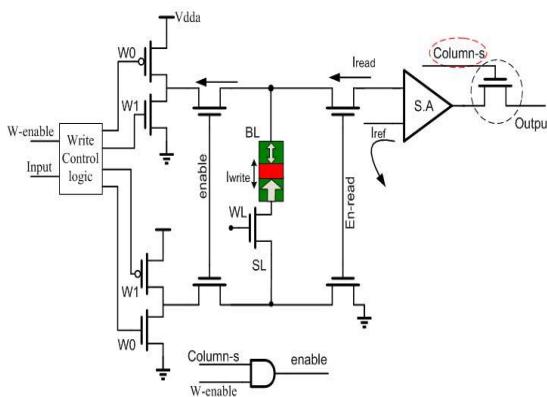


Fig. 6 Reading circuit

The column selected transistor is shifted to the post of SA, and the output of SA is outputted by the column selected transistor. The reduction of transistor number in sensing circuit decreases the sensitivity to process variations. Unfortunately, each column of cell array needs one SA, which results in area overhead. For the 16 kb STT-MRAM with 256 rows and 64 columns array, the area overhead is  $\sim 33 \mu\text{m}^2$ , which is 10% of the storage array. This area overhead can be negligible because the sensing circuit is often widely shared by many elements of memory array.

### III. PROPOSED IMPROVED ENABLE WRITING CIRCUIT USING STT-MRAM TECHNIQUE

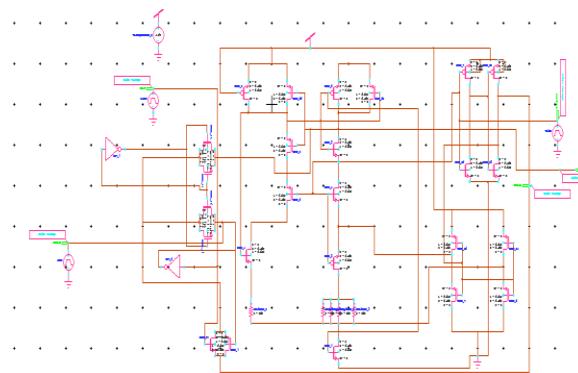


Fig. 7 Proposed MRAM circuit using STT-MRAM

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The above figure consists of RSM, Sensing amplifier, Read and write circuit. RSM act as a port at input and output. Sensing amplifier is used to sense the read and write signal also sense switching activities of turn on and off. The circuit is active write the data into the memory. And then reading circuit is activated to read the given data. In this proposed circuit see the reading operation when the system powered off.

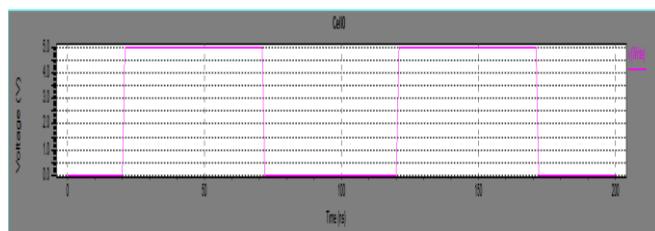


Fig. 8 Write signal output

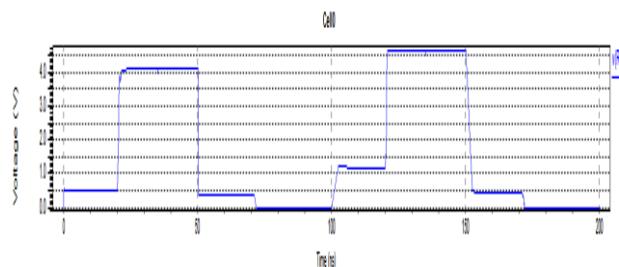


Fig. 9 Reading Signal

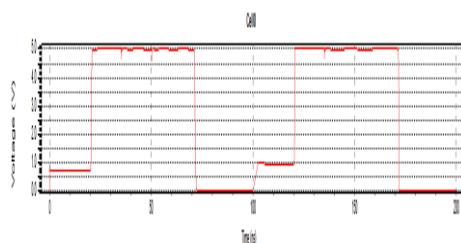


Fig. 10 Sensing output

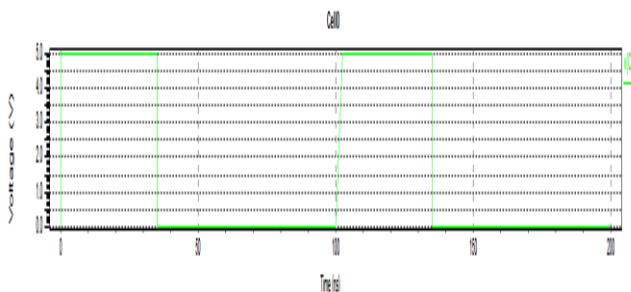


Fig. 11 Clock signal

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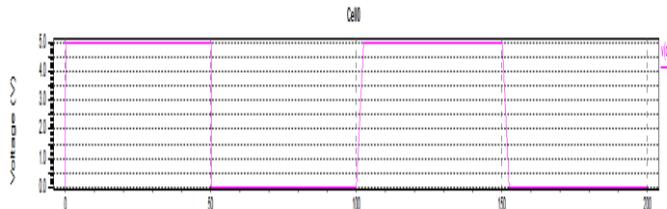


Fig. 12 Input Data

The above graphs are obtained from the simulation of the NVM cell STT-MRAM realization. The input 1010 given to the circuit as shown in fig 12. Give the clock signal to activate the circuit for read and write as shown in fig 11. Activate write circuit to sense the input to write the data as shown in fig 10. And then read the data as shown in fig 9. Fig 8 is the sensing output. It uses to sense the read signal. When power off the system a sensing circuit sense the read signal to continue read the data.

## V. CONCLUSION

In this paper, design of STT-MRAM based on Spin transfer torque and Magnetic flip-flop is proposed in our work with CMOS technology. In the e design that was based on self-gating power gate mechanism, our proposed design provides promising result than existing system. Our work concentrated on reduction of power and reduced delay, and also area efficiency, thus from the overall parameters we have achieved better performance than the existing design of Flip-flop. For this design held in CMOS design methodology and we have used Tanner EDA 15.11 as simulation tool to show the performance analysis.

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