

A High Step up Transformerless Single-Stage Single-Switch AC/DC Converter Using SEPIC

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ABSTRACT: This paper presents a high step-up transformerless ac/dc converter for universal line applications nearly 400v. The topology integrates a step up converter used for power factor correction with a boost converter and part of the input power is coupled to the output directly. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion with power factor correction and the voltage is boosted nearly up to 400v. The absence of transformer reduces the magnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts. Unlike most of the other converter, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents.

KEYWORDS: Single Ended Primary Inductor Converter (SEPIC), Power Factor Correction (PFC), Transformerless.

I. INTRODUCTION

Efficient AC-DC power conversion has been of much interest in recent years with the wide increase in electronic devices which demand clean DC power supplies. Today's industries aim to provide AC-DC adapters with very small form factors for portable applications. The improvement in device technology has led to efficient and high power density devices. This has created tremendous improvement in AC-DC converter size and efficiency. Power factor correction (PFC) stage followed by a DC-DC stage. A two stage approach mostly uses a boost PFC circuit for the first stage. This is because of the good PFC capability and high efficiency provided by this circuit. The consequence of using it in the first stage is the high voltage output which requires a capacitor with high voltage rating resulting in increased size and cost.

Recently many single stage converter architectures have been reported. The single stage architectures combine the PFC and-DC stage into a single stage reducing the control complexity. The PFC correction can also be done and is called bridgeless PFC. This circuit combines the operation of the bridge rectifier with the DC-DC converter into a single circuit. The aim is to reduce the number of components and the size of components to obtain an energy efficient power supply design. This thesis briefly reviews some of these architectures that can satisfy the requirements of the standards and provides a comprehensive review of the pros and cons of each. It also provides a feasibility study of one of the transformerless architecture to achieve a small size power converter for portable applications. The recent architectures in AC-DC conversion and provides a comparison, pointing to the important issues in power supply design that these architectures are aiming to solve.

The advantage of this topology is that it uses single switch for power factor correction and voltage regulation. In order to reduce the switching loss in normal working condition, a soft switching technique is implemented. Under light load condition, this problem is solved by using a SEPIC converter for the PFC stage of the single-stage single-switch converters as it can be completely turned off by operating the converter only near the zero crossing of the input voltage, due to the presence of the dead angle of input current. Thus, this project reviews various recent transformerless

architectures. A prototype of a non-isolated transformerless AC-DC converter was demonstrated that indicates the feasibility of designing an AC-DC converter with small form factor and good efficiency.

II. PROPOSED CIRCUIT AND ITS PRINCIPLE

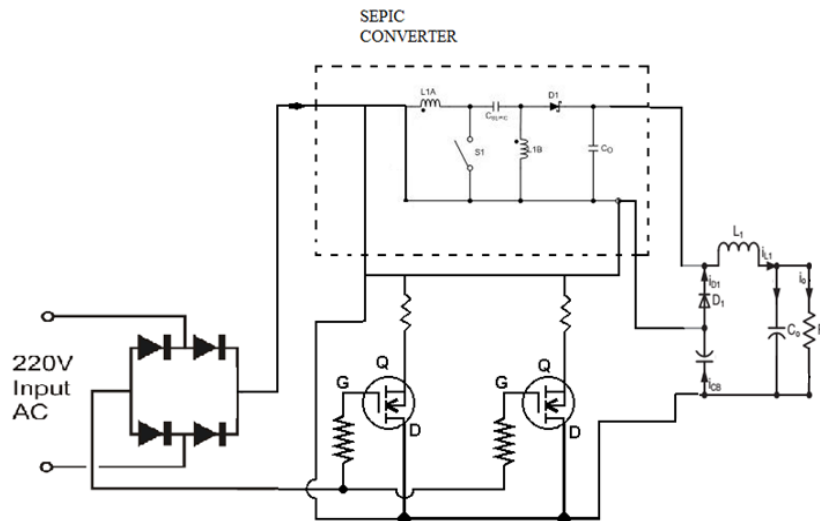


Fig.1. Proposed Circuit Diagram with use of SEPIC

The proposed circuit diagram for step up the output voltage with the help of SEPIC is shown in fig.1. It describes that the converted DC voltage is boosted by means of SEPIC around 400v. It is proven through the simulation result.

Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential at its output to be greater than, less than, or equal to that at its input; the output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC is similar to a traditional buck-boost converter, but has advantages of having non-inverted output (the output has the same voltage polarity as the input), using a series capacitor to couple energy from the input to the output (and thus can respond more gracefully to a short-circuit output), and being capable of true shutdown: when the switch is turned off, its output drops to 0 V, following a fairly hefty transient dump of charge.

A. Coupled Inductor SEPIC

The SEPIC with a coupled inductor is shown in fig. 2. When the FET (Q_1) turns on, the input voltage is applied across the primary winding. Since the winding ratio is 1:1, the secondary winding is also imposed with a voltage equal to the input voltage; but, because of the polarity of the windings, the anode of the rectifier (D_1) is pulled negative and reverse-biased.

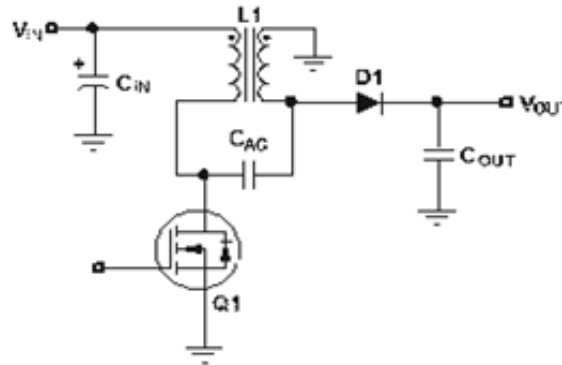


Fig.2. Coupled Inductor SEPIC

With the rectifier biased off, the output capacitor is required to support the load during this ON time, which forces the AC capacitor (C_{AC}) to be charged to the input voltage. While Q_1 is on, current flow in both windings is through Q_1 to ground, with the secondary current flowing through the AC capacitor. The total FET current during the ON time is the sum of the input current and the output secondary current. When the FET turns off, the voltage on the windings reverses polarity to maintain current flow. The secondary winding voltage is now clamped to the output voltage when the rectifier conducts to supply current to the output. Through transformer action, this clamps the output voltage across the primary winding. The voltage on the drain of the FET is clamped to the input voltage plus the output voltage. Current flow during the FET off time for both windings is through D_1 to the output, with the primary current flowing through the AC capacitor.

B. Balancing Volt-Microseconds

The circuit operates similarly when the coupled inductor is replaced with two uncoupled inductors. For the circuit to operate properly, volt-microsecond balance must be maintained across each magnetic core. That is, for the two uncoupled inductors, the products of each inductor's voltage and time must be equal in magnitude and opposite in polarity during the FET ON and OFF times. It can be algebraically shown that the AC capacitor voltage for uncoupled inductors is also charged to the input voltage. See the Appendix for details. The output-side inductor is clamped to the output voltage during the FET OFF time, as was the secondary winding of the coupled inductor. During the FET ON time, the AC capacitor imposes a potential equal to the input voltage but opposite in polarity across the inductor. With defined voltages clamped across the inductor for each interval, balancing the volt-microseconds determines the duty cycle (D) is defined in equation (1).

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad (1)$$

This is simply for continuous-conduction-mode (CCM) operation. The voltage imposed across the input-side inductor is equal to the input voltage when the FET is on. When the FET is off, volt-microsecond balance is maintained by clamping V_{OUT} across it. It is easy to remember that when the FET is on, the input voltage is applied across both inductors; and when the FET is off, the output voltage is imposed across both. The voltage and current waveforms of the two uncoupled-inductor SEPICs are quite similar to those of the coupled-inductor version, so much so that it would be difficult to tell them apart.

III. CIRCUIT CHARACTERISTICS

Static gain is a measure of the ability of a circuit to increase the power from the input to the output. It is usually defined as the ratio of the input of a system. At the steady state for the inductor L_1 , the relation presented in equation(2) & (3) occurs:

$$V_i (t_{on} + t_{off}) = V_{CM} t_{off} \quad (2)$$

$$V_i D = (V_{CM} - V_i) (1 - D) \quad (3)$$

Therefore, the C_M capacitor voltage is defined in equation (4), which is the same equation of the classical boost static gain given by,

$$V_{CM} / V_i = 1 / (1 - D) \quad (4)$$

During the period where the power switch is turned-off (t_{off}), the diodes D_M and D_O are in conduction state and the following relation can be defined in equations (5) & (6):

$$V_O = V_{CS} + V_{CM} \quad (5)$$

$$V_{CS} = V_O - V_{CM} \quad (6)$$

The L_2 average voltage is zero at the steady state, and the following relations can be considered.

$$(V_{CM} - V_{CS}) t_{on} = (V_O - V_{CM}) t_{off} \quad (7)$$

$$(V_{CM} - V_{CS}) D = (V_O - V_{CM}) (1 - D) \quad (8)$$

From equations (4), (6) and (7) the static gain of the proposed converter is obtained and presented in equation (9).

$$V_O / V_i = (1 + D) / (1 - D) \quad (9)$$

The voltage of the series capacitor V_{CS} is defined by substituting (4) and (9) in (8) resulting the following equation.

$$V_{CS} / V_i = D / (1 - D) \quad (10)$$

For a basic SEPIC converter the static gain is given by as follows which is equal to the same as the equation (10) because the output voltage is equal to the capacitor C_C voltage. Thus the static gain of the basic SEPIC converter is given by,

$$V_O / V_i = D / (1 - D) \quad (11)$$

The operation with a higher static gain results in an improvement in the operation with the lower input voltage.

IV. EXPERIMENTAL RESULTS

The circuit diagram in fig.1 results the output waveform of voltage and current shown in fig.3 and fig.4.

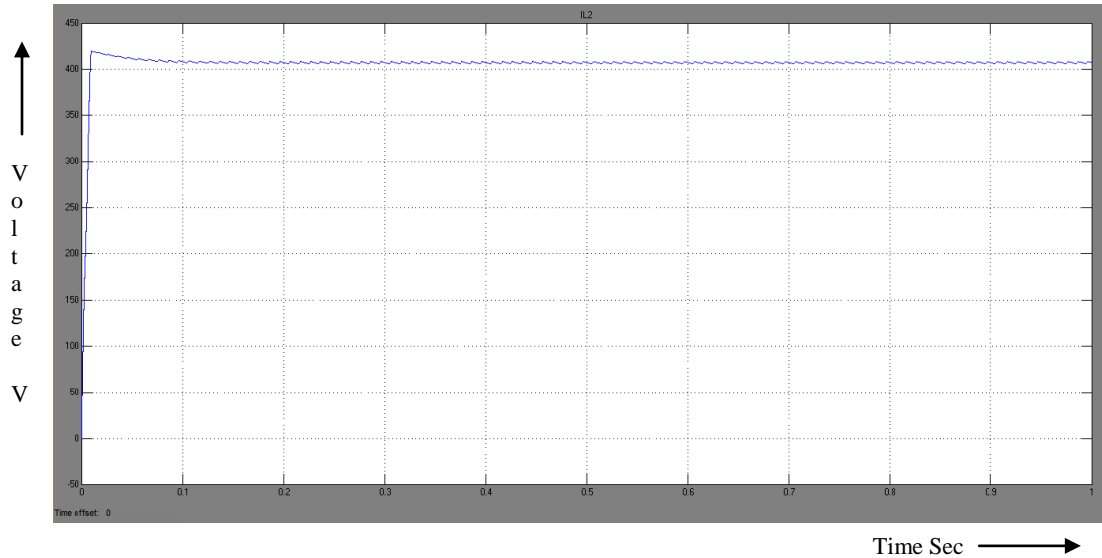


Fig.3. Output Voltage Waveform

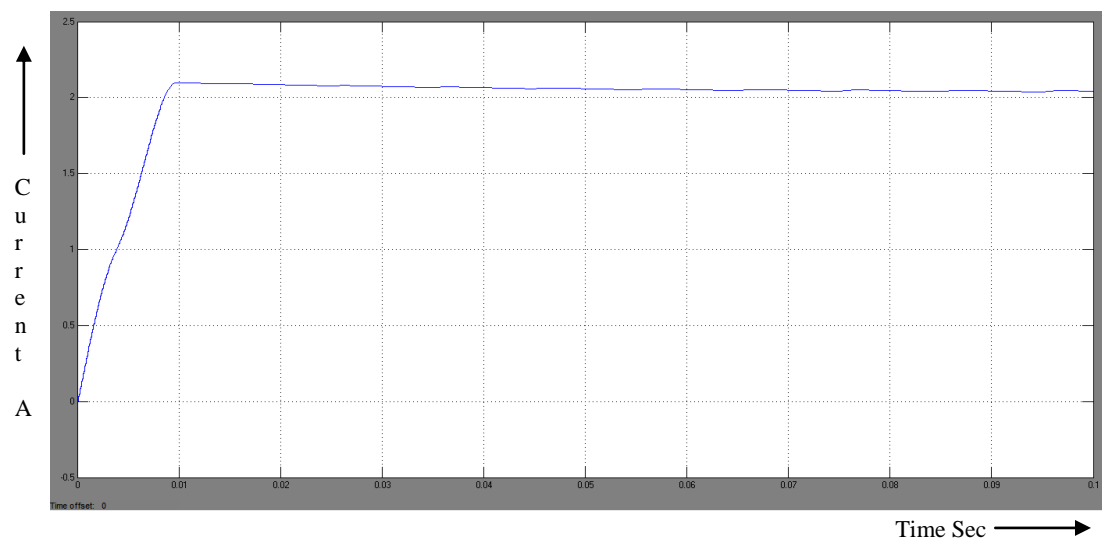


Fig.4. Output Current Waveform

V. CONCLUSION

In this project, the SEPIC single-stage ac/dc converter performance has been studied. The results have shown good agreements with the predicted values. The topology is able to obtain high output voltage without high step-up transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance and the cost of the proposed circuit are reduced compared with the isolated counterparts.

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REFERENCES

- [1] Antonio L. and Andrs B, 'New power factor correction AC-DC converter with reduced storage capacitor voltage', IEEE Trans. Ind. Electron, vol. 54, no. 1, pp. 384–397, Feb. 2007.
- [2] Cheung M.K.H. and Chow M.H.L, 'Practical design and evaluation of a 1kW PFC power supply based on reduced redundant power processing principle', IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 665–673, 2008.
- [3] Dylan Dah-Chuan Lu and Herbert Ho-Ching Iu , 'A Single-Stage AC/DC Converter With High Power Factor, Regulated Bus Voltage, and Output Voltage', IEEE Trans. Power Electron, vol. 23, no. 1, pp. 218–228, Jan. 2008.
- [4] Li H.Y. and Chen H.C. , 'Dynamic modelling and controller design for a single-stage single-switch parallel boost-flyback–flyback converter', IEEE Trans. Power Electron., vol. 27, no. 2, pp. 816–827, Feb. 2012.
- [5] Lu D.D.C. and Pjevalica V. , 'Single-Stage AC/DC Boost Forward converter with high power factor and regulated bus and output voltages', IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2128–2132, Jun. 2009.
- [6] Saisundar. S, Zhou Jun, Krishna Mainali, Simon Ng Sheung Yan and Eran Ofek, 'Transformerless AC-DC Converter', World Academy of Science, Engineering and Technology vol. 6, Sep. 2012.
- [7] Shiguo Luo, Weihong Qiu, Wenkai Wu and Issa Batarseh, 'Flyboost power factor correction cell and a new family of single-stage AC/DC converters', IEEE Trans. Power Electron, pp. 25-34, vol. 20, no. 1, Jan. 2005.
- [8] Shu-Kong Ki and Dylan Dah-Chuan Lu, 'Implementation of an Efficient Transformerless Single-Stage Single-Switch AC/DC Converter', IEEE Trans. Ind. Electron, vol.57, no. 12, pp. 4095-4105, Dec. 2010.
- [9] Shu-Kong Ki and Dylan Dah-Chuan Lu, 'A High Step-Down Transformerless Single-Stage Single-Switch AC/DC Converter', IEEE Trans. Power Electron., vol. 28, no. 1, pp. 36-45, Jan. 2013.
- [10] Zhao Q. and Lee F.C. , 'Voltage and current stress reduction in single-stage power-factor correction AC/DC converters with bulk capacitor voltage feedback', IEEE Trans. Power Electron, vol. 17, no. 4, pp. 477–484, Jul. 2010.