

**International Journal of Innovative Research in Science,
Engineering and Technology**

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

Implementation of ZCS-ZVS Buck Converter Using in Voltage Mode Control with Coupled Inductor

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ABSTRACT: Our new technology has been developed and implement with converters application. Soft switching can be used to reduce the size and weight of the converters. In most soft switching converters efficiency can be improved greatly under heavy load conditions, but the effects are poor under light load conditions due to additional power dissipations of auxiliary circuit branches. Therefore a novel topology for a buck converter, which works under soft switching conditions, is proposed . The main MOSFET switch can operate under a ZCS (zero current switching) condition at turn on and a ZVS (zero voltage switching) condition at turn off. High efficiency can be obtained under light loads. The analytical model for the switching intervals has been validated with the simulation results using MATLAB simulation tool.

KEYWORDS: Buck Converter, Coupled Inductor, ZVS,ZCS.

I. INTRODUCTION

The new rapid technological changes lead to the application of buck converters in various areas like aerospace, consumer electronics, appliances and general industries. Nowadays industries demand for small size, light weight and highly reliable dc-dc converters. Switching frequency can be used to reduce sizes and weights of converters.

There are many methods to realize soft switching, and the most common is using additional quasi-resonant circuits. It is not beneficial to select the proper rank of power switches, because there are more conduction losses when using higher voltage power switches.

Adopting interleaved structures is also a method to realize ZVS conditions. Several conventional synchronous dc-dc converters are connected in parallel to constitute interleaved structures [5] where inductor current of each phase flows in bidirectional directions (positive and negative). When the inductor current becomes negative, the energy stored in the inductor will discharge and charge the snubber capacitors, and if the stored energy in the inductor is not enough, ZVS conditions will not be achieved. However, the current ripple of each phase is very large.

Additionally, coupled inductors can also be utilized to achieve ZVS conditions. But in most soft switching converters, efficiencies can be improved greatly under heavy load conditions, but the effects are not good under light load conditions due to the additional power dissipations of auxiliary circuit branches. In some soft switching converters no matter how much the load is, the current waveform of the branch of the auxiliary coupled inductor is always the same.

Conventional buck converter and novel ZCS-ZVS buck converter with coupled inductor topology are presented in section II. Section III focuses on the detailed operating principles of each modes. Design of main circuits and analyses of simulation results of conventional buck converter and ZCS-ZVS buck converter with coupled inductor topology is given in section IV. Finally the conclusion is drawn in section V.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

II. CONVERTER TOPOLOGY AND OPERATING PRINCIPLES

The conventional buck converter topology and ZCS-ZVS buck converter with coupled inductor topologies are described in the following sections.

A. Conventional Buck Converter

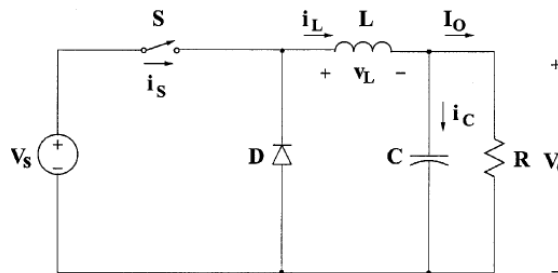


Fig.1. Conventional buck converter

The DC-DC converter is a device for converting one dc voltage level to another voltage level with a minimal loss of energy. DC conversion is of great importance in many applications, starting from low power applications to high power applications. A buck converter, as its name implies, can only produce lower average output voltage than the input voltage. The step-down dc-dc converter, commonly known as a buck converter, is shown in Fig. 1. It consists of dc input voltage source V_s , controlled switch S, diode D, filter inductor L, filter capacitor C, and load resistance R.

When the switch is on for a time duration DT, the switch conducts the inductor current and the diode becomes reverse biased. This results in a positive voltage $V_L = V_s - V_o$ across the inductor. This voltage causes a linear increase in the inductor current i_L . When the switch is turned off, because of the inductive energy storage, i_L continues to flow. This current now flows through the diode, and $V_L = -V_o$ for a time duration (1-D) T until the switch is turned on again.

The relationship among the input voltage, output voltage, and the switch duty ratio D can be derived, according to Faraday's law, the inductor volt-second product over a period of steady-state operation is zero. For the buck converter

$$(V_s - V_o)DT = -V_o(1-D)T \tag{1}$$

Hence, the dc voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$D = V_o / V_s \tag{2}$$

The dc-dc converters can have two distinct modes of operation: Continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM mode inductor current is continuous and in DCM mode it is discontinuous

B. ZCS-ZVS Buck Converter with coupled Inductor

The low-efficiency problem at light loads is mainly due to additional power dissipations of auxiliary circuit branches. Therefore an improved soft switching buck converter with coupled inductor topology is preferred to solve the low-efficiency problems at light loads. In this topology, the auxiliary circuit consists of an inductor coupled with the main inductor, a small inductor as well as a diode. The main MOSFET can operate under a ZCS condition at turn on and a ZVS condition at turn off.

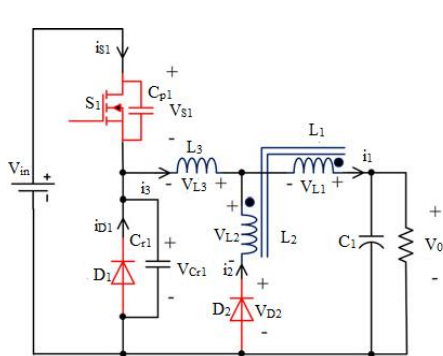


Fig.2. Circuit diagram of a ZCS-ZVS buck converter

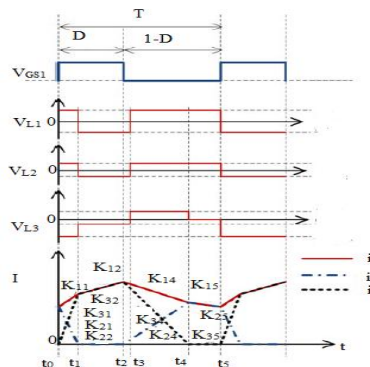


Fig. 3. Theoretical Waveforms of i_1, i_2, i_3 and inductor's voltages in steady state.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

The ZCS-ZVS buck converter topology is shown in Fig.2. In this topology, inductors L_1 and L_2 are tightly coupled on the same ferrite core, and L_1 is the main inductor. S_1 and D_1 are the main power switches, like a conventional buck converter. D_2 is an additional diode. The theoretical current waveforms of L_1 , L_2 , and L_3 of the proposed converter at steady state are shown in Fig.3. When S_1 is OFF, the converter comes into a free-wheeling stage. The branches of L_2 and L_3 will supply two flow channels for current freewheeling. Because L_3 is very small, the current of L_3 drops faster than that of L_1 , and also reduces to zero before S_1 turns ON. It provides the ZCS condition for S_1 .

Due to snubber capacitor C_{r1} , S_1 can turn OFF under a ZVS condition. C_{p1} is the parasitic capacitance of the MOSFET S_1 . But here no extra auxiliary MOSFET switch is added, so the control method is as simple as that of a conventional buck converter. The theoretical waveforms of inductor currents and voltages are required to analyse the ZCS-ZVS buck converter in steady state.

III. ANALYSES OF OPERATING PRINCIPLES

Based on the waveforms of the inductor currents, one switching cycle is divided into five intervals, as shown in Fig. 3, and the equivalent circuits for each interval are given in the section of corresponding modes of operation. Here K_{ij} denotes the slopes of inductor current at a different mode, where i denotes the number of the inductor and j denotes the number of the different operating mode. The detailed theoretical analyses of each mode will be given as follows.

1) Mode 1 [t_0-t_1]

Before t_0 , the converter works at a current free-wheeling stage, and both i_3 and i_{s1} are equal to zero. At t_0 , S_1 is triggered to conduct. Due to L_3 , i_{s1} will increase slowly, so S_1 can turn ON under a ZCS condition. Then, i_3 and i_1 will increase, and i_2 will go down. Since L_3 is very small, the current-rising rate of L_3 is larger than that of L_1 . At t_1 , i_3 and i_1 are equal, and i_2 is zero. It means that D_2 turns OFF automatically, and this mode ends. Based on KVL and KCL, we can get

$$\begin{cases} i_1 + i_2 + i_3 \\ V_0 - V_{L1} - V_{L2} = 0 \\ V_{L2} - V_{L3} - V_{in} = 0 \end{cases} \quad (3)$$

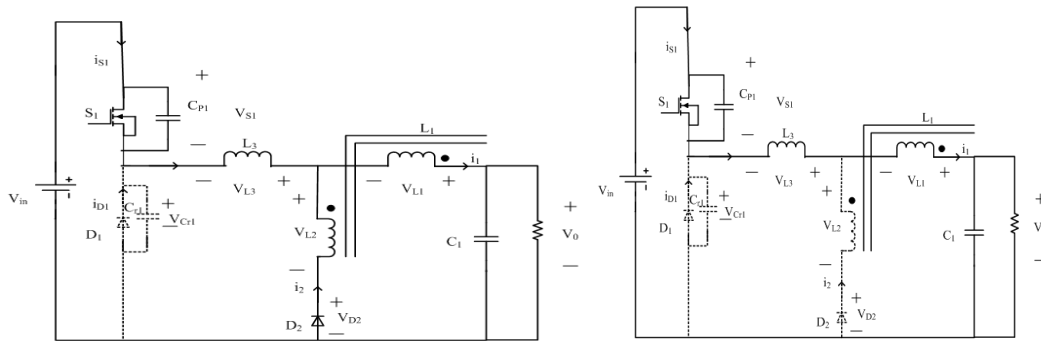


Fig. 3(a). Equivalent circuit for mode 1

The voltage equations of inductors L_1, L_2 and L_3 can be expressed as follows

$$\begin{cases} V_{L1} = -L_1 \frac{di_1}{dt} - M \frac{di_2}{dt} \\ V_{L2} = -L_2 \frac{di_2}{dt} - M \frac{di_1}{dt} \\ V_{L3} = -L_3 \frac{di_3}{dt} \end{cases} \quad (4)$$

Where M is the mutual inductance and equal to $\sqrt{L_1 L_2}$.

$$K_{11} = \frac{di_1}{dt} = \frac{V_{in} L_2}{(L_2 + M)L_3} - \frac{V_0(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \quad (5)$$

$$K_{21} = \frac{di_2}{dt} = -\frac{V_{in} L_1}{(L_1 + M)L_3} + \frac{V_0(M - L_3)}{(L_1 + L_2 + 2M)L_3} \quad (6)$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

$$K_{31} = \frac{di_3}{dt} = \frac{V_{in}}{L_3} - \frac{V_0 L_2}{(L_2 + M)L_3} \tag{7}$$

2) Mode 2 [t₁-t₂]

After t₁, i₃ and i₁ are equal, and both increase linearly. In this mode, D₂ is always OFF, and the branch of L₂ does not work. At t₂, S₁ turns OFF, and this mode ends. It is similar to that of a conventional buck converter. The slopes of i₁, i₂, and i₃

Fig.3(b). Equivalent circuit for Mode2

$$K_{12} = K_{32} = \frac{V_{in} - V_0}{L_1 + L_3}; K_{22} = 0 \tag{8}$$

3) Mode 3[t₂-t₃]

At t₂, S₁ turns OFF, and then a resonance occurs between inductors (L₁, L₃), parasitic capacitor C_{p1}, and snubber capacitors C_{r1}. C_{p1} is charged, and C_{r1} is discharged at the same time. When the voltage across C_{r1} reduces to zero, D₁ will conduct. This interval is very short, so it is assumed that the current in L₃ does not change in this mode. Because C_{p1} is very small, it can be neglected. Thus, the transition time T_{m1} can be obtained as follows.

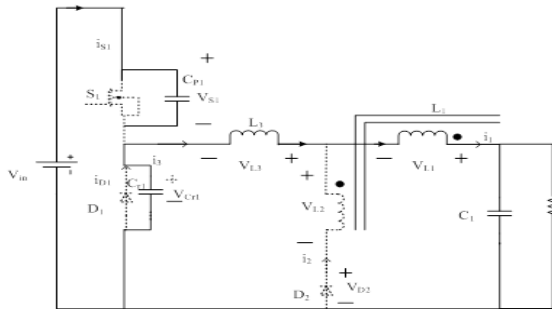


Fig.3(c). Equivalent circuit for Mode 3

$$T_{m1} = t_3 - t_2 = \frac{V_{in} C_{r1}}{I_{L3max}} \tag{9}$$

where I_{L3 max}, the value of i₃ at t₂ is positive and reaches a maximum in a switching cycle.

4) Mode 4 [t₃-t₄]

When D₁ conducts, D₂ will conduct simultaneously. The condition that D₂ will conduct is shown in the following analyses. Firstly, it is assumed that D₂ could not turn ON. The numbers of the turns of L₁ and L₂ are n₁ and n₂, respectively, so

$$V_{L1} = V_0 \times \frac{L_1}{L_1 + L_3} \tag{10}$$

Then

$$V_{L2} = \frac{n_2}{n_1} V_{L1} = \frac{n_2}{n_1} \times V_0 \times \frac{L_1}{L_1 + L_3} = \sqrt{\frac{L_2}{L_1}} \times V_0 \times \frac{L_1}{L_1 + L_3} = \frac{V_0 M}{L_1 + L_3} \tag{11}$$

From the KVL equation, we can get

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

$$V_0 - V_{L1} - V_{L2} - V_D = 0 \tag{12}$$

Substituting (10) and (11) into (12), we can obtain

$$V_{D2} = V_0 \times \frac{L_3 - M}{L_1 + L_3} \tag{13}$$

If D_2 conducts V_{D2} must be less than zero. i.e., the next inequality must be met $L_3 < M$ (14)

After t_3 , i_3 will decrease much faster than i_1 because L_3 is comparatively small. As long as i_3 reduces to zero, D_1 will turn OFF, and the condition of ZCS for S_1 is achieved. Then this mode naturally ends. After D_2 conducts, V_{D2} is equal to zero. Based on KVL and KCL, we can get

$$\begin{cases} i_1 = i_2 + i_3 \\ V_0 - V_{L1} - V_{L3} = 0 \\ V_{L2} - V_{L3} = 0 \end{cases} \tag{15}$$

Substituting (4) into (15), the current slopes of the inductors are obtained as follows:

$$K_{14} = \frac{di_1}{dt} = -\frac{V_0(L_3 + L_2)}{(L_1 + L_2 + 2M)L_3} \tag{16}$$

$$k_{24} = \frac{di_2}{dt} = \frac{V_0(M - L_3)}{(L_1 + L_2 + 2M)L_3} \tag{17}$$

$$K_{34} = \frac{di_3}{dt} = -\frac{V_0(L_2 + M)}{(L_1 + L_2 + 2M)L_3} \tag{18}$$

5) Mode 5 [$t_4 - t_5$]

At t_4 , D_1 turns OFF, then a small resonance between L_3 and C_{r1} occurs, in which i_3 oscillates around zero and the amplitude is pretty small, so i_3 is supposed to zero in this mode. Here, the current just flows through L_1 and L_2 , i.e., i_1 is equal to i_2 . Therefore, the slopes of i_1 , i_2 , and i_3 can be easily obtained as follows:

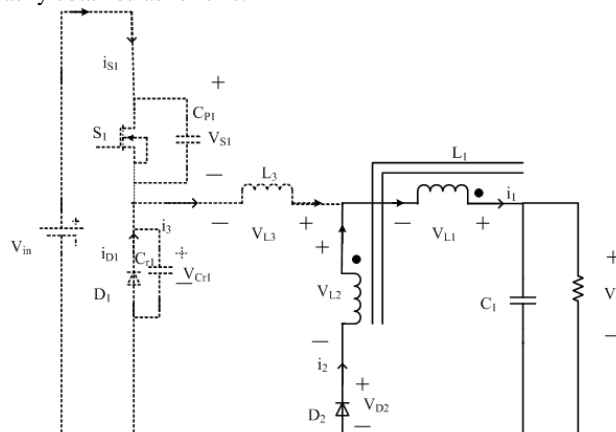


Fig.3(e). Equivalent circuit for Mode 5

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

$$K_{15} = \frac{di_1}{dt} = -\frac{V_0}{L_1 + L_2 + 2M} \tag{19}$$

$$K_{25} = \frac{di_2}{dt} = -\frac{V_0}{L_1 + L_2 + 2M}$$

$$K_{35} = 0 \tag{21}$$

III. DESIGN AND SIMULATIONS

A. Conventional Buck Converter

The duty ratio is given by:

$$D = \frac{V_{out}}{V_{in}} \tag{22}$$

On substituting the values of input voltage and output voltage given in Table I in (22) we get $D = 0.51$.

The value of capacitor and the inductor can be obtained from the relation below:

$$C = \frac{T_s V_0 (1 - D) T_S}{8L \Delta V_0} \tag{23}$$

(23) ΔV_0 -Ripple voltage (0-10% of output voltage) and $T_s = 1/f_s = 2\mu s$. On

substituting the values of T_s, V_0, L and assuming $\Delta V_0 = 0.141$ and L from the Table I, the value of C is obtained as $100\mu F$.

R- Load resistance

C- Capacitance

T_s -Switching Time period

f_s -Switching Frequency

$$L = \frac{(V_{in} - V_0) \times \left(\frac{D}{f_s}\right)}{\Delta I_L} \tag{24}$$

ΔI_L -Ripple current (0-30% of the load current).

Similarly the value of inductor is obtained as $62.3\mu H$.

The conventional buck converter is designed for a switching frequency of 50 kHz and a duty ratio of 0.51. The parameter values thus obtained are tabulated as shown below.

TABLE I

SIMULATION PARAMETERS OF CONVENTIONAL BUCK CONVERTER

Input Voltage	70V
Output Voltage	36V
Inductance	62.3 μ H
Capacitance	100 μ F
Resistive load	2.16 Ω
Switching Frequency	50KHz
Duty Ratio	0.51

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

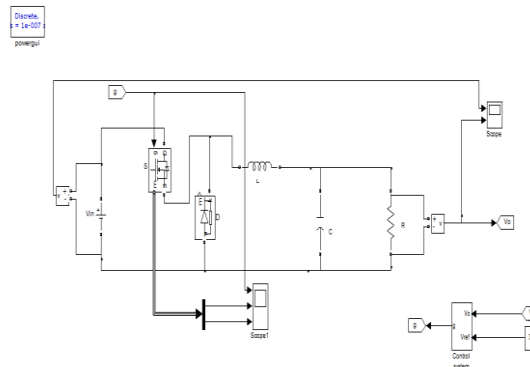


Fig. 4. Simulation of conventional buck converter

B. ZCS-ZVS Buck Converter with Coupled Inductor

To ensure that the ZCS-ZVS buck converter operates under the soft-switching condition, component parameters must be designed properly, especially the selections of the inductors (L_1, L_2 and L_3). The current of L_3 must be discontinuous to achieve soft-switching conditions. As the load increases, the duration that the current of L_3 remains zero will reduce to zero, and then L_3 will work at a continuous conduction mode (CCM) and discontinuous conduction mode (DCM) can be used to calculate the parameters of main circuits. It can be assumed that the buck converter would operate under BCM at a theoretic maximum load, which is more than the real maximum load.

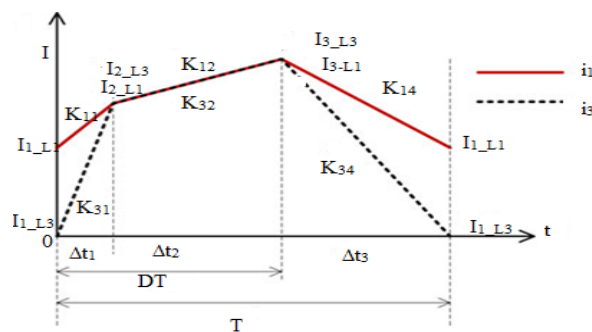


Fig. 5. Theoretical waveforms of inductors currents at BCM.

TABLE II
RELATED TARGET SPECIFICATIONS OF THE ZCS-ZVS BUCK CONVERTER

Parameters	Values
V_{in}	70 V
V_0	36 V
P_{output_max}	600 W
f_{sw}	50 kHz
T	20 μ s
$I_{Load_Max_Real}$	16.7 A
$I_{Load_Max_Theoretic}$	18.4 A
I_{1_L1}	14.72 A
I_{2_L1}	17 A
I_{3_L1}	22.08 A
I_{1_L3}	0 A
I_{2_L3}	17 A
I_{3_L3}	22.08 A

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

The theoretical waveforms of inductor currents at BCM are shown in Fig. 5. In this design, the theoretic maximum load is set to be 1.1 times the real maximum load. In Fig. 5, it can be seen that mode 5 does not occur in BCM. Because the duration time of mode 3 is very short, it is not considered for calculating inductor parameters. One switching cycle can be divided into three intervals. Based on the slopes and variations of $L_1, L_2,$ and $L_3,$ some equations can be obtained as in (25).

The Inductor currents of mode 1 and mode 3 are attained by the theoretical maximum load average current, and the ripple coefficient of the inductor current. T is the time of one switching period. Then $\Delta t_1, \Delta t_2, \Delta t_3, L_1, L_2,$ and L_3 can be solved from (25), and the duty ratio D is equal to $(\Delta t_1 + \Delta t_2)/T$.

$$\begin{cases} \Delta t_1 + \Delta t_2 + \Delta t_3 = T \\ K_{11} * \Delta t_1 = I_{2_L1} - I_{1_L1} \\ K_{31} * \Delta t_1 = I_{2_L3} - I_{1_L3} \\ K_{12} * \Delta t_2 = I_{3_L1} - I_{2_L1} \\ K_{14} * \Delta t_3 = I_{1_L1} - I_{3_L1} \\ K_{34} * \Delta t_3 = I_{1_L3} - I_{3_L3} \end{cases} \quad (25)$$

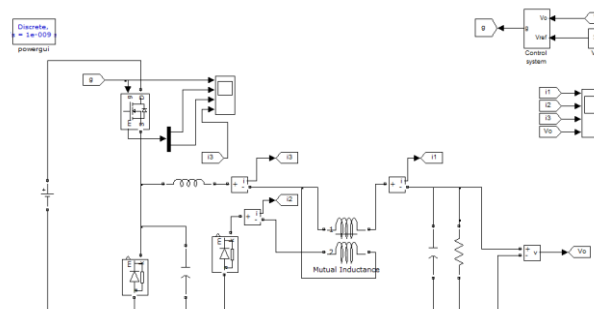


Fig. 6. Simulation of ZCS-ZVS buck converter

The related target specifications shown in Table II are substituted into (25), the solved results are presented in Table III, where the basic equation in a buck converter as $D = V_o/V_{in}$ is also met in BCM.

TABLE III
SOLVED RESULTS OF INDUCTANCES AND DURATION TIMES

Δt_1	0.623μs
Δt_2	9.66μs
Δt_3	9.71μs
L_1	62.3μH
L_2	1.49μH
L_3	2.37μH
D	0.51

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

TABLE IV
SIMULATION PARAMETERS OF ZCS-ZVS BUCK CONVERTER

Sl. No.	Components	Ratings
1	DC Source	70 V
2	Output Voltage	36 V
2	Inductor L_1	62.3 μ H
3	Inductor L_2	1.92 μ H
4	Inductor L_3	1.4 μ H
5	Snubber Capacitor C_{r1}	4700 pF
6	Output Capacitor C_0	100 μ F
7	Resistive Load R	2.16 Ω

The simulation parameters of ZCS-ZVS buck converter is shown in Table IV.

C. Simulation Results

The conventional buck converter and ZCS-ZVS buck converter was simulated using MATLAB/SIMULINK and the resulting waveforms are as shown below.

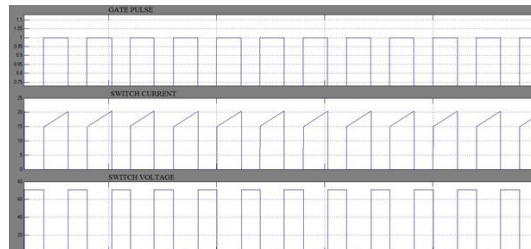


Fig. 7. Gate pulse, switch current and voltage waveform of conventional buck converter.

During the turn on process, after the gate trigger pulse is applied switch current increases and switch voltage decreases to zero which give rise to switching loss and during the turn off process switch current decreases to zero and switch voltage rises to a value equal to the input voltage which again give rise to switching losses which in turn reduces the efficiency of conventional buck converter. From the Fig. 7.it can be inferred that soft switching is not applicable here and the basic buck converter works under hard switching conditions. Switch suffers from high voltage and current stress under hard switching conditions.If a converter works under hard switching condition, switching losses increases at higher switching frequency and the total efficiencies will drop.

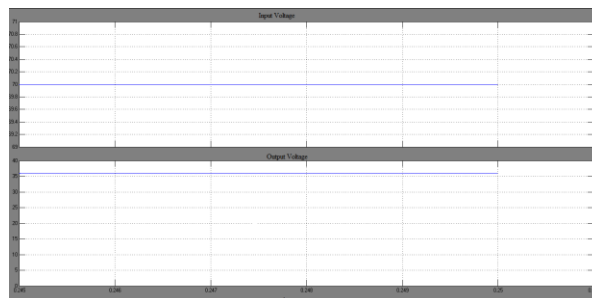


Fig. 8. Input voltage and Output voltage waveforms of Conventional buck converter.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Special Issue 13, December 2015

Here conduction losses will be high and efficiency will be poor at light loads. At higher switching frequency the switching losses will be high when compared to ZCS-ZVS buck converter. It can be inferred from the waveform that switching loss is more for a conventional buck converter which works under hard switching condition. Here soft switching technique cannot be adopted due to the absence of auxiliary circuits used to realize soft switching technique used in the ZCS-ZVS buck converter.

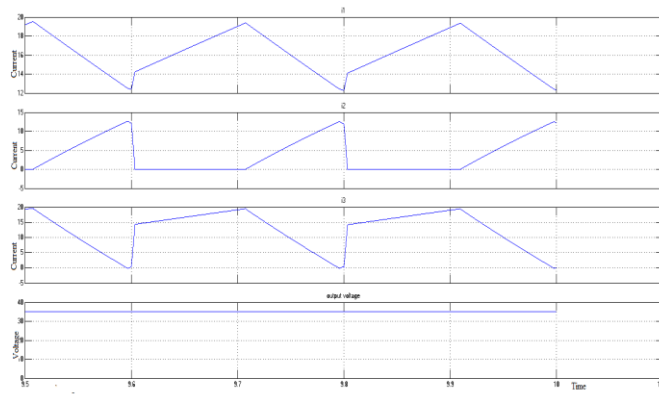


Fig. 9 Simulation results of ZCS-ZVS buck converter with coupled inductor.

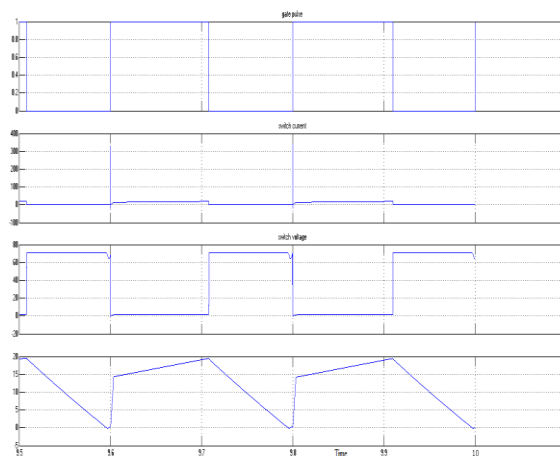


Fig.10 Switching waveforms of Switch S_1 , and Current waveform of L_3 .

The simulation results of ZCS-ZVS buck converter with coupled inductor is shown in Fig. 9. The theoretical maximum load (18.4A) and the real maximum load (16.7A) along with the simulation waveforms of i_1, i_2, i_3 are obtained from the parameters shown in Tables II and III. In Fig. 9, it can be seen that inductor L_3 works under BCM and mode 5 does not occur for a theoretical maximum load. But for a real maximum load i_3 remains zero in a short time and thereby ZCS turn on can be realized.

VI. CONCLUSION

The conventional buck converter and ZCS-ZVS buck converter were simulated using MATLAB/SIMULINK. The comparison between the both topologies was made. It was found that by making inductor L_3 to work under DCM, ZCS turn on and ZVS turn off for S_1 were achieved. Moreover no auxiliary MOSFET is added in this topology, so the control method is as simple as that of conventional buck converter. The low efficiency problem at light loads can be solved easily using the ZCS-ZVS buck converter with coupled inductor topology than the conventional buck converter.

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