RF & Logical Performance Inas Based DMG HEMT High Speed & High Power Application

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ABSTRACT: In this paper we have double material gate (DMG) HEMT. It has variation in barrier layer thickness affects nitide-based HEMTs more strongly than antimonide-based DMG HEMTs. Higher Electron Mobility and drift velocity can be realized by reducing of Lg and increasing the indium content in the InAs channel. Due to the high electron mobility, velocity and large conduction band offset InAs. InAs-channel HEMT is promising for high speed logic applications. Greater potential of 40nm InAs HEMTs. InAs HEMTs has ultra low-noise, sub-millimeter wave and terahertz applications.

KEYWORDS: InAs, HEMT, Dual Material Gate (DMG), RF, high speed and high power application.

I. INTRODUCTION

Antimonide-based compound semiconductor are opening a new field for semiconductor industry as can be used both as third generation infrared photo-detectors and ultra-high speed, ultra-low power consuming integrated circuit fabrication [1]. DMG structure is more effective to reducing SCEs for antimonide-based HEMTs than nitride-based HEMT, while nitride-based DMG HEMT give more efficient carrier transport than antimonide-based counterpart [2]. In the field device technology, HEMTs are gain interest due to their potential to replace MOSFETs. In HEMTs are faster, low power consuming and easy to fabricate compared to MOSFET[3].

Scaling of device is a fundamental in semiconductor industry to make smaller, fast and less power consume chips HEMTs follow the trend [4]. In DMG FET, two gates made different materials of different work functions is joining laterally to create a single gate. The work function one of gate M1 is chosen to be greater than the other M2. Gate M1 works as controlling gate and gate M2 works as screening gate of drain voltage. It enhances electric field and inserts a step function in channel potential at interface of double gates. The enhanced average electric field improves the carrier transport efficient and the step functions reduce the short channel effects. But the scaling going in to deep sub-microns level, the need for an analytical modelling of subthreshold behavior of DMG HEMT emerges. S.P.Kumar et al. [5] first proposed an analytical model for the subthreshold behavior of nitride-based DMG FET. In our previous paper [2] the model of [5] was modified and an analytical model for antimonide-based HEMTs was developed.

In [2], the Al0.3In0.7Sb/InAs combination used of barrier and channel. Among the antimony-based material AlSb and GaSb are approximately lattice match to InAs and these semiconductors are jointly known as 6.1 A° family. In this paper we also study the Al0.3Ga0.7Sb/GaSb and Al0.3In0.7Sb/In0.15Ga0.85Sb barrier and channel combinations and compare their results.

II. DEVICE FABRICATION

Fig.1 is the schematic of symmetric Double-Metal-Gate (DMG) In0.3Al0.7Sb/InAs HEMT. The work function of metal M1 and M2 respectively. As it will be n-channel HEMT, so M1 must be greater than M2 [5]. We have chosen the value
of gate work function for M1 and M2 5.2eV and 4.2eV respectively the barrier layer completely depleted under normal condition and to confined electron in the heterointerface In$_{0.3}$Al$_{0.7}$Sb/InAs. Table 1 show the parameter used in the HEMT model.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Name of the parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nd</td>
<td>Doping in the barrier layer</td>
<td>10$^{19}$ cm</td>
</tr>
<tr>
<td>Nd$^+$</td>
<td>Doping in source and drain region</td>
<td>10$^{17}$ cm</td>
</tr>
<tr>
<td>T</td>
<td>Operating temperature</td>
<td>300K</td>
</tr>
<tr>
<td>L</td>
<td>Total Effective channel length</td>
<td>120nm</td>
</tr>
<tr>
<td>d_d</td>
<td>Thickness of doped barrier layer</td>
<td>25nm</td>
</tr>
<tr>
<td>d_i</td>
<td>Thickness of spacer layer</td>
<td>5nm</td>
</tr>
<tr>
<td>£_s</td>
<td>Dielectric constant of</td>
<td>12.6</td>
</tr>
</tbody>
</table>

III. RESULTS AND DISCUSSIONS

We used TCAD device simulator of channel potential and electric field distribution along the channel to verify the model of [2] Fig.2 show electric field Variations vs. normalized channel length and the channel potential vs. normalized channel length for DMG In$_{0.3}$Al$_{0.7}$Sb/InAs HEMT.

Figure 2 $I_{DS}$–$V_{GS}$ characteristics of the device with $L_g=120$nm
We have shown the effects of varying gate length of metal gate keep go to the total length L constant. As we can see in the figures 1, the minimum potential barrier and thus enhances the drive current (I_on). The total current drain of gm = 0.0015950 and V_T= 0.6160125. Its show the increases in control of gate over than channel potential.

![Image](image1.png)

**Figure 3** I_Ds–V_Ds characteristics of the device with L_G= 120 nm

Device current–voltage (I–V) measurements were carried out on devices with a gate–source distance L_gs of 0.04µm, a gate length L_g of 0.12µm, and a gate–drain distance L_gd of 0.04µm. For these simulations, the gate1 voltage is kept at 5.3V and various gate2 voltage 4.5–5V.

![Image](image2.png)

**Figure 4** Variation of channel potential with normalized channel position for different combination of gate length L1 and L2, keeping the L constant for gate In0.3Al0.7Sb/InAs HEMT

In figure 4 we have shown the effects of varying the gate length of first metal gate (L1) keeping the total gate length L_constant. As we can see in the figure-4, the minimum potential increases as the L1 decreases. It reduces the potential barrier and thus enhances the drive current (I_on). Moreover it increases the control of gate over the channel potential. The change in with change in L1 for various formations of HEMTs.

![Image](image3.png)

**Figure 5** L constant for gate L_g = 120 nm In0.3Al0.7Sb/InAs HEMT having a simultaneous record f_T of 280 GHz and an f_0 of 621 GHz at V_DS = 0.5 V.
To avoid this problem, we have focused on $V_{DS} \leq 0.5$ V because in this region $L_g$ is relatively well behaved and our small signal model predicts the gain characteristics. Using this model, Figure 1 we extrapolated a value of $f_{max}$ of 621 GHz at $V_{DS} = 0.5$ V. The average $f_{max}$ obtained the various systems at this bias point is 661GHz ±4 GHz. We are confident in reporting an $f_{max}$ of 621 GHz at the bias point. Our small-signal model extraction reveals that this excellent value of $f_{max}$ arises from a combination of $g_m/g_{o} = 15.4$ and $C_{gs}/C_{gd} = 6.3$. The relatively low values of $C_{gd}$ arise partly from the widening $L_s$ide. To our knowledge of the authors, this is the first simultaneous demonstration of both $f_r$ and $f_{max}$ in excess of 621GHz in any transistor technology on this material system.

IV. CONCLUSIONS

To solve the problem of short channel effect and carrier transport inefficiency of the HEMTs, a new structure called Double Material Gate (DMG) was proposed. In the work gate threshold voltage not good efficiently so improving threshold MOSHEMT werealternative solutions for solving this problem. The result of the proposed model matches very well with results obtained from TCAD device simulator.

Moreover, our model has reducing SCEs and increasing transport efficiencies. So our model opens up solutions for short channel effects removing in the interesting field of semiconductor technology. Further we can improve triple material gate (TMG) and also Double Gate on this model by that DIBL still reduce more and frequency increase on HEMT. Than more we can develop HEMT structure into MOSHEMT.

REFERENCES


