

A Platform for Evaluating Low-Energy Multiprocessors on Cots Devices

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ABSTRACT: Embedded systems are usually energy constrained. Moreover, in these systems, increased productivity and reduced time to market are essential for product success. To design complex embedded systems while reducing the development time and cost, there is a great tendency to use commercial off-the-shelf (“COTS”) devices. At system level, dynamic voltage and frequency scaling (DVFS) is one of the most effective techniques for energy reduction. Nonetheless, many widely used COTS processors either do not have DVFS or apply DVFS only to processor cores. An easy-to-implement COTS-based evaluation platform for low-energy embedded systems is presented. To achieve energy saving, DVFS is provided for the whole microcontroller including core, phase-locked loop, memory, and I/O. In addition, facilities are provided for experimenting with fault-tolerance techniques. The platform is equipped with energy measurement and debugging equipment. Physical experiments show that applying DVFS on the whole microcontroller provides up to 47% and 12% energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively. Although the platform is designed for ARM-based embedded systems, our approach is general and can be applied to other types of systems.

I. INTRODUCTION

Embedded systems are ubiquitous, and demand for these systems is growing progressively. A wide range of embedded systems are battery operated. As, for many of these systems, there is no possibility of frequently charging or replacing their batteries, they are highly energy constrained. Power consumption is the limiting factor for the functionality of future wearable devices. Since interactive applications like wireless information access generate bursts of activities, it is important to match the performance of the wearable device accordingly. This paper describes a system with a microprocessor whose speed can be varied frequency scaling as well as its supply voltage. Voltage scaling is important for reducing power consumption to very low values when operating at low speeds. Measurements show that the energy per instruction at minimal speed is 1/5 of the energy required at full speed. The frequency and voltage can be scaled dynamically from user space. This allows power-aware applications to quickly adjust the performance level of the processor whenever the workload changes. Experiments with an H.263 video benchmark show that the power-aware decoder outperforms a static fixed-frequency policy as well as a dynamic interval-based scheduler. Lowering the supply voltage requires all components to operate at low voltage. Additional reductions can be obtained by selectively lowering the supply voltage of specific parts. An obvious candidate is the processor since it is responsible for 10 to 30% of the power consumption. The dynamic approach to low power is using power down features to minimize the power consumption of unused hardware. For portable computers this means turning of the hard disk, processor, screen, modem, sound. Power consumption is becoming the limiting factor for the functionality of wearable devices, because advances in battery technology are progressing slowly whereas computation and communication demands are increasing rapidly.

In this paper, a new fault injection approach to measure SEU sensitivity in COTS microprocessors is presented. It consists in a hardware-implemented module that performs fault injection through the available JTAG-based On-Chip Debugger (OCD). This approach can be applied to most microprocessors, since JTAG standard is a widely supported interface and OCDs are usually available in current microprocessors. Hardware implementation avoids the communication between the target system and the software debugging tool, increasing significantly the fault injection efficiency. The method has been applied to a complex microprocessor (ARM). Experimental results demonstrate the approach is a fast, efficient, and cost-effective solution. For illustration- 8051 microcontroller has all program & data

memory, counters & timers, interrupts, I/O ports and therefore its embedded memory microcontroller. There are existing approaches to inject faults by means of using the OCD but they have some of the following limitations: Communication with the host PC is necessary, which is a time bottleneck; they are not easily applicable to different microprocessors, since a specific vendor's mechanism is used, or they imply intrusiveness because a modification of the target system is required. This paper presents a fault injection method devised to inject faults in any microprocessor that supports an OCD with Joint Test Action Group (JTAG) interface. The injection system is implemented in hardware in order to accelerate the evaluation process. This approach is nonintrusive, because no target system modification is required. It is a widespread solution, since the JTAG standard is one of the most common interfaces used, and because it profits from the OCD available in current microprocessors.

These are the five observations.

- 1) The high-to-low voltage scaling delay is greater than the low-to-high delay (about 45% for the processor core and PLL and about 110% for memory and I/O).
- 2) Voltage and frequency scaling is very effective in reducing power consumption not only for the processor core but also for the other parts of the microcontroller, including PLL, memory, and I/O.
- 3) Although PLL, memory, and I/O have less power consumption compared with the processor core, they have comparable energy consumption to that of the core.
- 4) Although PLL has a very small contribution in the total power consumption, as it is always operational, its energy consumption is comparable with that of the others.
- 5) Applying DVFS on the whole microcontroller results in a considerable energy savings compared with the sole use of DPM or applying DVFS only on the processor core.

II. HARDWARE PLATFORM DESIGN

The microcontroller is composed of an ARM7 processor core, a system controller, memory elements, and peripheral devices. It is noteworthy that the computational power of ARM7 is quite sufficient for the majority of embedded applications. For example, ARM7 can easily execute all benchmarks in MiBench benchmark suite. When you are looking for the right embedded processors, with the FutureElectronics.com parametric search, you can filter the results by various attributes: by Clock Frequency 16 Hz, 200 MHz, 266 MHz, 400 MHz, RAM size 512 B, 4 kB, 32kB, 64 k, Data Bus Width from 16 b to 32 b. ARM7 can also execute fairly complex operating systems e.g., Real-Time Executive for Multiprocessor Systems RTEMS and Keil RTX. Nevertheless, for highly computation-intensive applications, the performance of ARM7 might not be adequate. In this case, it should be noted that our proposed platform is not inherently dependent on ARM7. Most I/O lines of the peripherals are multiplexed with the parallel I/O (PIO) controller. Each PIO line may be assigned to a peripheral or used as general purpose I/O. These features provide flexibility to designers and assure effective use of the components.

A. COTS DEVICES ON EMBEDDED SYSTEM

Commercial Off-The-Shelf (COTS) is a term that references non-developmental items (NDI) sold in the commercial marketplace and used or obtained through government contracts. The set of rules for COTS is defined by the Federal Acquisition Regulation (FAR). A COTS product is usually a computer hardware or software product tailored for specific uses and made available to the general public. Such products are designed to be readily available and user friendly. A typical example of a COTS product is Microsoft Office or antivirus software. A COTS product is generally any product available off-the-shelf and not requiring custom development before installation.

B. ISOLATION AMPLIFIER

Isolation amplifiers are a form of differential amplifier that allows measurement of small signals in the presence of a high common mode voltage by providing electrical isolation and an electrical safety barrier. Isolation amplifiers are a form of differential amplifier that allows measurement of small signals in the presence of a high common mode voltage by providing electrical isolation and an electrical safety barrier. They protect data acquisition components from common mode voltages, which are potential differences between instrument ground and signal ground. Instruments that are applied in the presence of a common mode voltage without an isolation barrier allow ground currents to circulate, leading in the best case to a noisy representation of the signal under investigation. In the worst

case, assuming that the magnitude of common mode voltage or current is sufficient, instrument destruction is likely. Isolation amplifiers are used in medical instruments to ensure isolation of a patient from power supply leakage current.

C. RECORDING ELECTRODE

Recording electrode transfers electrical potentials at the recording site to the input of the recording machine.

Device to record one of the two extremities of an electric circuit; one of the two poles of an electric battery or of the end of the conductors connected there. An electrical terminal specialized for a particular electrochemical reaction.

D. LOW PASS FILTER

A low-pass filter is a filter that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than the cut off frequency. A low-pass filter is a filter that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than the cut off frequency. The amount of attenuation for each frequency depends on the filter design. The filter is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass filter.

Low-pass filters exist in many different forms, including electronic circuits, anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend. An optical filter can correctly be called a low-pass filter, but conventionally is called a long pass filter, to avoid confusion.

III. PROPOSED SYSTEM

The aim is to design complex embedded systems while reducing the development time and cost, there is a great tendency to use commercial off-the-shelf ("COTS") devices ECG is given as the input. Here, an easy-to-implement COTS-based evaluation platform for low-energy embedded systems is presented. To achieve energy saving, DVFS is provided for the whole microcontroller. In addition, facilities are provided for experimenting with fault-tolerance techniques. The platform is equipped with energy measurement and debugging equipment. Physical experiments show that applying DVFS on the whole microcontroller provides up to 47% and 12% energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively. In dealing with today's highly competitive embedded systems markets and time-to-market pressure and in order to deliver correct-the-first-time products with multiple system requirements, the use of commercial off-the-shelf (COTS) device is very beneficial in designing embedded systems. Some vendors offer reconfigurable hardware solutions to accelerate the design process and provide a variety of programmable logic device (PLD)-based evaluation kits. However, instead of focusing embedded systems, these platforms allow to functionally test the SOC or ASIC devices to be produced. It provides DVFS capability for the microcontrollers, including not only the processor cores but also PLL, memory, and I/O memory, and I/O is quite effective includes circuitry too accurately and separately measure energy/power consumption. It based on an ARM-based COTS microcontroller; hence, it can be used for a wide range of existing microcontroller. Future Electronics has a full selection of embedded processors from several manufacturers, including embedded microprocessor chips and embedded microcontroller chips and even an FPGA embedded processor. Simply choose from the embedded processor technical attributes below and your search results will quickly be narrowed in order to match your specific embedded processor application needs. For illustration- 8051 microcontroller has all program & data memory, counters & timers.

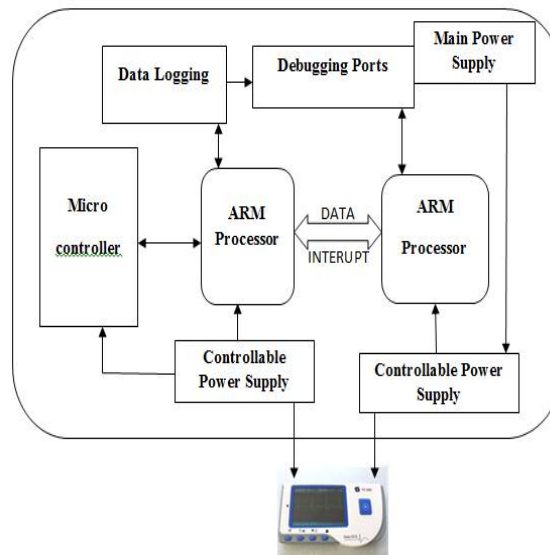


Figure 1:Block diagram of hardware platform

IV. ENERGY MANAGEMENT AND DEBUGGING UNITS

The power management for microprocessors can be done over the whole processor or in specific components, such as cache memory and main memory. With dynamic voltage scaling and dynamic frequency scaling, the CPU core voltage, clock rate, or both, can be altered to decrease power consumption at the price of potentially lower performance. This is sometimes done in real time to optimize the power-performance trade-off.

Monitoring packet routing or packet loss data for misbehavior detection of communication protocol compliance during packet transmission, IDSs for MCPSs may test medical sensor measurements and actuator settings for misbehavior detection of physical properties manifested because of attacks.

Examples:

1. AMD Cool'n'Quiet
2. AMD Power Now
3. IBM Energy Scale
4. Intel Speed Step
5. Transmeta LongRun and LongRun2
6. VIA LongHaul PowerSaver

4.1 POWER MANAGEMENT TECHNIQUES

Dynamic Voltage and Frequency Scaling (DVFS) describes the use of two power saving techniques (dynamic frequency scaling and dynamic voltage scaling) used to save power in embedded systems including cell phones. This type of power saving is different from what most of us generally think about like standby or hibernate power states. All of these are useful of course. You can reduce the power consumed by your embedded system by lowering the frequency and or voltage of the CPU and attached peripherals. This can be done by using several voltage and frequency scaling techniques.

1. DPM

DPM usually has only two operational states for systems components, namely active and idle. The active power consumption of a clock-enabled component can be determined by its operating frequency and supply voltage, as denoted by PActive.

$$P_{Active} = I_{Leakage}V + C_{eff}V^2f \text{ ---Eqn (1)}$$

2. DVFS

The basic idea behind DVFS techniques is to determine the minimum frequency that satisfies all timing constraints and then to adjust the lowest possible voltage that allows this speed. Assuming a linear relationship between frequency and voltage, the combined effects of voltage and frequency scaling result in decreasing the active power consumption proportional to V^3 and reducing the energy consumption proportional to V .

Clock Description	Power Management Scheme
Master Clock	Selecting a slow clock
Processor Clock	Switching off the processor in idle mode
Peripheral Clock	Individually disable the peripherals clock
USB Clock	Disabling the associated Peripherals Clock

2. Therefore, by scaling both the voltage and frequency, the energy can be significantly reduced. However, this achievement does not come for free because a tradeoff exists between speed and energy consumption. Software-controlled clock generators and voltage regulators allow the system to use DVFS. This provides the possibility for the device to vary the supply voltage rather than using just a single fixed voltage. To provide voltage scaling capability for this device, the dc/dc converter and embedded voltage regulator in is replaced with a controllable power supply.

3. OPPORTUNITIES OFFERED BY PARALLEL PROCESSING

Since the proposed platform has multiple processing units i.e., two ARM7-based and one AVR-based microcontrollers and since it has the facilities for energy power management i.e., DVFS and DPM, one advantage of the platform is that it can be used to research into the possible opportunities for energy management that may be offered by parallel processing. To give an insight into this issue, we provide an example to illustrate when DVFS is used in executing parallel tasks; a two-processor system consumes less energy as compared with a single-processor system. Suppose that the slack time that is available to execute two tasks T1 and T2 with N1 and N2 CPU cycles is S. $N1/f_{max}$ and $N2/f_{max}$ are respectively

4. DEBUG AND TEST UNITS

To debug a program or hardware device is to start with a problem, isolate the source of the problem, and then fix it. A user of a program that does not know how to fix the problem may learn enough about the problem to be able to avoid it until it is permanently fixed. When someone says they've debugged a program or "worked the bugs out" of a program, they imply that they fixed it so that the bugs no longer exist.

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of or one or more faults within some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naively designed system in which even a small failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability or life-critical systems. JTAG interface is one of the most common OCD interfaces in current microprocessors. Including a JTAG controller in the Hardware-Implemented Fault Injection System makes it applicable to most microprocessors. The hardware implementation prevents the need to interact with an externally attached PC at intermediate stages of the fault injection process, saving a large amount of required time. Debugging Commands Module contains the sequence of JTAG commands necessary to perform the required debugging tasks, such as reading or writing registers and memory, setting breakpoints, restarting the execution, etc. A debugging action for example, read a register is executed by introducing several JTAG instructions and data. Depending on the action to perform, the set of required JTAG commands is different. A set of commands for every required action has been developed. Each set is named a utility. The Fault Injection Controller activates the corresponding commands according to the actual state, establishing the command execution order.

For mission- and safety-critical real-time embedded systems, energy efficiency and reliability are two important design objectives that must be often achieved simultaneously. Recently, the standby-sparing scheme that uses a primary processor and a spare processor has been exploited to provide fault tolerance while keeping the energy consumption under control through DVS and DPM techniques. We consider the standby-sparing technique for fixed-priority periodic real-time tasks. We propose a dual-queue mechanism through which the executions of backup tasks are maximally delayed, as well as online algorithms to manage energy consumption. Our experimental results show that the proposed scheme provides energy savings over time-redundancy based techniques while offering reliability improvements.

5. EXTENSIONS AND FUTURE WORK

The proposed platform can provide an experimental setup for different research projects. For example, the platform can be used to experiment with fault-tolerance techniques as a direction for future work by the use of these facilities. 1) The two microcontrollers are connected such that they can interrupt, restart, and turn on/off each other. 2) Each of the microcontrollers can access the internal parts of the other via JTAG. This is helpful to implement fault detection mechanisms that require comparing parts of a Processor with their correspondents in the other one.

V. CONCLUSION

A hardware platform that consists of two ARM-based microcontrollers, each fed separately by variable voltages. This platform is very suitable for evaluating embedded systems with low energy consumption and fault tolerance requirements. In this platform, we provide DVFS capability for the whole microcontroller including the processor core, PLL, memory, and I/O. Physical experiments show that applying DVFS on the whole microcontroller is considerably more efficient in reducing power/energy consumption compared with applying DVFS only on the processor core or using power-down policies that are currently used by most embedded processors. Physical experiments show that applying DVFS on the whole microcontroller provides up to 47% and 12% energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively. In addition, the platform is equipped with accurate energy/power measurement units, debugging ports, and facilities for evaluating fault-tolerance techniques. Although the platform is designed for ARM-based microcontrollers, it is general, and other COTS devices and embedded processors can be similarly used in the design of the platform.

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