

# An Improved Novel 64-Bit QCA Adder

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**ABSTRACT:** This paper presents a new design of a novel 64-bit quantum-dot-cellular automata (QCA) adder that achieved speed performances higher than all the existing adders of the same bit span, less area requirement and less power consumption compared to the cheap Ripple Carry Adder (RCA) and Carry Flow Adder (CFA) established. It also decreases the number of QCA cells compared to previous design. QCA is an attractive Nano-electronic computing technology based on cells of coupled quantum dots. The 64-bit novel adder operates in the RCA fashion but it could propagate a carry signal through a number of cascaded majority gates (MGs) significantly lower than the conventional adders. In adding together, the number of clock cycles required for completing the explanation was also limited because of the adopted basic logic and layout strategy.

**KEYWORDS:** Adders, Nano-electronic computing, Quantum-dot-Cellular (QCA).

## I. INTRODUCTION

Quantum-dot-Cellular (QCA) is an attractive emerging technology featuring computer operations at high speed and low power consumption. It was proposed by Craig S. Lent [1] at the university of Notre Dame [2]. A comprehensive study on this subject is found in [3]. The QCA technology is based on the encoding of binary information in the charge configuration within quantum dot cells. The columbic interaction between the QCA cells provides the required computational power. There is no current flowing between the cells and so, no power or information is delivered to individual internal cells [4]. The cells are locally interconnected due to the physics of cell-to-cell interaction because of the rearrangement of electron positions [5-6]. Recent papers show that QCA can achieve high density, fast switching speed and room temperature operation [7]. In the last few years, the efficient logic circuit design has received a great deal of attention. The arithmetic circuits have got special efforts in this manner with the major interest focused on the binary addition. Of course, the designs commonly employed in traditional CMOS are considered a first reference for the new design environment.

Ripple Carry, Carry look ahead and conditional sum adders were implemented. The carry flow adder shown in was mainly an improved RCA in which detrimental wires were mitigated. Parallel-prefix architectures like Brent-kung adder and Han-Carlson adder were analyzed and implemented in QCA. Recently further efficient designs were proposed for the CLA and BKA. Theoretical formulations established for CLA and parallel-prefix adders were exploited here for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit positions with the delay of just one majority gate (MG). In addition to this, the top level architecture leads to very compact layout, thus avoiding unnecessary clock phases due to lengthy interconnections. The paper also proposes a detailed analysis and design strategy for an improved 64-bit adder using QCA technology. The new QCA adder design reduces the number of QCA cells compared to existing reported designs. We demonstrate that it is possible to design a CLA QCA one-bit adder with the same reduced hardware as the bit serial adder, as retaining the simpler clock scheme and parallel structure of the novel CLA approach. The proposed design is based on a new algorithm that requires only three MGs and two inverters for the QCA addition. Thus, the bit serial QCA adder uses a version of the proposed one-bit QCA adders.

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

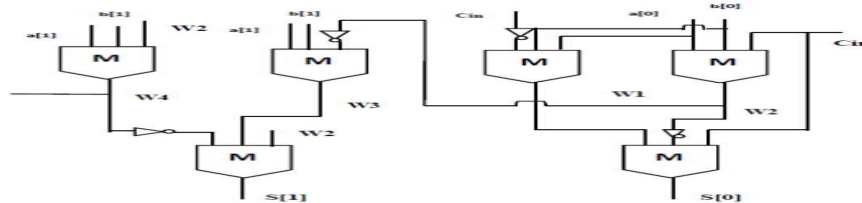


Fig.1.Novel 2-bit basic module

The proposed adder runs in the RCA fashion but it exhibits a computational delay lower than all the state-of-the-art competitors and achieves the lowest area-delay product (ADP).

## II. BACK GROUND

The QCA cell is the basic unit of QCA created with four quantum dots positioned at the vertices of a square. The cell is charged with two extra electrons which are able to tunnel through the dots inside the cell. Because of the coulombic repulsion, the two electrons will always tend to occupy the opposite corners. It is assumed that the tunneling to the outside of the cell is not allowed due to a high potential barrier. Therefore, there are two possible arrangements of electron locations in the cell which determine two possible stable states known as polarization. It is denoted by P. The figures are shown below.

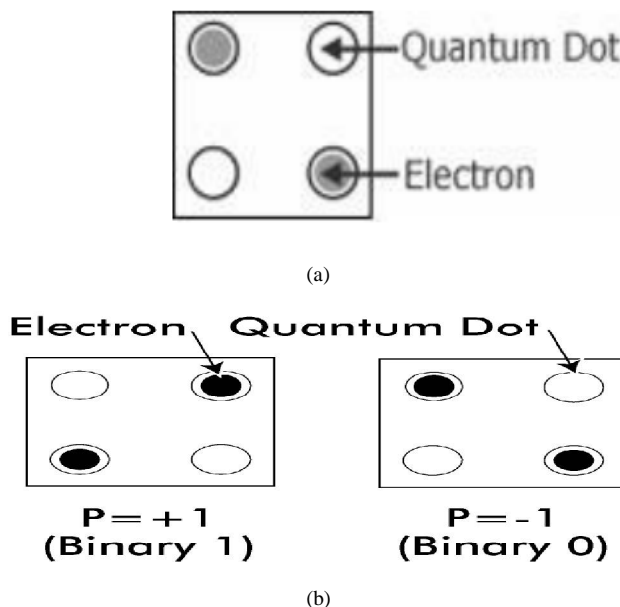


Fig.2.(a) Simplified diagram of QCA(b) Four dot quantum cell

The above figures also show the two possible stable states (minimum energy) QCA cells. Although arbitrarily chosen, using cell polarization,  $P=-1$  represents logic "0" and  $P=+1$  is used to represent logic "1", which become standard practice. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells don't have intrinsic data flow directionality. To achieve controllable data flow directionality, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90 degree. This clock scheme, called the clocking scheme, makes the QCA design intrinsically pipelined as each clock zone behaves like a D-latch [8].

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

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The fundamental logic gates available within the QCA technology are the inverter and the majority gates, which are shown below.

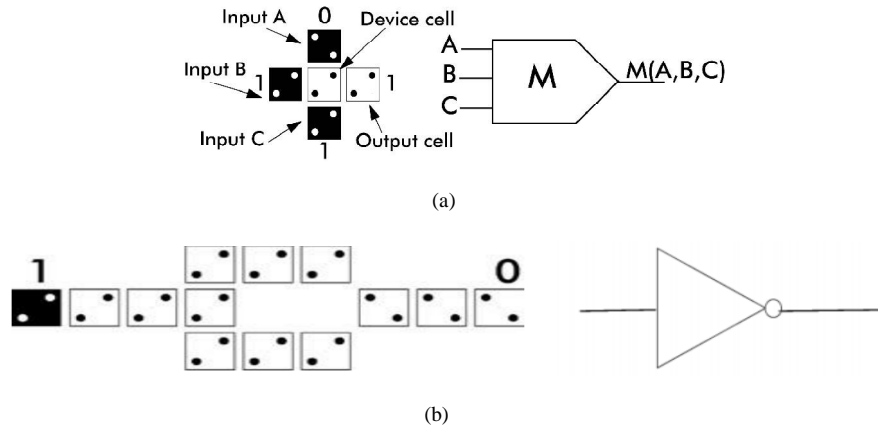


Fig.3. (a) QCA Majority Gate (MG)(b) QCA Inverter

The MG performs a three input logic function. Assuming the inputs are A, B and C, the logic function of the MG is

$$M(A, B, C) = AB + AC + CA \dots \dots \dots (1)$$

### III. EXISTING METHOD

The novel n-bit adder carry chain block and the novel n-bit adder sum block which were implemented for designing the 64-bit adder are shown below.

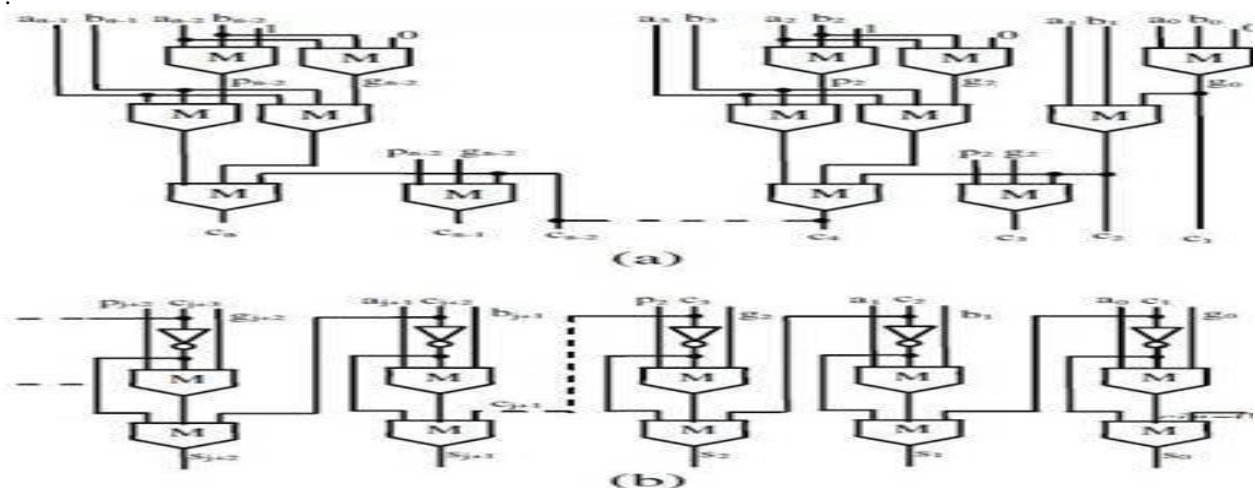


Fig.4. (a) Carry chain (b) Sum chain

The 64-bit QCA full adder as designed previously runs in the RCA fashion. However, it also exhibits some drawbacks. The design fails to compute the input combination (a0 b0 cin) = (010) for 1-bit operation as the computed

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sum gives  $S_0=0$  instead of 1. The drawback of this adder design is also modified for correctness in the new proposed method.

## IV. PROPOSED METHGOD

The improved 64-bit QCA full adder runs in the Ripple Carry Adder (RCA) fashion and exhibits a computational delay lower than all the state-of-the-art competitors and achieves the lowest area-delay product (ADP). The QCA consists of  $n$  1-bit full adder for  $n$ -bit input. It is assumed that the initial carry-in is zero. The carry-out generated by the initial 1-bit full adder is given as the carry-in to the next 1-bit full adder and so on.

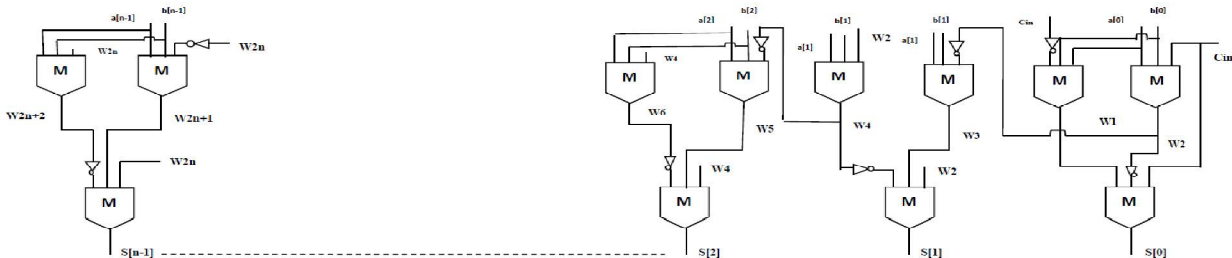


Fig.4. Novel n-bit adder

To implement the RCA in QCA, let us consider two  $n$ -bit addends  $A = a_{n-1}, \dots, a_0$  and  $B = b_{n-1}, \dots, b_0$ .

The MGs perform the logic function given in equation (1) provided that all input cells are associated to the same clock signal  $clk_x$  (with  $x$  ranging from 0 to 3), whereas the remaining cells of the MG are associated to the clock signal  $clk_{x+1}$ .

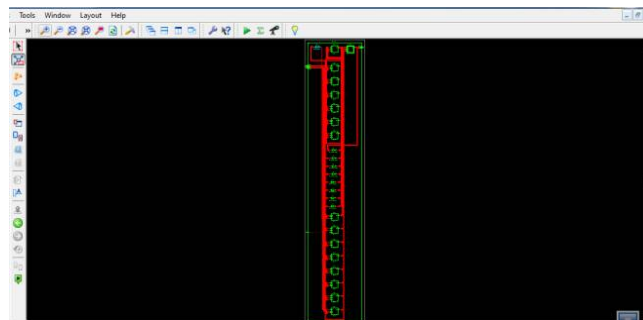


Fig.5. Novel 8-bit adder

The above diagram shows the internal RTL schematic representation of novel 8-bit QCA adder. This can be obtained by using Xilinx. This will act as the building block of novel 16-bit, 32-bit and finally 64-bit adders.

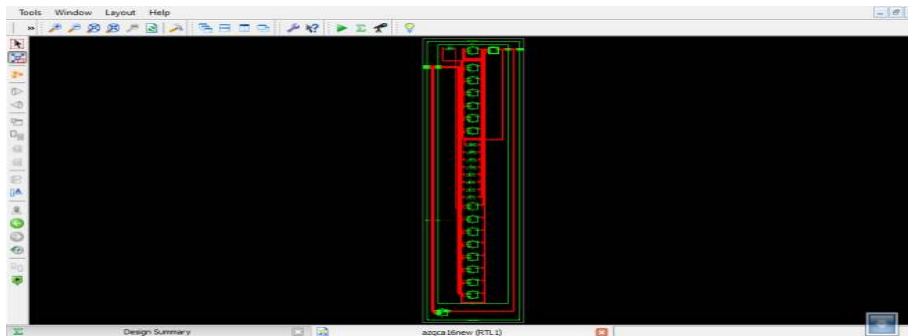


Fig.6.Novel 16-bit adder

There are several adders in QCA available in literature. The RCA [11],[13] and CFA [12] process n-bit operands by cascading n-full bit adders (FAs). Even though these adders exploit different topologies of the generic FA, they have got carry-in to carry-out path consisting of one MG, and carry-in to sum bit path containing two MGs with one inverter. The result is that the worst case computational path of the n-bit RCA and n-bit CFA consist of (n+2) MGs and one inverter. The CLA architecture formed by 4-bit slices was also presented. In particular, the auxiliary propagate ( $p_i$ ) and generate ( $g_i$ ) signals, given as

$$p_i = a_i + b_i \text{ and}$$

$$g_i = a_i \cdot b_i$$

are computed for each bit of the operands and then they are grouped four by four. Such a designed n-bit CLA has computational path composed of  $(7 + 4 \times \log_4 n)$  cascaded MGs along with one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path. Moreover, to compute carry signals, one level of the CLA logic is required for each factor of four in the operands word length. This means that, to process n-bit addends,  $\log_4 n$  levels of CLA logic are required, each contributing to the computational path with four cascaded MGs. Finally, the computation of sum bits introduces two more cascaded MGs and one inverter. The parallel prefix BKA demonstrated exploits more efficient basic CLA logic structures. As its main advantage over the previously described adders, the BKA can achieve lower computational delay. When n-bit operands are processed, its worst case computational path consists of  $4 \times \log_4 n - 3$  cascaded MGs and one inverter. Apart from level required to compute propagate and generate signals, the prefix tree consists of  $2 \times \log_4 n - 2$  stages.

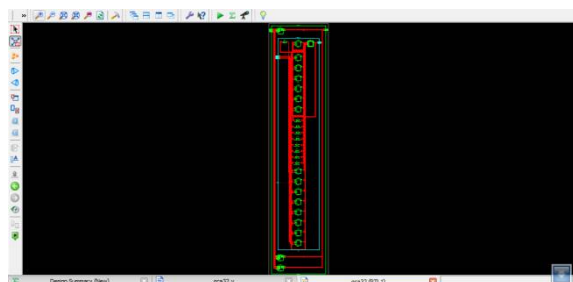


Fig.7.Novel 32-bit adder

From the logic equations provided, it can be easily verified that the first stage of the tree introduces one MG in the computational path; the last stage of the tree with only one MG and the intermediate stages introduce two cascaded MGs in the critical path. Lastly, for the computation of the sum bits, further two cascaded MGs and one inverter are added. With the main objective of trading off area and delay, the hybrid adder (HYBA) described combines a parallel

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prefix adder with the RCA. In the presence of n-bit operands, this architecture has a worst computational path containing of  $2 \times \log_4(n + 2)$  cascaded MGs and one inverter. When the methodology recently proposed was exploited, the worst case path of the CLA is reduced to  $4 \times \log_4 n + 2 \times \log_4 n - 1$ MGs and one inverter. The above mentioned approach can be applied to design the BKA. In this case, the overall area is reduced with respect to, but maintaining the same computational path. By applying the decomposition method demonstrated, the computational path of the CLA and CFA are reduced to  $7 \times 2 \times \log_4(n/8)$  MGs and one inverter and to  $\left(\frac{n}{2}\right) + 3$  MGs and one inverter respectively.

### V. EXPERIMENTAL RESULTS

The proposed adder design architecture is implemented for several operands word lengths using the QCA Designer tool by adopting the same rules and simulation results used.

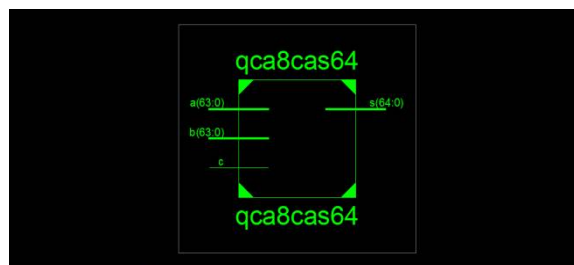


Fig.8. Block Diagram

The above diagram shows the block diagram of novel 64-bit adder. This is obtained with the help of Xilinx. The novel 64-bit QCA adder is designed by cascading eight 8-bit QCA adders.

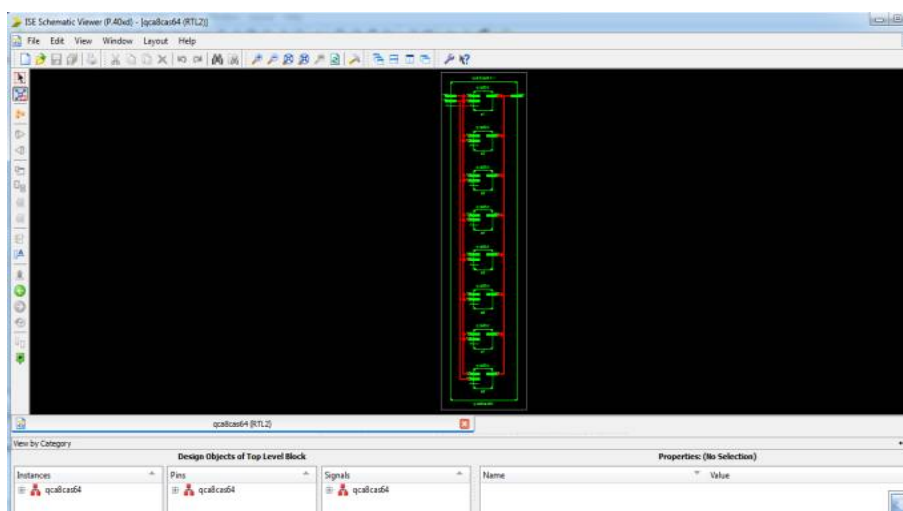


Fig.9. RTL Schematic

The above figure shows the internal RTL Schematic of novel 64-bit QCA adder. As stated above, this can be obtained by using Xilinx. It is clearly seen that the 8-bit QCA adders are being cascaded to provide the necessary design of novel 64-bit QCA adder.

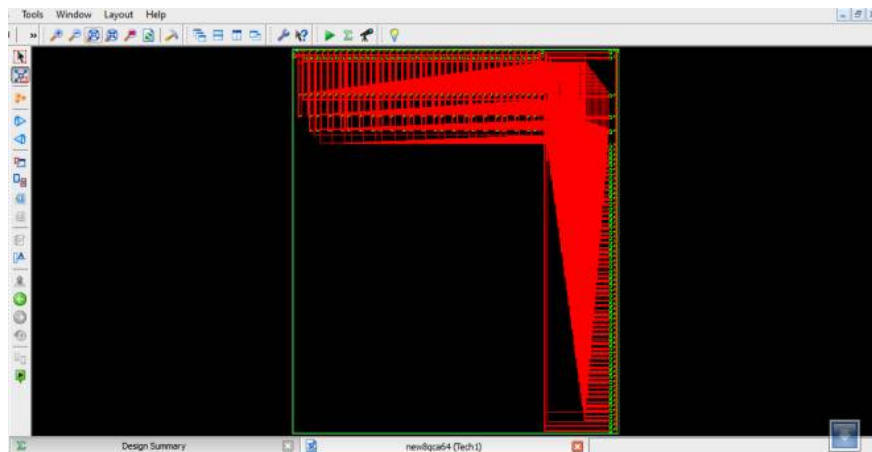


Fig.12. Technology Schematic

The above figure shows the technology schematic of novel 64-bit QCA adder. This can also be obtained by using Xilinx. The operation of this can be explained with the help of above RTL schematic.

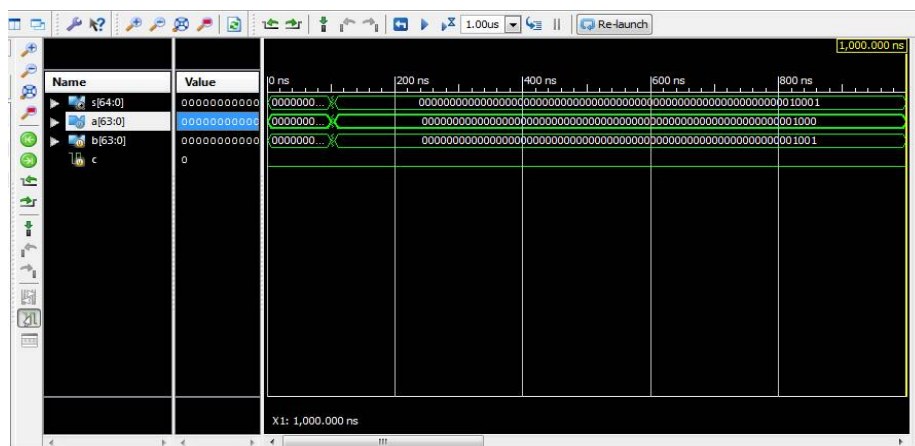


Fig.13. Simulation Output

The above figure shows the simulation output for 64 bit adder. The simulation result shows that the 64 bit QCA adder calculates the amount of delays and it reduces the number of cell count as well.

## VI. CONCLUSION

The new 64-bit designed in QCA was implemented. The drawback incurred in the previous design was successfully removed and rectified. It also achieved speed performances higher than all the QCA adders of the same bit span, with an area requirement comparable with the cheap RCA and CFA demonstrated. In addition, the number of majority gates (MGs) is also reduced, thus increasing cheap computational capabilities. Moreover, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. The 64-bit binary adder designed is described in this brief.

## REFERENCES

- [1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum cellular automata," *Nanotechnology*, vol.4, no. 1, pp. 49–57, 1993.

## International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

- [2] University of Notre Dame, Dept. of electrical engineering. Web: <http://www.nd.edu/qcahome/>
- [3] K. Walus and G. A. Jullien, "Design tools for an emerging SoC technology: Quantum-dot cellular automata," Proc. IEEE, vol. 94, no. 6, pp. 1225–1244, Jun. 2006.
- [4] Lent C. S. and Tougaw P.D., "Lines of interacting quantum-dot cells: a binary wire", Journal of applied Physics, vol. 74, pp: 6227-33, 1993.
- [5] Askari, M., M. Taghizadeh, Kh. Fardad, "Digital Design using Quantum-Dot Cellular Automata (A Nanotechnology Method)," in Proc. International Conference on Computer and Communication Engineering, pp. 952-955, 2008.
- [6] Askari, M., M. Taghizadeh, Kh. Fardad, "Design and Analysis of a Sequential Ring Counter for QCA Implementation," in Proc. International Conference on Computer and Communication Engineering, pp. 933-936, 2008.
- [7] A.Choudhury, D.Z.Chen, X.S.Hu and M.T. Niemer, "Fabricable interconnect and molecular QCA circuits." IEEE Trans. Comput. Aided design Integr. Circuit syst., vol.26,no.11,pp. 1977-1991.
- [8] J.D.Wood and D.Tougaw, "Matrix multiplication using quantum-dot cellular automata to implement conventional microelectronics," IEEE Trans. Nanotechnol. , vol. 10, no. 5, pp. 1036–1042, Sep. 2011.
- [9] W. Liu, L. Lu, M. O'Neill, and E. E.Swartzlander, Jr. "Design rules for quantum-dot cellular automata," in Proc. IEEE Int. Symp. Circuits Syst. , May 2011, pp. 2361–2364.
- [10] K. Kim, K. Wu, and R. Karri, "Toward designing robust QCA architectures in the presence of sneak noise paths," in Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit. , Mar. 2005, pp. 1214–1219.
- [11] Cho, H., E.E. Swartzlander, "Adder Designs and Analyses for Quantum-Dot Cellular Automata," IEEE Transactions on Nanotechnology, vol. 6(3), pp. 374-383, 2007.
- [12] H.Cho and E.E.Swartzlander, "Adder design and multiplier design in quantum-dot cellular automata", IEEE trans.Comput., vol.58, no.6, pp.721-727, Jan.2012.
- [13] V. Pudi and K. Sridharan, "Low complexity design of ripple carry and Brent–Kung adders in QCA," IEEE Trans.Nanotechnol., vol. 11, no.1, pp. 105–119, Jan. 2012.
- [14] V. Pudi and K. Sridharan, "Efficient design of a hybrid adder in quantum dot cellular automata," IEEE Trans. Very Large Scale Integr.(VLSI) Syst., vol.19, no. 9, pp. 1535–1548, Sep.2011.
- [15] M. Janez, P. Pecar, and M. Mraz, "Layout design of manufacturable quantum-dot cellular automata," Microelectron. J., vol. 43, no. 7, pp.501–513, 2012.