

An Efficient Realization Area-Time with Multi Constant Multiplications for Low Power Design

M. Hymavathi¹, TayyabUnnissa Begum²

Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India^{1,2}

ABSTRACT:In this paper, critical path of multiple constant multiplication (MCM) block is analysed precisely and optimized for high-speed and low-complexity implementation. A delay model based on signal propagation path is proposed for more precise estimation of critical path delay of MCM blocks than the conventional adder depth and the number of cascaded full adders. A dual objective configuration optimization (DOCO) algorithm is developed to optimize the shift-add network configuration to derive high-speed and low-complexity implementation of the MCM block for a given fundamental set along with a corresponding additional fundamental set. A genetic algorithm (GA)-based technique is further proposed to search for optimum additional fundamentals. In the evolution process of GA, theDOCO is applied to each searched additional fundamental set to optimize the configuration of the corresponding shift-add network.

KEYWORDS:Efficient Distributed Arithmetic (DA), Finite Impulse Response (FIR), Look-up-table (LUT)

I. INTRODUCTION

There are many hand-held products that include digital signal processing (DSP), for example, cellular phones and hearing aids. For this type of portable equipment a long battery life time and low battery weight is desirable. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift addition architecture where each constant multiplication is realized using addition/subtraction and shift operations in an MCM operation For the shift-adds implementation of constant multiplications, a straightforward method, generally known as digit based run at the gate level. In this paper, we initially determine the gate-level implementation costs of digit-serial addition, subtraction, and left shift operations used in the shift adds design of digit-serial MCM operations. Then, we introduce the exact CSE algorithm that formalizes the gate-level area optimization problem as a 0–1 integer linear programming (ILP) problem when constants are defined under a particular number representation. We also present a new optimization model that reduces the 0–1 ILP problem size significantly and, consequently, the runtime of a generic 0–1 ILP solver. Since there are still instances which the exact CSE algorithm cannot handle, we describe the approximate GB algorithm that iteratively finds the “best” partial product which leads to the optimal area in digit-serial MCM design at the gate level.

II. RELATED WORK

R. Pasko, P. Schaumont, V. Derudder, S. Vernalde, and D. Durackova, “A new algorithm for elimination of common subexpressions,” IEEE Trans. Comput.-Aided Design Integr. Circuit Syst., vol. 18, no. 1, pp. 58–68, Jan. 1999.

The problem of an efficient hardware implementation of multiplications with one or more constants is encountered in many different digital signal processing areas, such as image processing or digital filter optimization. In a more general form, this is a problem of common subexpression elimination, and as such it also occurs in compiler optimization and many high-level synthesis tasks. An efficient solution of this problem can yield significant improvements in important

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

design parameters like implementation area or power consumption. In this paper, a new solution of the multiple constant multiplication problem based on the common subexpression elimination technique is presented. The performance of our method is demonstrated primarily on a finite-duration impulse response filter design. The idea is to implement a set

of constant multiplications as a set of add-shift operations and to optimize these with respect to the common subexpressions afterwards. We show that the number of add/subtract operations can be reduced significantly this way. The applicability of the presented algorithm to the different high-level synthesis tasks is also indicated. Benchmarks demonstrating the algorithm's efficiency are included as well.

F. Xu, J. J. Chen, C. H. Chang, and C. C. Jong, "A modified reduced adder graph algorithm for multiplier block minimization in digital filters," in Proc. IEEE Asia-Pacific Conf. Circuits Syst., Dec.2004, vol. 2, pp. 705–708.

A modified reduced adder graph (MRAG) Algorithm and its hybrid variant are proposed for effective digital filter implementation. A few upgrades are made to exploit absolutely the efficient surest part of the n-dimensional decreased adder graph (RAG-n) algorithm. Simulation results display MRAG is in a position of generating cut back adder rate.

Y. Pan and P. K. Meher, "Bit-level optimization of adder-trees for multiple constant multiplications for efficient FIR filter implementation," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 2, pp. 455–462, Feb. 2014.

Multiple constant multiplication (MCM) scheme is widely used for implementing transposed direct-form FIR filters. While the research focus of MCM has been on more effective common sub expression elimination, the optimization of adder-trees, which sum up the computed sub-expressions for each coefficient, is largely omitted. In this paper, we have identified the resource minimization problem in the scheduling of adder-tree operations for the MCM block, and presented a mixed integer programming (MIP) based algorithm for more efficient MCM based implementation of FIR filters. Experimental result shows that up to 15% reduction of area and 11.6% reduction of power (with an average of 8.46% and 5.96% respectively) can be achieved on the top of already optimized adder/subtractor network of the MCM block.

Multiple constant multiplications: efficient and versatile framework and algorithms for exploring common subexpression elimination Author: Potkonjak, M. Srivastava, M.B.; Chandrakasan, A.P.

Many applications in DSP, telecommunications, graphics, and control have computations that either involve a large number of multiplications of one variable with several constants, or an easily be transformed to that form. A proper optimization of this part of the computation, which we name the more than one consistent multiplication (MCM) quandary, mostly results in a huge development in a couple of key design metrics, such as throughput, subject, and energy. Nevertheless, until now little awareness has been paid to the MCM predicament.

Multiple constant multiplication (MCM) constitutes a typical fixed-point arithmetic operation in digital signal Processing. It is the focus of a lot of research on high-speed and low power devices in communication systems and signal processing systems. In multiplier less MCM, multipliers are replaced by simpler components such as adders and hard-wired shifts (adders in our paper include also subtractors as their hardware costs are similar). By using the Negative digits (subtractor in circuit) in their signed digit representations, coefficients may be synthesized with fewer adders; therefore the area and power consumption of the circuit can be reduced. An example of a multiplier-based and a multiplier less based MCM implementations respectively, wherein 4 multiplications are replaced by 6 adders and 6 hardwired shifts. Such Multiplier less MCMs are utilized, for example, in the design of finite-impulse response Filters.

III. PROPOSED SYSTEM

The optimization of gate-level area problem in digit-serial MCM design is an NP-complete problem due to the NP-completeness of the MCM problem. Thus, naturally, there will be always 0–1 ILP problems generated by the exact

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

CSE algorithm that current 0–1 ILP solvers find difficult to handle. Hence, the GB heuristic algorithms, which obtain a good solution using less computational resources, are indispensable. In our approximate algorithm called MINAS-DS, as done in algorithms designed for the MCM problem given in Definition 1, we find the fewest number of intermediate constants such that all the target and intermediate constants are synthesized using a single operation. However, while selecting an intermediate constant for the implementation of the not yet synthesized target constants in each iteration, we favour the one among the possible intermediate constants that can be synthesized using the least hardware and will enable us to implement the not-yet synthesized target constants in a smaller area with the available constants.

After the set of target and intermediate constants that realizes the MCM operation is found, each constant is synthesized using an A-operation that yields the minimum area in the digit-serial MCM design. The area of the digit-serial MCM operation is determined as the total gate-level implementation cost of each digit-serial addition, subtraction, and shift operation under the digit size parameter d as described above. The preprocessing phase of the algorithm is the same as that of the exact CSE algorithm, and its main part and routines are given. The right shift of an A-operation is assumed to be zero as shown in fig.1.

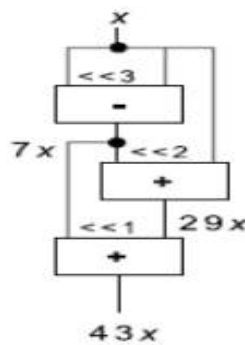


Fig.1

IV. DESIGN AND IMPLEMENTATION

Multiple Constant Multiplication (MCM) is an arithmetic operation that multiplies a set of fixed point constants with the same fixed-point variable X . From a circuit point of view, MCM dominates the complexity of the whole category of Linear Time Invariant (LTI) systems, such as, FIR/IIR filters, DSP transforms (DCT, DFT, Walsh, etc), LTI controllers, Crypto-systems, etc. To be efficiently implemented, MCM must avoid costly multipliers. The hardware alternative must be multiplier less, i.e., using only additions, subtractions, and shifts. Therefore, the MCM problem is defined as the process of finding the minimum number of addition/subtraction operations. The computational complexity of MCM is conjectured to be NP-hard.

In some applications such as linear transformations and transposed form finite impulse response (FIR) filters as illustrated in figure of acyclic graph the same variable is multiplied by a set of constant coefficients, which are known a priori. Such structures are referred to as multiple constant multiplications (MCM). Efficient implementation of MCM is important for high-speed, low-complexity and low-power DSP systems. Typically the multiplications in an MCM block are realized by a network of adders (subtractors) and hardwired shifts with sharing of partial products across all the multiplications. The MCM problem is extensively studied and many different algorithms have been proposed by researchers to optimize the area consumption and computation time of the MCM block. All these approaches can be put into two broad categories:

- i) Common sub expression elimination (CSE) technique proposed by Hartley , and
- ii) The graph-dependence (GD) algorithms.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

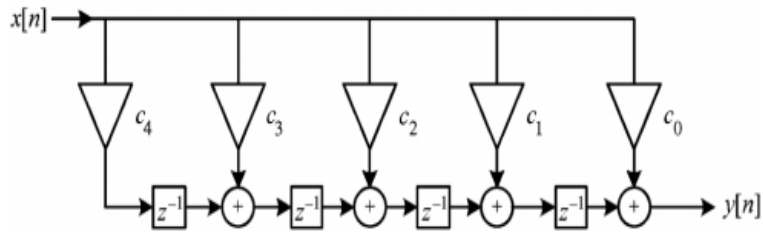


Fig.2: Transposed structure of a FIR filter with 5 coefficients

The GD algorithms share the same optimal part and use different criteria to determine additional fundamentals. While the earlier GD algorithms, focus on reducing the number of additional fundamentals (i.e., word-level adders), in some recent works, the bit-level information of word-level adders has been taken into consideration to minimize the number of full adders. To optimize the bit-level complexity suggest a two-step design path as shown in Fig.4. Besides finding the additional fundamentals as those word-level techniques, the interconnection of DAG, referred to as shift-add network configuration (second step in Fig.4), is further optimized to minimize the FA cost.

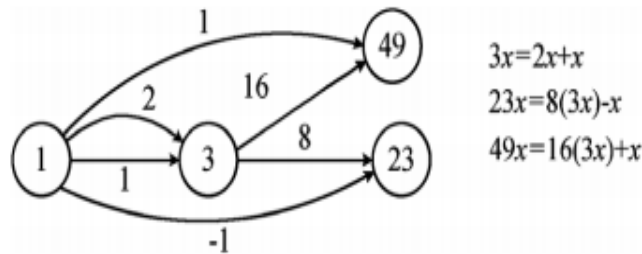


Fig. 3. Directed acyclic graph of constants multipliers of 23 and 49

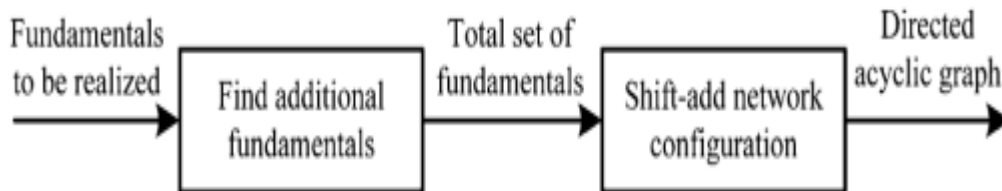


Fig. 4. Design path of MCM optimization at bit-level

We propose hereafter a new MCM algorithm, called RADIX-2r, for it is essentially based on the radix-2r arithmetic. It has the merit over the existing MCM algorithms of being:

A-Operation: In this section, the bit-level complexity model for the MCM problem based on operation is discussed and the shift-add network configuration optimization technique for reducing hardware complexity is introduced. Prior to that, the definition of operation is reviewed for the convenience of readers. The notation of operation was first

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

introduced in for a parameterized representation of adds, subtracts and shifts for MCM implementation. The formal definition of operation is as follows

$$A_p(u, v) = |2^{l_1} + (-1)^s 2^{l_2} v| 2^{-r} \dots \dots \dots (1)$$

Where u and v are two previously realized fundamentals. $p=\{ l_1, l_2, r, s\}$ is the parameter set, where l_1, l_2 are respectively, the bit positions through which and are shifted to left, r is the bit positions through which and both are shifted to right, and s indicates if the shifted fundamentals are added or subtracted.

In the MCM problem, there are only two kinds of possible operations: i) one of the input fundamentals, say, is left shifted by one or more bit positions, while the value of the other input fundamental does not change (otherwise the result is not odd). ii) Both input fundamentals and are right shifted with the same amount of bit positions. This constraint can be expressed as:

$$\begin{aligned} l_1 > 0, l_2 = r = 0 \\ l_1 = l_2 = 0, r > 0 \end{aligned} \dots \dots \dots (2)$$

B. Bit-Level Complexity Model

In this paper, we use the sign transformation technique of [21] to eliminate half adders in subtract operations. Half adders used for the last bit of word-level adders are counted as full adders. The number of full adders, denoted as N_{fa} needed to realize an adder in the multiplier block is estimated to be:

$$\begin{aligned} N_{fa} &= \lceil \log |f_i| \rceil - l_1 + w_{in} \text{ for } l_1 > 0, l_2 = r = 0 \\ &= \lceil \log |f_i| \rceil + w_{in} \text{ for } l_1 = l_2 = 0, r > 0 \dots \dots \dots (3) \end{aligned}$$

where f_i is the fundamental to be realized, and w_{in} is the word length of the input to the multiplier block. The total number of full adders needed to implement the MCM block, denoted as $Total\ FA = \sum_{i=1}^n N_{fa}$, where n is the number of word-level adders.

C. Optimization of Shift-Add Network Configuration for Reduction of Hardware Complexity

In the following example we show that the shift-add network configuration of the DAG can be optimized to reduce the FA cost. Supposing that an 8-bit input is multiplied by a coefficient set $\{3, 13\}$ using a shift-add network, there are 4 different options to realize the MCM block as shown in Fig. 5. The FA costs for DAGs of (a), (b), (c), and (d) are 17, 16, 19, and 18, respectively. Different shift-add network configurations result in different FA costs.

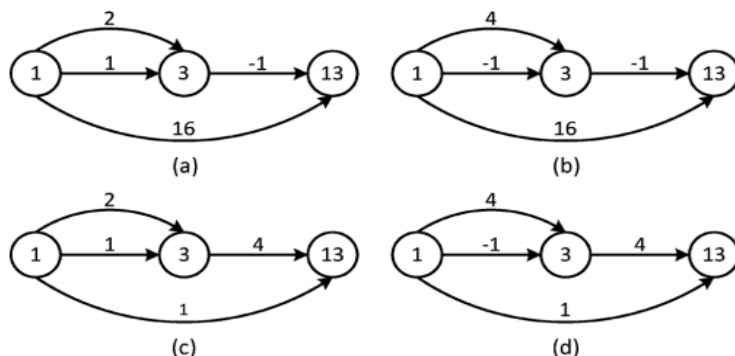


Fig. 5. Different ways to implement coefficient set $\{3, 13\}$.

V. SIGNAL PROPAGATION PATH BASED CRITICAL PATH OPTIMIZATION

Here a fine-grained signal propagation path based delay model is proposed for the analysis of critical path of MCM blocks. Thereafter, a shift-add network configuration optimization scheme is developed for reducing CPD as well as hardware complexity.

Let us take the full adder in Fig. 6(a) as an example. From the implementation perspective of a full adder, the input signals from and to the outputs and travel through different paths. This results in different intrinsic delays for different signal paths. Furthermore, the loads driven by the outputs of a full adder impact the delays as well. Thus, instead of assuming the computation time of the sum and carry out to be the same, we treat the delays of different signal paths in a full/half adder individually. In order to have a realistic estimation, the two consecutive adder structure shown in Fig. 6(b) is used to estimate the delays of different signal paths of full/half adders. This consecutive addition is a typical operation in a MCM block.

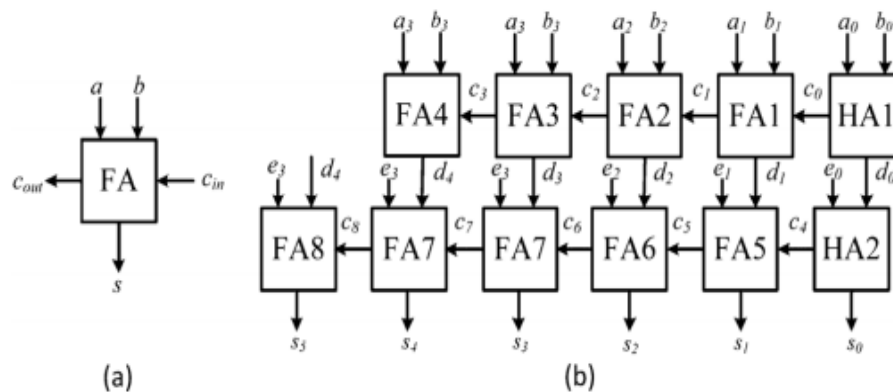


Fig. 6. (a) Full adder. (b) Two consecutive additions.

VI. CONCLUSION

In this project, the critical path of MCM blocks are analysed based on the signal path and a fine-grained delay model for CPD estimation is proposed. Based on this precise estimate of path, we proposed an algorithm named DOCO to optimize the shift-add network configuration of MCM blocks for the reduction of CPD and hardware complexity subject to an additional fundamental set. In this order to find the optimum additional fundamentals for a given fundamental set, a GA-based search method is proposed. The DOCO algorithm is adopted in the proposed GA-based technique to optimize the shift add network configurations.

REFERENCES

- [1] Y. Voronenko and M. Püschel, "Multiplierless multiple constant multiplication," *ACM Trans. Algorithms*, vol. 3, no. 2, p. 11, Sep. 2007.
- [2] R. Pasko, P. Schaumont, V. Derudder, S. Vernalde, and D. Durackova, "A new algorithm for elimination of common subexpressions," *IEEE Trans. Comput.-Aided Design Integr. Circuit Syst.*, vol. 18, no. 1, pp. 58–68, Jan. 1999.
- [3] M. M. Peiro, E. I. Boemo, and L. Wanhammar, "Design of high-speed multiplierless filters using a nonrecursive signed common subexpression algorithm," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.* vol. 49, no. 3, pp. 196–203, Mar. 2002.
- [4] F. Xu, C. H. Chang, and C. C. Jong, "Contention resolution algorithm for common subexpression Wiley. elimination in digital filter design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 10, pp. 695–700, Oct. 2005.
- [5] F. Xu, C. H. Chang, and C. C. Jong, "Contention resolution algorithm for common subexpression elimination in digital filter design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 10, pp. 695–700, Oct. 2005.
- [6] O. Gustafsson and L. Wanhammar, "Ilp modelling of the common subexpression sharing problem," in *Proc. IEEE 9th Int. Conf. Electron., Circuits Syst.*, Sep. 2002, vol. 3, pp. 1171–1174.
- [7] A. Yurdakul and G. Dundar, "Multiplierless realization of linear DSP transforms by using common two-term expressions," *J. VLSI Signal Process.*, vol. 22, pp. 163–172, Sep. 1999.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

[8] L. Aksoy, E. da Costa, P. Flores, and J. Monteiro, "Exact and approximate algorithms for the optimization of area and delay in multiple constant multiplications," IEEE Trans. Comput.-Aided Design Integr. Circuit Syst., vol. 27, no. 6, pp. 1013–1026, Jan. 2008.

BIOGRAPHY



M. Hymavathi presently, working as Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India. Her research interests are in area of low power VLSI, FPGA architectures.



TayyabUnnissa Begum presently, working as Assistant Professor, Department of ECE, Lords Institute of Engineering and Technology, Telangana, India. Her research interests are in area of low power VLSI, FPGA architectures.