

Fault Tolerant Parallel Filters with Efficient Addition Structure

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ABSTRACT: In today's world there's an excellent need for the design of low power and area efficient high performance DSP system. FIR filter is taken into account to be the elemental device within the broad application of wireless in addition because the video and image processing system. With the aim of obtaining the reliable operation, these filters are protected exploitation the Error correction Code. The pipelined FIR filter design that reduces the critical path by interleaving the pipelined latches on the datapath, with the sense of accelerating the quantity of latches then the system latency. However the parallel processed FIR filter design will increase the sample rate thereby replicating the hardware, so the multiple range of inputs gets processed parallelly and at identical time generating multiple varieties of outputs with the disadvantage of magnified space within the design. To overcome this disadvantage and within the sense of holding these advantage of multiprocessing, the hardware economical filter structure is to be proposed, and these filter structure is to be recovered from error by the application of Error Correction Code.

KEYWORDS: FIR filter, Error Correction Code, Parallel Processing.

I. INTRODUCTION

Finite impulse response (FIR) digital filters are common parts in several digital signal processing (DSP) systems. Throughout the years, with the progressively development in terribly large scale integration (VLSI) technology, the real time realization of FIR filter with less hardware demand and fewer latency has become more and more important. as a result of the complexness of implementation grows with the length of filter, many algorithms are created to develop effective architectures for realization of FIR filters in application specific integrated circuits (ASIC) and field programmable gate arrays (FPGA) platforms and one in all them is error robust design. The most portion of error tolerant -based FIR computation is parity blocks that stores the precomputed values and might be read out simply, that makes FIR computation compatible for FPGA realization, as a result of the memory is that the basic parts of FPGA.

Moreover, this technology represents variety of attractive features like simplicity, regularity and modularity of design. Also, the error detection technique is designed to meet various speed requirements, as an example, it is designed for high-speed implementation wherever all bits of one word are processed per clock, it can even be designed for medium-speed implementation wherever many bits of one word (not all bits) are processed per clock. In recent years, fault tolerant-based FIR filter has gained substantial quality as a primary DSP operation and are rapidly replacement classic analog filters.

II. RELATED WORK

Triple Modular Redundancy has three identical logic circuits (logic gates) are used to compute the specified Boolean function. The set of data at the input of the first circuit are identical to the input of the second and third gates. In computing, triple modular redundancy, sometimes called triple-mode redundancy. TMR is a fault-tolerant form of N-modular redundancy, in which three systems perform a process and that result is processed by a majority-voting system to produce a single output.

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If any one of the three systems fails, the other two systems can correct and mask the fault. The TMR concept can be applied to many forms of redundancy, such as software redundancy in the form of N-version programming, and is commonly found in fault-tolerant computer systems. Some ECC memory uses triple modular redundancy hardware (rather than the more common Hamming code), because triple modular redundancy hardware is faster than Hamming error correction software.

The existing pipeline filter structure is shown in the Fig.1. This filter structure is designed for four input and four filter coefficients. The four filters are considered to be x_1, x_2, x_3 and x_4 and the filter coefficients are found to be h_0, h_1, h_2 and h_3 . The output generated will be y_1, y_2, y_3 and y_4 .

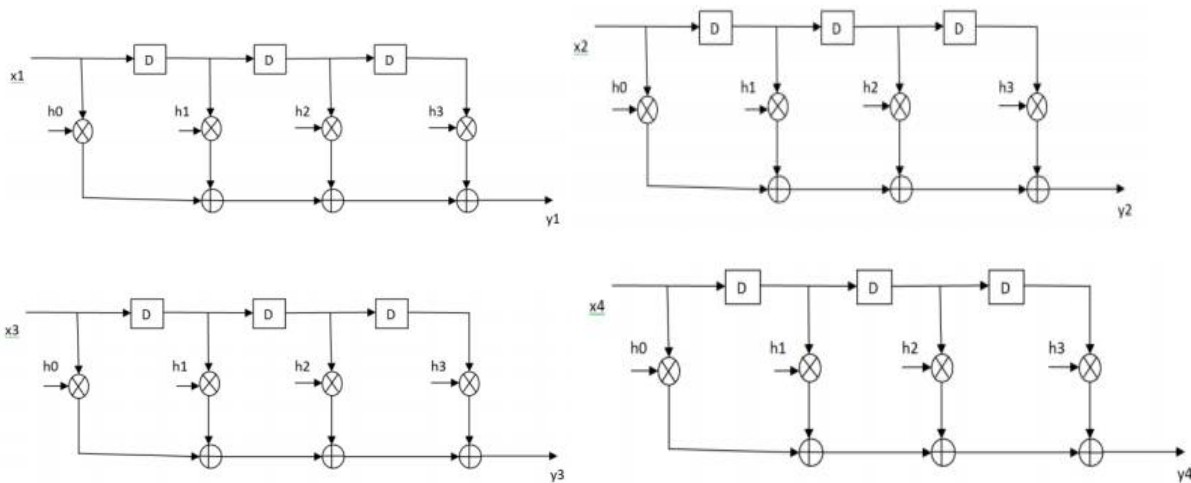


Fig.1 Four filter pipelined structure

A. Original Module

The original module should be represented in the Fig.1. In this module the applied input gets convoluted by using its filter coefficients then it generates the convoluted output.

B. Redundant Module

The redundant module is the module used for achieving the reliable operation over the original module. The redundant module is said to be the parity module which is used to generate the parity bits. These parity bits are represented as z_1, z_2, z_3 . The module takes a block of k bits and generated the block of n bits and the parity is obtained as $n-k$ bits.

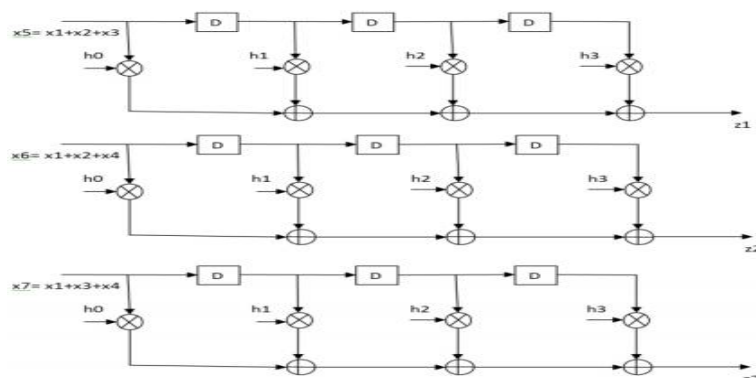


Fig.2

III. PROPOSED SYSTEM

The proposed filter structure has a difference in the adder structure implementation as compared with the existing pipeline structure. This efficient adder structure implementation in the pipelined filter is given in the Fig.4. below.

A. Original Module

The original module is represented in the Fig.4. In this module the applied input gets convoluted by using the efficient adder structure. The original module is represented in same Fig.3.

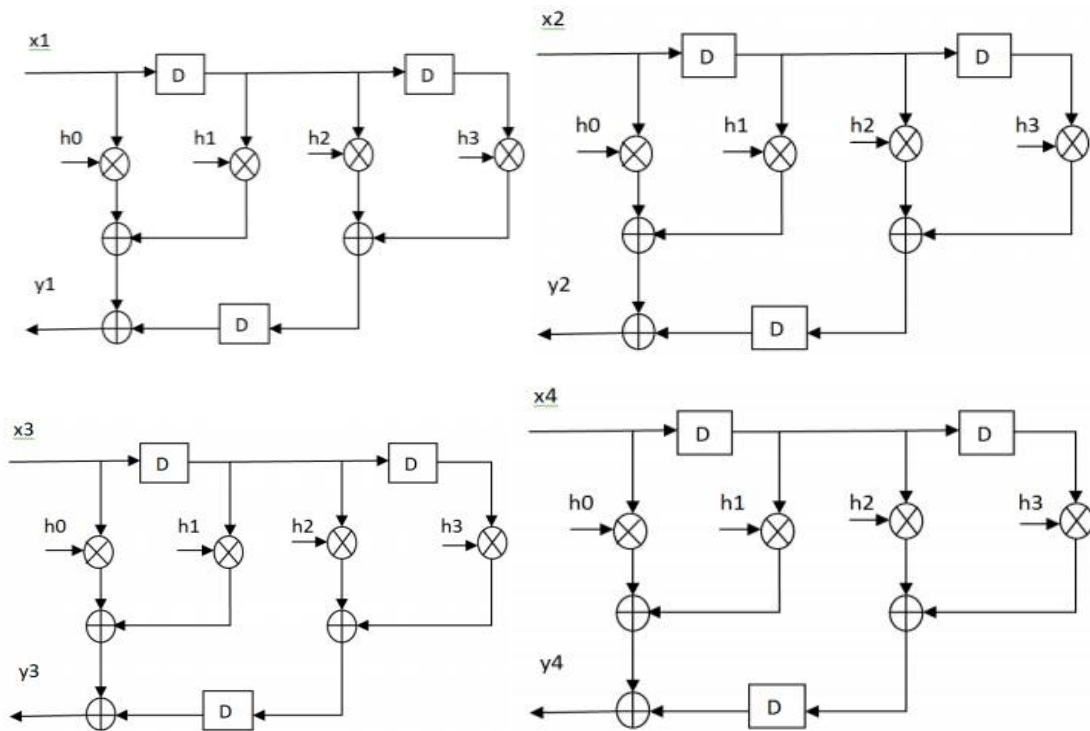


Fig.3. Proposed Efficient Adder Pipelined Structure

B. Redundant Module

The redundant module is same as that of the existing systems redundant module used for achieving the reliable operation over the main module. This module is used for generating the parity bits also represented as z1, z2 and z3. The parity is calculated as n-k bits.

Let us consider a simple example of Hamming code with k=4 and n=7, here the parity bits p1, p2 and p3 are computed based on the data bits d1, d2, d3 and d4 as follows:

$$\begin{aligned}
 p1 &= d1 \oplus d2 \oplus d3 \\
 p2 &= d1 \oplus d2 \oplus d4 \\
 p3 &= d1 \oplus d3 \oplus d4
 \end{aligned}$$

The redundant module for the proposed system is shown in the Fig.5.

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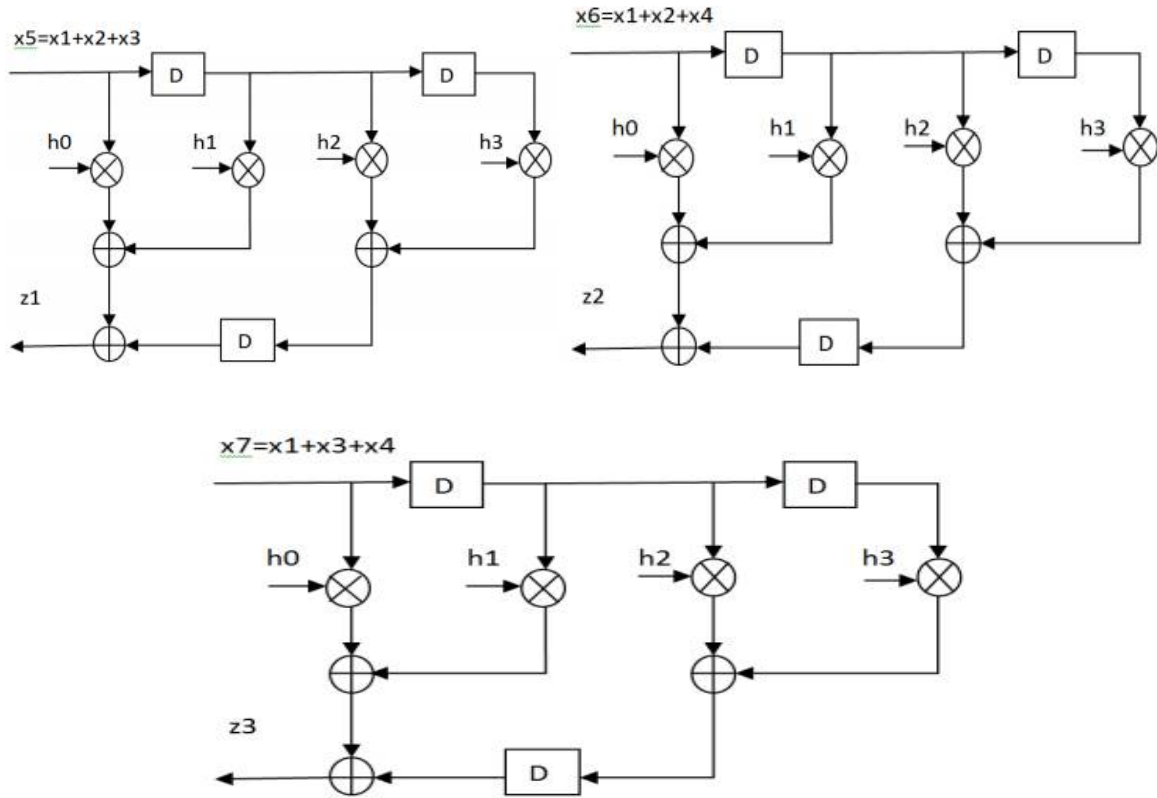


Fig.4. Proposed Redundant Module

C.Single Error Correction Module

The single error correction module is used to correct the single bit error in the generated convoluted output at the proposed areaefficient adder structure. The single error correction module is shown in the Fig.5.

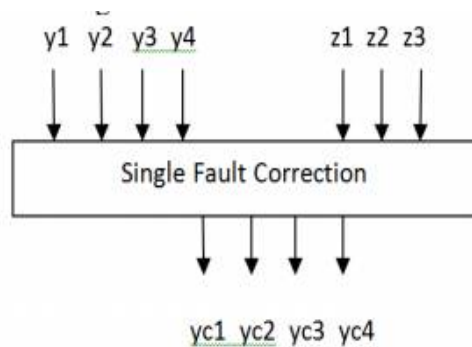


Fig.5 Proposed Single Error Correction Module

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IV. SIMULATION RESULTS

The Simulation results and the RTL schematic for the existing and proposed module are given below:

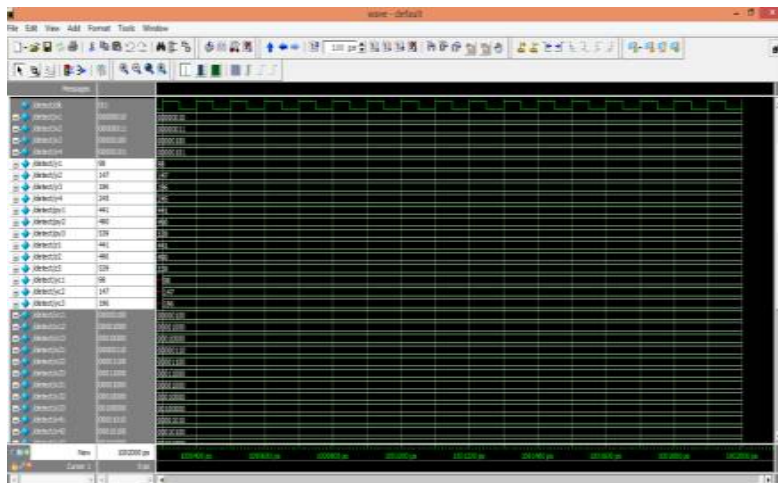


Fig.6. Simulation result for the Existing system

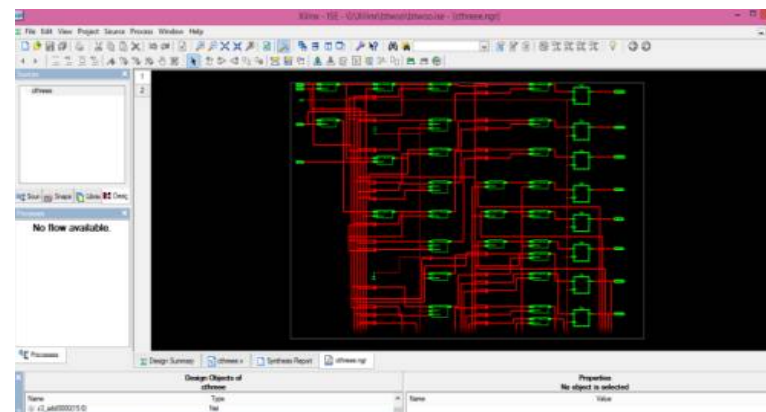
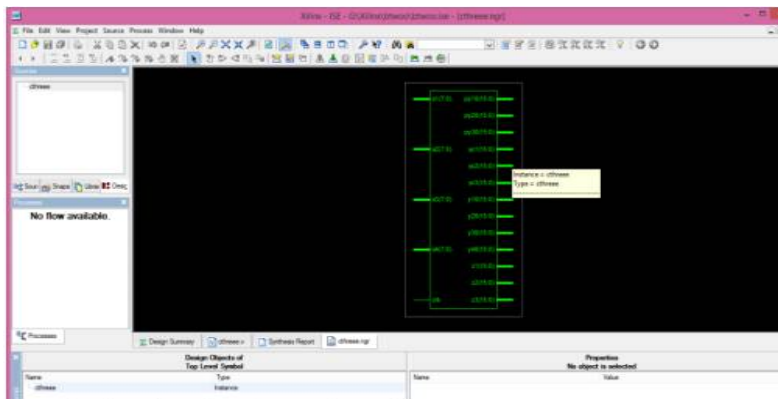


Fig.7. RTL schematic view proposed filter structure

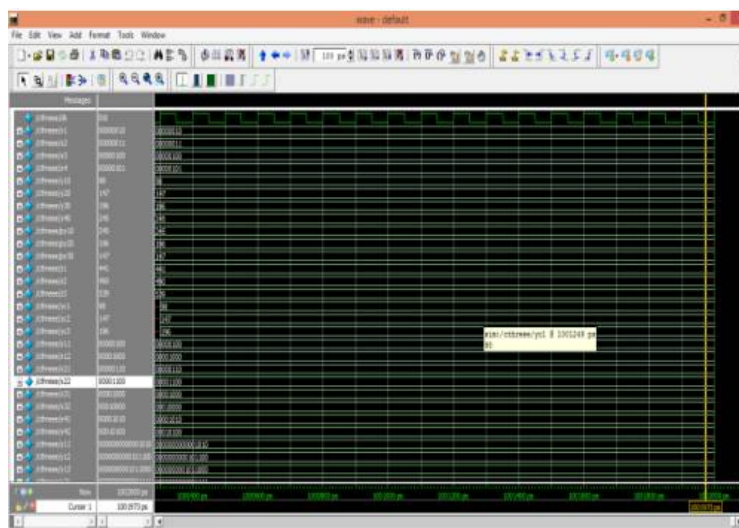


Fig.8.Simulation Result of proposed system

V. CONCLUSION

In this paper, the Filter is designed with efficient hardware implementation structure for getting the reduced power with reduced hardware cost. The altered filter structure produces the analogous result as that of the existing module. The power consumption should be reduced from 320mW to 312mW. The resource utilization can be obtained by analysing the slices, flipflops, used gate clk's, and IOB's. The single bit error correction is accomplished by using the Hamming Error Correction Code in the proposed system.

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BIOGRAPHY



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