

# Modified Dual Output SEPIC Converter Integrated With Semi-Z-Source Inverter

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**ABSTRACT:** This paper presents a combination of DC-DC Converter and a DC-AC Inverter. The DC-DC Converter employed is a modified dual output SEPIC converter with high static gain. The inverter employed is a low-cost Semi-Z-Source inverter. The configuration employs magnetic coupling in the SEPIC converter which allows the increase of static gain. These semi-Z-source inverters employ the Z-source/quasi-Z-source network and only two active switches to achieve the same output voltage as the traditional voltage-fed full-bridge inverter does. The two active switches of the semi-Z-source inverter are controlled complementarily. The input dc source and the output ac voltage of the semi-Z-source inverter share the same ground, thus leading to less leakage ground current advantages over other non-doubly grounded inverters, such as voltage-fed full-bridge inverter. A revised nonlinear sinusoid pulse width modulation method for a semi-Z-source inverter is also proposed. By using this method, desired duty cycle can be generated to output the sinusoidal voltage. The major advantage of the proposed circuit is its reduced THD (less than 3%). A prototype is built; experimental results are provided to verify and demonstrate the special features of the proposed circuit.

**KEYWORDS:** quasi-Z-source, semi-Z-source, SEPIC converter, voltage multiplier.

## I. INTRODUCTION

The development of a converter-inverter combination is an important research area due to crescent demand for several applications such as SMPS. An application where the proposed converters can be applied is the photovoltaic energy generation in grid-connected systems using the ac module or micro-inverter structure [3]. The usual structure used for high power grid-connected photovoltaic generation is the centralized inverter, where several PV modules are connected in series in order to obtain the dc voltage level necessary for the inverter operation and the energy transference to the grid with low-current harmonic distortion. However, a common problem in this structure is the power losses due to the centralized maximum power point tracking (MPPT), mismatch losses among the PV modules, and generation reduction due to a partial shading of the series-connected PV modules structure, where reduced strings are connected with dc-dc converters with the MPPT algorithm and the output of these dc-dc converters are connected to the inverter input. However, in residential applications, most research is focused on the module-integrated converters where the energy generated by a single PV module is transferred to the grid by a dedicated converter integrated with the PV module [4]. Some of the main advantages of this PV generation structure are the modularity, allowing an easy increase of the installed power, the individual MPPT and reduction of the partial shading and panel mismatching effects, thus improving the energy-harvesting capability.

However, there are some design challenges in an ac module structure as the efficiency improvement, cost reduction, and the reliable operation throughout the module lifetime. An alternative for the ac module implementation is a two-stage topology as presented in Fig. 1. The operation with high efficiency is a problem for the dc-dc converter due to the low input voltage, high input current, high output voltage, and static gain. When a high step-up ratio is necessary for the implementation of the first power stage, the usual solution is the use of isolated dc-dc converters. The transformer turns

ratio allows us to increase the converter static gain. The base topology presented in this paper is a modification of the SEPIC dc–dc converter and the main operation characteristics obtained with this modification comply with the requirements necessary in the high static gain applications.

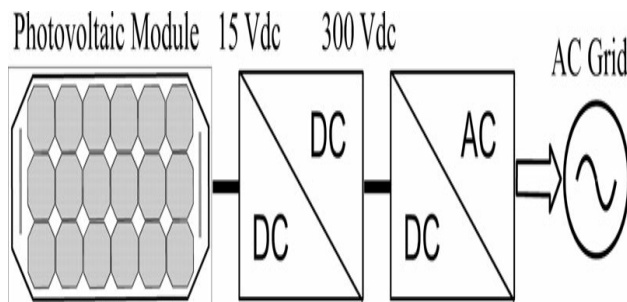


Fig. 1. Two-Stage AC Module Structure

The solution using a magnetic coupling is obtained including a secondary winding in an inductor of the converter, operating as a flyback transformer, increasing the static gain. However, due to the configuration of the power circuit used, the usual problems presented by the single switch isolated dc– dc converter are not presented by this structure with transformer. Only part of the power processed by the converter is transferred to the output through the coupling inductor and another part of the power is transferred directly by the non-isolated converter, reducing the weight, volume, and losses of the transformer. The leakage inductance is a problem for the single-switch isolated dc–dc converters resulting in the switch overvoltage, and the energy stored in the leakage inductance must be dissipated in snubber or clamping circuits. However, the leakage inductance is necessary in the proposed converter with transformer in order to obtain ZCS turn-on commutation and to reduce the diodes reverse recovery current, increasing the converter efficiency. The energy stored in the leakage inductance is transferred to the converter output through the diodes and capacitor of the circuit. The voltages in all semiconductors are clamped by the intrinsic converter operation without dissipative components.

The inverter circuit of the proposed combination can achieve the same output voltage as the traditional voltage-fed full-bridge inverter does, with only two active switches. Recently, many Z-source /modified Z-source single-phase inverters have been proposed for PV, motor drive or UPS applications[5]-[9]. Compared with the traditional single-phase Z-source inverters, the semi- Z-source inverters share the same form of Z-source network. But the Z-source network used in semi-Z-source inverter is in ac side, which is smaller in size than the traditional Z-source network used in dc side. The modulation strategy of the circuit is also different. The traditional Z-source inverters use sinusoidal reference with extra shoot-through reference to output sinusoid voltage and achieve the voltage boost function. However, in order to output sinusoid voltage, the semi-Z-source inverter has to utilize its nonlinear voltage gain curve to generate a modified voltage reference. These differences are the reasons why the author uses the term semi-Z-source inverter to represent the proposed and to distinguish it from the traditional single-phase Z-source inverter. The circuit operation and the modulation strategy of the proposed topology are analysed in detail and verified by the experimental results.

## II. PROPOSED DC-AC CONVERTER

### A. Semi-Z-Source Inverter

Fig. 2 shows the single-phase semi-Z-source and semi-quasi-Z-source inverters based on the different impedance network. The semi-Z-source inverter, as shown in Fig. 2(a), is already discussed in [10]. This paper will concentrate on semi-quasi-Z-source inverter and the PWM control strategy. For the semi-Z-source and quasi-Z-source inverter, only two bidirectional current conducting and unidirectional voltage blocking switching devices, such as insulated gate bipolar transistor (IGBT) and MOSFET, are needed for the operation. Because the voltage gain of the full-bridge inverter is a straight line, the sinusoidal PWM (SPWM) control strategy can be used to output the sinusoid voltage.

Because the voltage gain of the proposed semi-Z-source inverter is not a straight line as the full-bridge inverter, a modified SPWM strategy has to be used in order to output the sinusoid voltage.

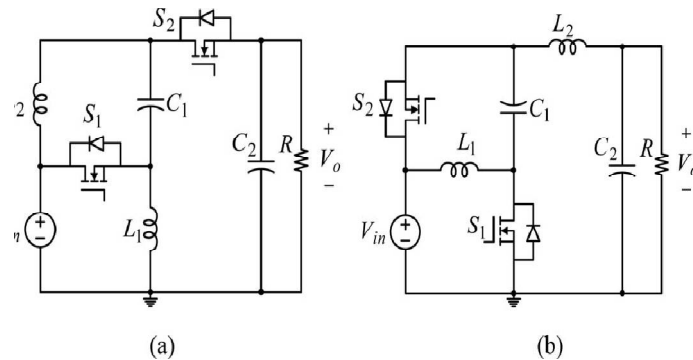


Fig. 2. Proposed single-phase semi-z-source inverters (a) Semi-Z-Source inverter (b) Semi-quasi-Z-Source inverter

Fig. 3 shows the voltage gain curve of the semi-Z-source inverters. The y-axis is the voltage gain of the inverter, and the x-axis is the duty cycle of switch  $S_1$ . Switches  $S_1$  and  $S_2$  are conducted in a complementary manner. By operating switch  $S_1$  with duty cycle changing from 0 to  $2/3$ , the proposed inverters are able to output the same voltage range ( $+V_{in}$  to  $-V_{in}$ ) as the full-bridge inverter, as shown in Fig. 3 with red solid line. When the duty cycle of  $S_1$  changes from (0–0.5), the inverter can output the positive output voltage; when the duty cycle of  $S_1$  changes from (0.5– $2/3$ ), the inverter can output the negative output voltage. When the duty cycle is equal to 0.5, the semi-Z-source inverters are able to output zero voltage.

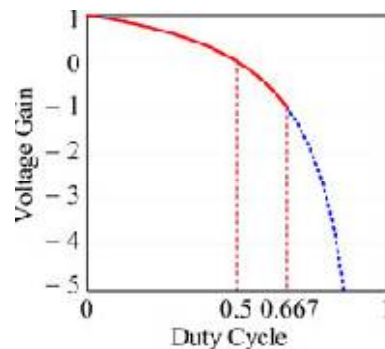


Fig. 3. Duty cycle operation region of proposed semi-Z-source inverters (solid red line)

During the period when  $S_1$  turns on, capacitor  $C_1$  and the input voltage source charge the two inductors, and the inductor current is increased. When switch  $S_2$  is conducted, the two inductors become the source and the inductor current is decreased. The inductor current reference and the capacitor voltage reference direction are marked in the figure for the following steady-state equation derivation. For more detailed dc operation modes of this circuit, the reader could refer to [11].

According to the inductor voltage second balance and the capacitor charge balance equations, we can have the following steady-state equation :

$$\frac{V_o}{V_{in}} = \frac{1-2D}{1-D} \quad (1)$$

$$V_{c1} = \frac{D}{1-D} V_{in} \quad (2)$$

$$IL2 = -I_o \quad (3)$$

$$IL1 = -\frac{D}{1-D}I_o \tag{4}$$

The output voltage of the inverter can be represented by (5) and the modulation index can be defined as (6); plugging (5) and (6) into (1), we can get (7);  $D' = 1 - D$  is the duty cycle of  $S2$  as derived in (8). Because the relationship between the full-bridge inverter output and input voltage is linear in terms of switch duty cycle, the sinusoid output voltage can be achieved by using a sinusoidal changed duty cycle. But the output voltage and the input voltage of the semi-Z-source inverter are no longer in a linear relationship with the switch duty cycle. In order to achieve the sinusoid output voltage, the duty cycle cannot be changed in a sinusoid manner. A corresponding nonlinear revised duty cycle has to be used to generate the correct sinusoid output voltage. A new duty cycle reference, as shown in (7) or (8), has to be used. The generation of pulses using this new modified reference is shown in Fig. 4.

$$V_o = V \sin \omega t \tag{5}$$

$$M = \frac{V}{V_{in}} \tag{6}$$

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{7}$$

$$D' = \frac{1}{2 - M \sin \omega t} \tag{8}$$

The modified SPWM method of semi-Z-source inverters is shown in Fig. 4. Instead of using the sinusoid voltage reference, a modified voltage reference as derived in (8) is used as the reference signal for the conduction of switch  $S2$  in order to output the sinusoid voltage. When the reference is greater than the carrier, switch  $S2$  is turned ON; otherwise,  $S2$  is turned OFF. And the gate signal of  $S1$  is complementary with switch  $S2$ . The modified voltage reference as derived in (7) can be also used directly to generate the gate signal of  $S1$ . But in real implantation, the gate signal generation of  $S2$  needs less calculation of DSP, which is usually preferred. So Fig. 4 uses the generation of gate signal  $S2$  as an example. The modulation index of the modified SPWM method is also in the range of 0–1.

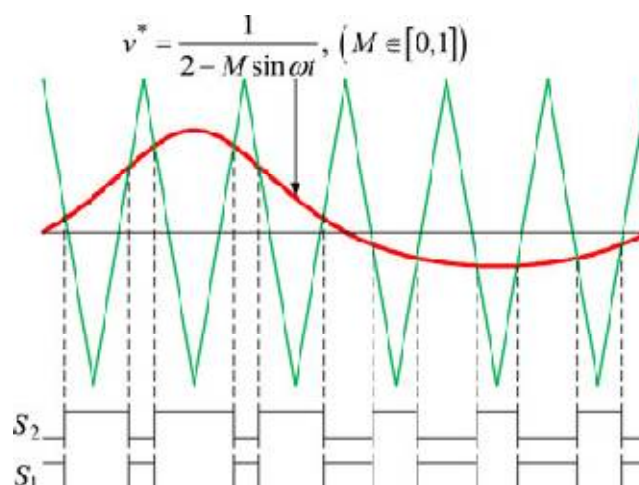


Fig. 4. Modified SPWM for semi-Z-source inverter

Fig. 4 shows the situation when the modulation index  $M = 2/3$  as an example. Fig. 5 shows the duty cycle operation region with different output voltages when the modulation index is equal to 1. The x-axis of Fig. 5 is the output voltage

angle  $\omega t$ . As shown in (5), with the change of  $\omega t$ , the sinusoidal output voltage can be achieved. It can be shown from Fig. 5 that in order to output the sinusoid voltage, the duty cycle  $D$  is limited in the region (0–2/3).

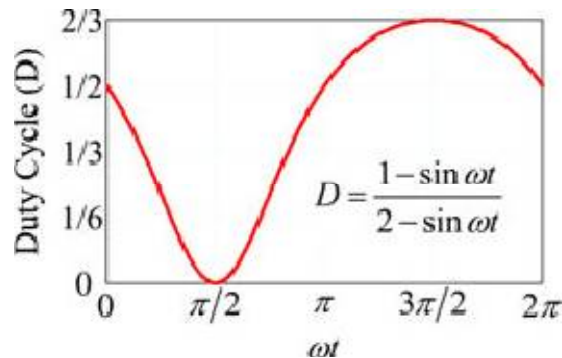


Fig. 5. Duty cycle operation region of semi-Z-source inverters when the modulation index is equal to 1

### B. SEPIC Converter with Magnetic Coupling

A simple solution to elevate the static gain without increases the duty cycle and the switch voltage of a SEPIC converter is to include a secondary winding in the  $L2$  inductor. To reduce the overvoltage at the output diode  $D_o$  due to the existence of the coupling winding  $L2$  leakage inductance, a voltage multiplier at the secondary side is added as shown in Fig. 6. This voltage multiplier increases the converter static gain, the voltage across the output diode is reduced to a value lower than the output voltage and the energy stored in the leakage inductance is transferred to the output. Therefore, the secondary voltage multiplier composed by the diode  $DM2$  and capacitor  $CS2$  is also a non-dissipative clamping circuit for the output diode.

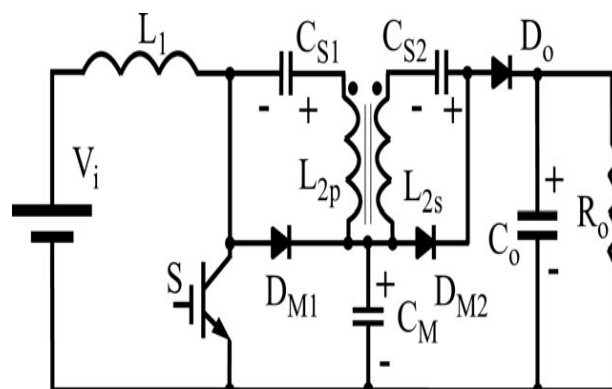


Fig. 6. Modified SEPIC converter with magnetic coupling and output diode voltage clamping

### C. Proposed converter circuit

The proposed converter-inverter combination is shown in Fig. 7. The input supply is given to the modified SEPIC converter. The SEPIC converter produces multiple DC outputs at a switching frequency of 24kHz. The three-winding transformer produces magnetic coupling and electrical isolation. The secondary winding and its associated voltage multiplier produces one DC output. The tertiary winding along with its voltage multiplier produces the second DC output. The semi-Z-source inverter is connected to one of the DC outputs. The inverter converts this DC input into AC output at a switching frequency of 50kHz.

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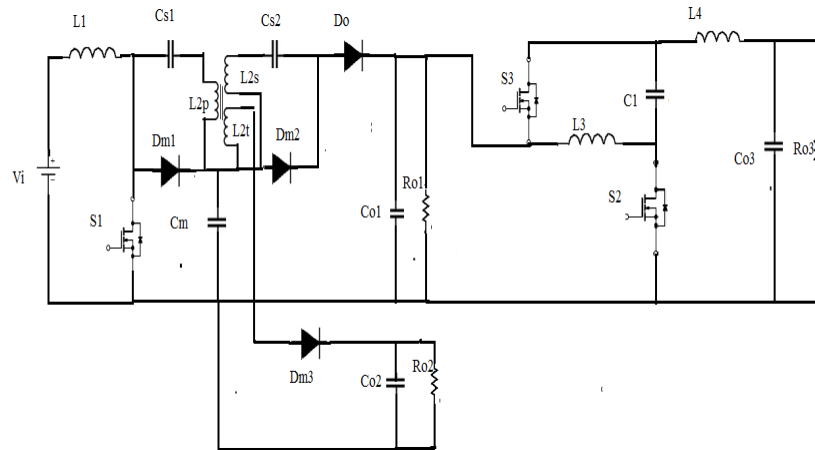


Fig. 7. Proposed converter-inverter circuit

### III. EXPERIMENTAL RESULTS

The experimental results were obtained following the parameters specified in Table I. The experimental results obtained with the modified dual-output SEPIC converter are presented in Fig. 11. The converter operates with an input voltage of 15 V and a resistive load of 1800 ohms. The switching frequency is equal to 24kHz and output voltage is equal to 125V.

TABLE I  
PROTOTYPES PARAMETERS

Parameter	Values
Input Voltage(Vi)	15V DC
Output Voltage(Vo)	125V AC

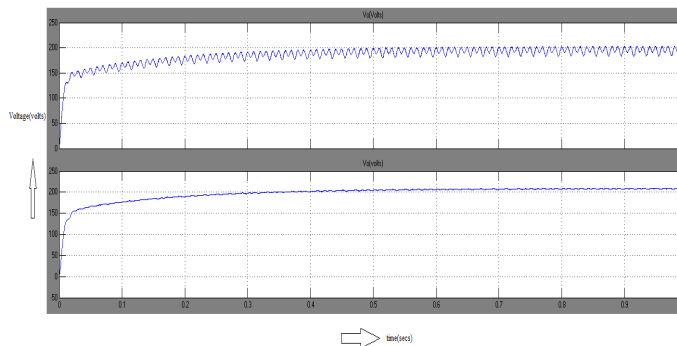


Fig. 8. Multiple DC outputs

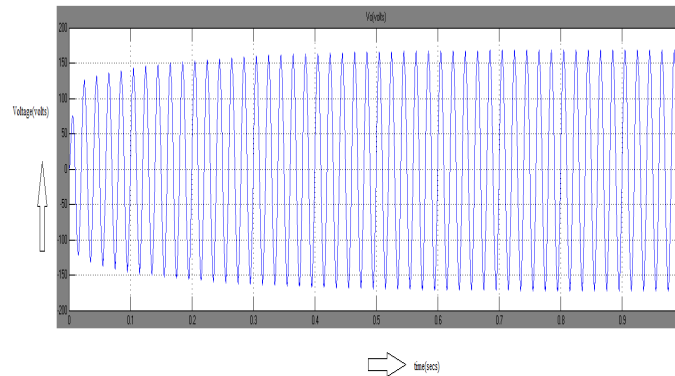


Fig. 9. Final AC output

The semi-Z-source inverter is built with one of the output voltage of modified dual-output SEPIC converter as the input voltage. The switching frequency of the inverter prototype is 50kHz. The load resistance is about 1800 ohms. The experimental results obtained with the semi-Z-source inverter is presented in Fig. 9. The major advantage of the proposed converter-inverter circuit is that the inverter has negligible THD ( about 3%). The THD of the proposed circuit is shown in Fig. 10. The proposed converter-inverter circuit combination can be used for wide applications such as SMPS in computers. The converter circuit used can be implemented for multi-outputs. Also, the inverter circuit can be developed for two-phase or three-phase.

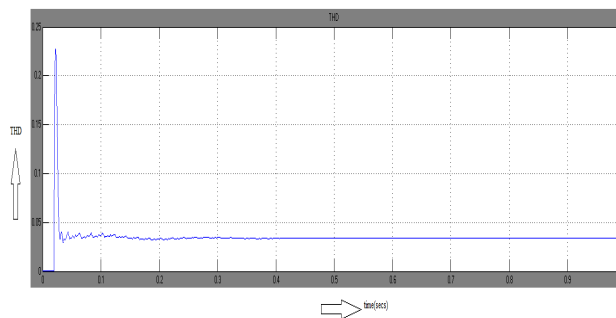


Fig. 10. THD of the proposed circuit

#### IV. EXPERIMENTAL RESULTS

In this paper, combination of a converter and inverter circuit is proposed. The converter circuit used is a modified dual-output SEPIC converter. The SEPIC converter employs magnetic coupling which can help in increasing the static gain. The inverter circuit is a semi-Z-source inverter. A revised nonlinear sinusoid pulse width modulation method is used for the semi-Z-source inverter. By using this method, desired duty cycle can be generated to output the sinusoidal voltage. The major advantage of the proposed circuit is its reduced THD (less than 3%). A prototype is built; experimental results are provided to verify and demonstrate the special features of the proposed circuit.

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