

Modified UPQC for Compensation Power Quality Problems Using MLI with Modified PWM Method

Elavarasan P¹, Sathyamurthy K²

PG Scholar, Dept of EEE, Arignar Anna Institute of Science and Technology, Chennai, India¹

Assistant Professor, Dept of EEE, Arignar Anna Institute of Science and Technology, Chennai, India²

ABSTRACT: The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. In this project, a UPQC topology for applications with non-stiff source is proposed. The proposed topology enables UPQC to have a reduced harmonics. In this project the unified power quality conditioner (UPQC) deals with a solution to compensate the voltage sags and swells and to protect sensitive load. In order to apply the MLI in the distribution systems with voltage in range of kilovolts, series converter as one of the important components of UPQC should be implemented based on the multilevel converters which have the capability to handle voltage in the range of kilovolts and power of several megawatts. So, in this project a configuration of UPQC based on asymmetrical cascade Multicell converter is proposed. The main property of this asymmetrical CM converter is increase in the number of output voltage levels with reduced number of switches. Also, the pre-sag compensation strategy and the proposed voltage sag/swell detection.

KEYWORDS: FACTS, SSSC, SVC, IPFC, CSC, UPFC, UPQC, STATCOM.

I. INTRODUCTION

With the advancement of power electronics and digital control technology, the renewable energy the proliferation of the power electronics devices, nonlinear loads and unbalanced loads have degraded the power quality (PQ) in the power distribution network. Custom power devices have been proposed for enhancing the quality and reliability of electrical power. Unified PQ conditioner (UPQC) is a versatile custom power device which consists of two inverters connected back-to-back and deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer (UPQC 15 MLI). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor. Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter. In general, the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage. This is done in order to ensure a proper compensation at the peak of the source voltage. The authors mentioned about the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system for distortion-free compensation. Due to the aforementioned criteria, many researchers have used a higher value of dc capacitor voltage based on applications. Similarly, for series active filter, the dc-link voltage is maintained at a value equal to the peak of the line-to-line voltage of the system for proper compensation. To reduce the dc-link voltage storage capacity, few attempts were made in literature. A hybrid filter has been discussed for motor drive applications. The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application, and the reactive power compensation is not considered, which is an important aspect in UPQC applications. In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing. Four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, the authors proposed a T-connected transformer and three-phase VSC-based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer. In conventional 11 levels multi-level inverter is implemented but harmonics is injected. So, we have implement 15 level in proposed system.

II. LITERATURE SURVEY

The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. In this project, a UPQC 15 level MLI topology for applications with non-stiff source. This project deals with a dynamic voltage restorer (UPQC 15 MLI) as a Solution to compensate the voltage sags and swells and to protect sensitive loads. Multilevel converters are very interesting alternatives for medium and high-power applications. Here we developed an improved configuration of double flying capacitor Multicell (DFCM) converter. The benefits of this new converter comparing with conventional DFCM, are doubling of the number of output voltage levels and improving the output voltage frequency spectrum. Multilevel converters are very interesting alternatives for medium and high-power applications. Here we developed an improved configuration of double flying capacitor Multicell (DFCM) converter. The benefits of this new converter comparing with conventional DFCM, are doubling of the number of output voltage levels and improving the output voltage frequency spectrum.

III. PROJECT DESCRIPTION

To reduce harmonics of circuit, we have implemented 15 level MLI is applied.

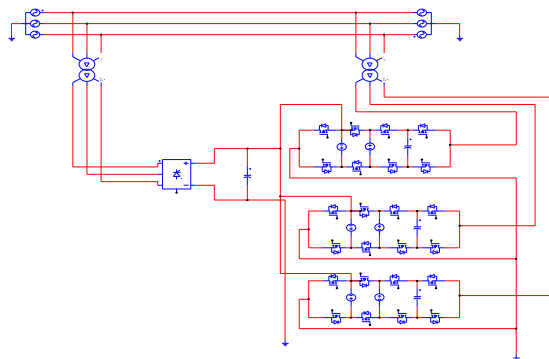


Fig. 1 Normal Pwm method with 8 switches for 11 level inverter

PROPOSED SYSTEM

1. Modified Pwm method with 10 switches for 15 level inverter.
2. 15 level inverter injecting UPQC devices or Statcom for compensation power quality problems.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

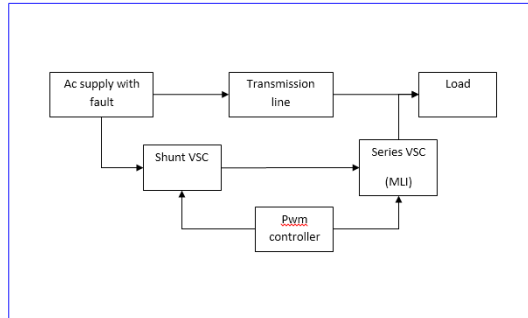


Fig 2 Block diagram

A Unified Power Quality Conditioner (UPQC) is a device that is similar in construction to a Unified Power Flow Conditioner (UPFC). The UPQC, just as in a UPFC, employs two voltage source inverters (VSIs) that connected to a D.C. energy storage capacitor. One of these two VSIs is connected in series with A.C. line while the other is connected in shunt with the A.C. system.

A UPQC that combines the operations of a Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Regulator (UPQC 15 MLI) together.

One of the serious problems in electrical systems is the Increasing number of electronic components of devices that are used by industry as well as residences. These devices, which need high-quality energy to work properly, at the same time, are the most responsible ones for injections of harmonics in the distribution system. Therefore, devices that soften this drawback have been developed.

One of them is the unified power quality conditioner (UPQC), It consists of a shunt active filter together with a series-active filter. This combination allows a simultaneous compensation of the load currents and the supply voltages, so that compensated current drawn from the network and the compensated supply voltage delivered to the load are sinusoidal, balanced and minimized. The series- and shunt-active filters are connected in a back-to-back configuration, in which the shunt converter is responsible for regulating the common DC-link voltage.

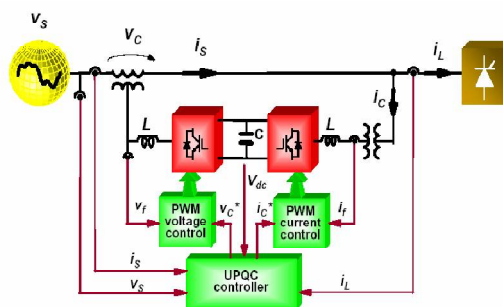


Fig. 3 General Configuration of the Unified Power Quality Conditioner

AUPQCis employed in a power transmission system to perform shunt and series compensation at the same time. A power distribution system may contain unbalance, distortion and even D.C. components. Therefore aUPQCoperate, better Than a UPFC, with all these aspects in order to provide shunt or series compensation.

The UPQC is a relatively new device and not much work has yet been reported on it. Sometimes it has been viewed as combination of series and shunt active filters.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

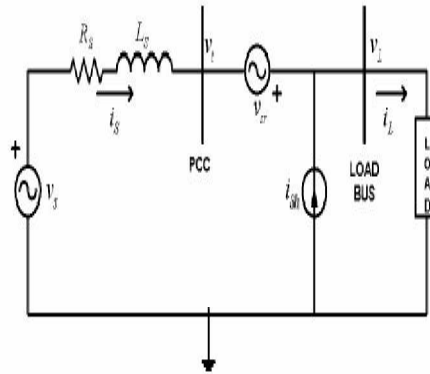


FIG. 4 Equivalent Circuit For UPQC

Taking the load voltage, V_L as a reference phasor and suppose the lagging power factor of the load is $\cos\phi_L$ we can write;

$$V_L = V_L \angle 0^\circ$$

$$I_L = I_L \angle -\theta_L$$

$$V_t = V_L(1+k) \angle 0^\circ$$

Where factor k represents the fluctuation of source voltage, defined as,

$$k = \frac{v_t - V_L}{V_L}$$

The voltage injected by series APF must be equal to,

$$v_{sr} = v_t - V_t = -k V_L \angle 0^\circ$$

The UPQC is assumed to be lossless and therefore, the active power demanded by the load is equal to the active power input at PCC. The UPQC provides a nearly unity power factor source current, therefore, for a given load condition the input active power at PCC can be expressed by the following equations,

$$P_t = P_L$$

$$V_t \cdot i_s = V_L \cdot I_L \cdot \cos\theta_L$$

$$V_L(1+k) \cdot i_s = V_L \cdot I_L \cdot \cos\theta_L$$

The above equation suggests that the source current i_s depends on the factor k , since ϕ_L and I_L are load characteristics and are constant for a particular type of load. The complex apparent power absorbed by the series APF can be expressed as,

$$S_{sr} = v_{sr} \cdot i_s^*$$

$$P_{sr} = v_{sr} \cdot i_s \cdot \cos\theta_s = -k \cdot V_L \cdot I_L \cdot \cos\theta_s$$

$$q_{sr} = v_{sr} \cdot i_s \cdot \sin\theta_s$$

$\phi_s = 0$, since UPQC is maintaining unity power factor

$$P_{sr} = v_{sr} \cdot i_s = -k \cdot V_L \cdot I_L$$

$$q_{sr} = 0$$

The complex apparent power absorbed by the shunt APF can be expressed as,

$$S_{sh} = V_L \cdot i_{sh}^*$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

The current provided by the shunt APF, is the difference between the Input source current and the load current, which includes the load Harmonics current and the reactive current. Therefore, we can write;

$$i_{sh} = i_s - i_l$$

$$i_{sh} = i_s \angle 0^\circ - i_l \angle -\theta_l$$

$$i_{sh} = i_s - (i_l \cdot \cos \theta_l - j i_l \cdot \sin \theta_l) = (i_s - i_l \cdot \cos \theta_l) + j i_l \cdot \sin \theta_l$$

$$p_{sh} = V_L \cdot i_{sh} \cdot \cos \theta_{sh} = V_L \cdot i_l \cdot \sin \theta_l$$

$$q_{sh} = V_L \cdot i_{sh} \cdot \sin \theta_{sh} = V_L \cdot i_l \cdot \sin \theta_l$$

Based on the above analysis the different modes of operation are discussed

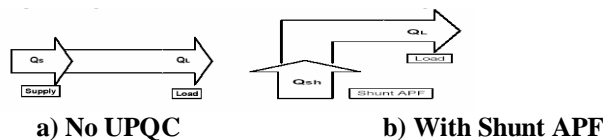


Fig. 5 Reactive Power Flow

The reactive power flow during the normal working condition when UPQC is not connected in the circuit is shown in the Fig.(a). In this condition the reactive power required by the load is completely supplied by the source only. When the UPQC is connected in the network and the shunt APF is put into the operation, the reactive power required by the load is now provided by the shunt APF alone; such that no reactive power burden is put on the mains. So as long as the shunt APF is ON, it is handling all the reactive power even during voltage sag, voltage swell and current harmonic compensation condition.

The series APF is not taking any active part in supplying the load reactive power. The reactive power flow during the entire operation of UPQC is shown in the Fig. (b). In this case no active power transfer takes place via UPQC, termed as Zero Active Power Consumption Mode.

If the load is a non linear one producing harmonics, in such cases the shunt APF injects current equals to the sum of harmonics current but in opposite direction, thus cancelling out any current harmonics generated by non linear load. During this current harmonics compensation mode of operation the shunt APF does not consume any real power from the source since it injected only harmonics currents. Here

Phasor represents the normal working condition, considering leading power factor angle of the load. During this condition i_s will be exactly equal to the i_L . When shunt APF is put into the operation, it cancels out the vars generated by load by injecting a 90° lagging current such that the source current will be in phase with the terminal voltage. The phasor representing this inductive effect is shown in Fig.3.8 the phasor representations during voltage sag and voltage swell condition on the system are shown in the Fig.3.9 and Fig. 3.10 respectively.

Variation of angle θ_{sh} during different modes of operations of UPQC, represented by zones. Figure consists of seven zones of operations. The x axis represents the reference load voltage whereas the shunt APF compensating current can vary from 0° to 360°. If the load is pure resistive, shunt APF does not inject any compensating current since there is no reactive power demand from the load, this condition is represented by zone I. considering the case of inductive load, the load var requirement is supplied by shunt APF by injecting 90° leading current.

IV. CIRCUIT TOPOLOGY

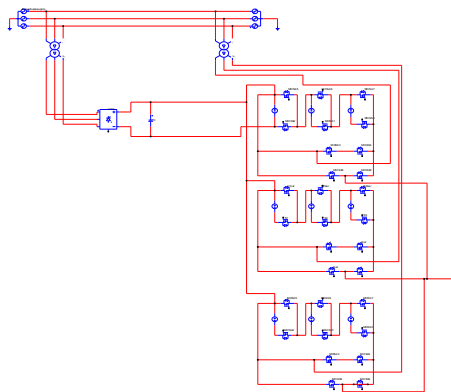


Fig. 6 Proposed Inverter Circuit

A typical UPQC 15 MLI for voltage sag/swell compensation is shown in Fig. 4. 1. When the supply-side voltage changes the UPQC 15 MLI injects a series voltage to maintain the magnitude of the load voltage at its reference value. The UPQC 15 MLI is essentially a voltage-source converter that produces an ac output voltage and injects it in series with the supply voltage. Note that the voltage injection also results in the supply or absorb of active and reactive power. Reactive power can be supplied without taking energy from the dc-side capacitor; however, an active power supply must involve the exchange of stored energy.

The series converter consists of a three-phase voltage-source converter or three single-phase voltage-source converters. It starts to inject three single-phase compensating voltages in series into the power line as soon as voltage sag or swell occurs. In this project, asymmetrical CM converter, introduced in [3], based UPQC 15 MLI is proposed to increase the number of output voltage levels and as a result, reduce the output voltage THD and make it possible to implement UPQC 15 MLI in the distribution systems with voltage in range of kilovolts. A new 15-level asymmetrical CM converter is shown in Fig. 2. The main property of the new configuration of asymmetrical CM converter in comparison with the conventional asymmetrical CM converter is reduction in the number of required high-frequency switches by 50 percent while only 4 low-frequency switches are added. As a result, the cost, size and the power loss of the new configuration of asymmetrical CM converter is decreased. The configuration of UPQC 15 MLI based on configuration of 15-level asymmetrical CM converter is shown in Fig. 4.1.

CONTROL STRATEGIES

Asymmetrical Cascade Multicell Converter Control Strategy The mentioned configuration of asymmetrical CM converter is controlled by level shifted sinusoidal pulse width modulation (LS-SPWM), as shown in Fig. 4, while the absolute of the reference signal is intersected with the level shifted triangle carriers. The low-frequency switch (Ja) is on for positive reference signal and is off for negative reference signal. All states of switches are illustrated in details in Table-I. **B. Voltage Sag/Swell Compensation Strategy** To avoid tripping of the load, the amplitude and phase angle of the load voltage has to be restored by the UPQC 15 MLI. Different strategies can be used to achieve this goal.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

TABLE-I
STATE OF SWITCHES IN 15-LEVEL ASY. CASCADE MULTICELL CONVERTER.

Output Voltage Level	State of Switches
	J_a
Positive	1
Negative	0
	(S_2, S_1, S_0)
0	(0, 0, 0)
1	(0, 0, 1)
2	(0, 1, 0)
3	(0, 1, 1)
4	(1, 0, 0)
5	(1, 0, 1)
6	(1, 1, 0)
7	(1, 1, 1)

In this , the SRF, which is proposed in ,is used to detect the voltage sags/swells and determine the UPQC 15 MLI reference injected voltage. At the beginning, the voltage sag/swell must be detected and then, the UPQC 15 MLI reference injected voltage must be determined.

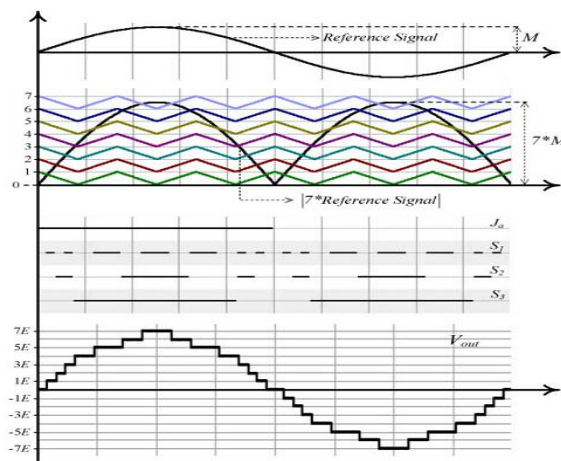


Fig. 7 Level Shifted Sinusoidal Pulse Width Modulation.

states of switches and output voltage for 15-level asymmetrical cascade Multicell converter. where, a grid V, b grid V, c grid V are the measured line-neutral grid voltages of phases a, b and c, respectively and d grid V, q grid V, 0, grid V are the d-component, q-component and zero-component of grid voltages in the SRF, respectively. Also, the rms value (line-neutral) of balanced grid voltage (grid V) can be calculated using the d-component and q-component of grid voltages as follows:

$$|V_{grid}| = \frac{1}{\sqrt{2}} \sqrt{(V_{grid,d})^2 + (V_{grid,q})^2}$$

Then, the phase angle of phase a voltage in the pre-sag state (healthy state) is stored as the reference angle as follows:

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

$$\theta^{ref} = \arctan \left(\frac{V_{grid,d}|_{dc}}{V_{grid,q}|_{dc}} \right)$$

Components of grid voltages in the SRF, respectively. In the case of single phase voltage sag/swell or unbalanced three phase voltage sag/swell, the zero-component of grid voltages in the SRF is not nil. Therefore, it can be used as a parameter to detect the voltage sag/swell.

However, in the case of balanced three phase voltage sag/swell, the zero-component of grid voltages in the SRF is nil and only the rms value of balanced grid voltage in the sag/swell state changes. Because of that, it is necessary to use the rms value of line-neutral grid voltages (grid V) obtained from (2) as another parameter to detect the voltage sag/swell. Finally, the following proposed algorithm based on two steps is performed iteratively to detect the voltage sag/swell: Step-1: The zero-component of grid voltages in the SRF which is obtained from (1) is analyzed.

If it is not equal zero, it means that the unbalanced voltage sag/swell is occurred. So, the voltage sag/swell is detected and then, exit the algorithm. If the zero component is equal to zero, go to step-2. The nil zero-component means that the grid voltages are balanced. So, the rms value of grid voltages must be analyzed as step-2. Step-2: The rms value of line-neutral grid voltages (grid V) obtained from (2) is compared with the reference rms value of line-neutral grid voltages (ref rms V). If they are not equal to each other, it means that the voltage sag/swell is occurred. So, the voltage sag/swell is detected and then, exit the algorithm.

If there is no difference between them, go to step-1. Using the balanced or unbalanced voltage sag/swell. After the detection of voltage sag/swell, the reference rms value of line-neutral grid voltages (ref rms V) and the obtained reference angle (ref θ) are used to determine the values of reference grid voltages in the SRF as follows: explained algorithm makes it possible to detect any

$$V_{grid,d}^{ref} = \sqrt{2} \cdot V_{rms}^{ref} \cdot \sin(\theta^{ref})$$

$$V_{grid,q}^{ref} = \sqrt{2} \cdot V_{rms}^{ref} \cdot \cos(\theta^{ref})$$

$$V_{dvr,d}^{ref} = V_{grid,d}^{ref} - V_{grid,d}$$

$$V_{dvr,q}^{ref} = V_{grid,q}^{ref} - V_{grid,q}$$

$$V_{dvr,0}^{ref} = -V_{grid,0}$$

$$\begin{bmatrix} V_{dvr,a}^{ref} \\ V_{dvr,b}^{ref} \\ V_{dvr,c}^{ref} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1 \\ \cos(\omega t - 120) & \sin(\omega t - 120) & 1 \\ \cos(\omega t + 120) & \sin(\omega t + 120) & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{dvr,d}^{ref} \\ V_{dvr,q}^{ref} \\ V_{dvr,0}^{ref} \end{bmatrix}$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

V. SIMULATION RESULTS

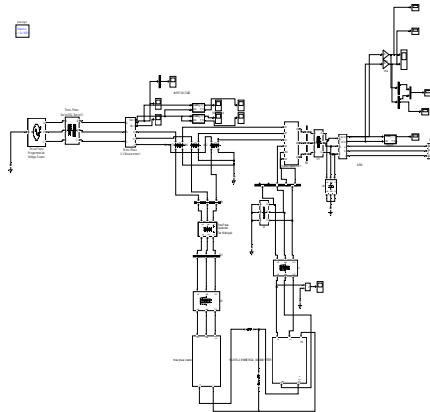


Fig. 8 Simulation Circuit Diagram

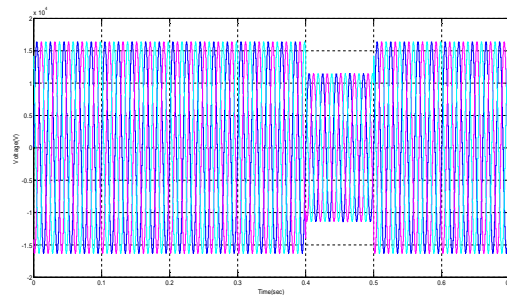


Fig.9 Input Sag Voltage of Proposed Method

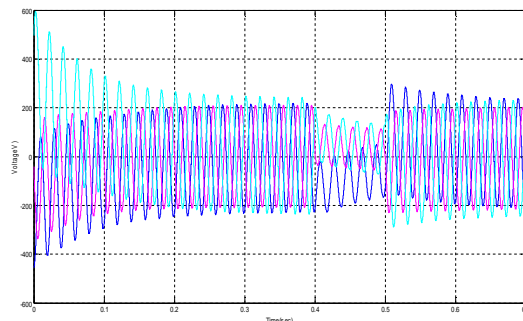


Fig. 10 Input Sag Current of Proposed Method

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

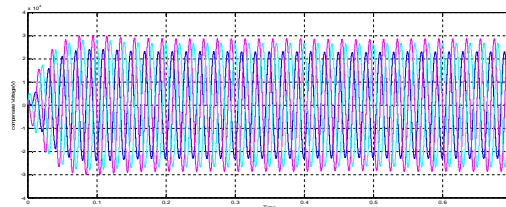


FIG.6.4 COMPENSATED SAG VOLTAGE OF PROPOSED METHOD

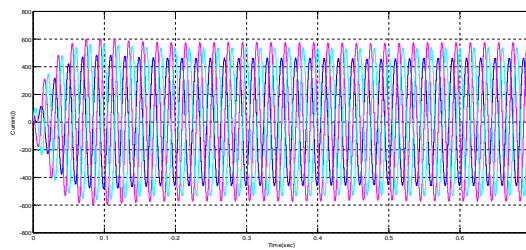


FIG.6.5 COMPENSATED SAG CURRENT OF PROPOSED METHOD

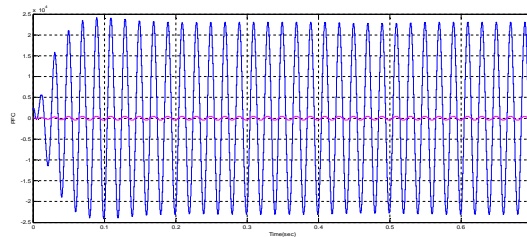


FIG.6.6 SAG PFC OF PROPOSED METHOD

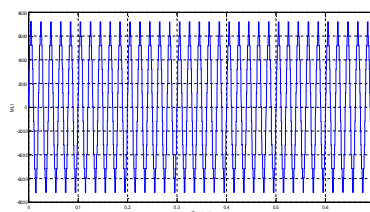


FIG.6.7 MLI OF PROPOSED METHOD

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

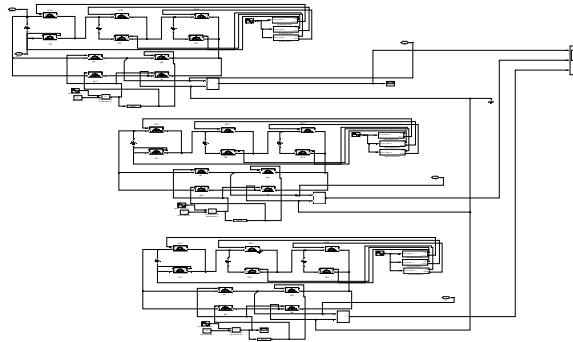


FIG.6.8 MLI CIRCUIT OF PROPOSED METHOD

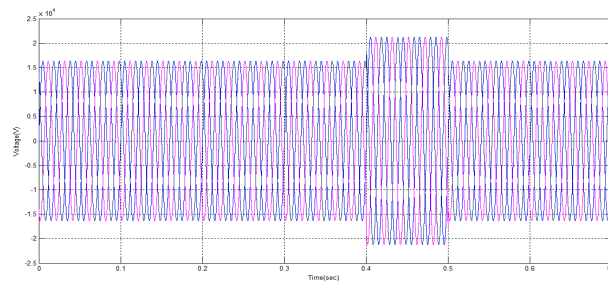


FIG.6.9 SWELLS VOLTAGE OF PROPOSED METHOD

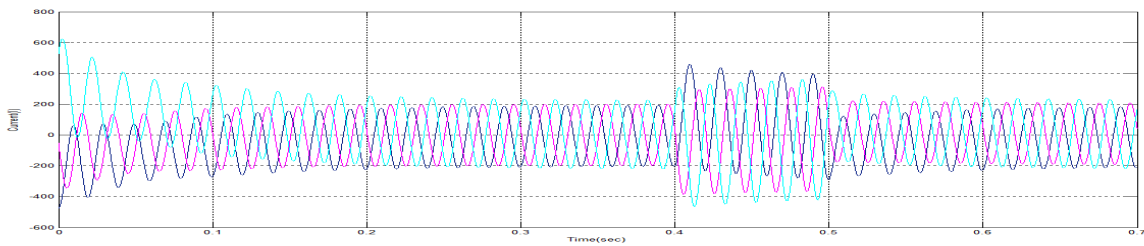


FIG.6.10 SWELL CURRENT OF PROPOSED SWELL METH

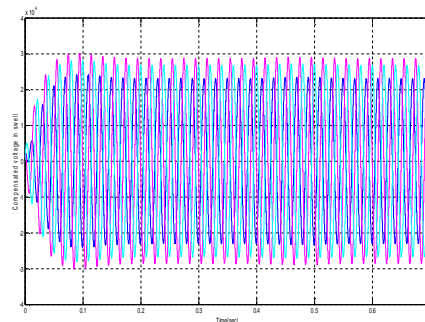


FIG.6.11 COMPENSATE VOLTAGE OF PROPOSED SWELL METHOD

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

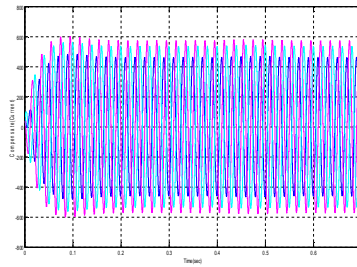


FIG.6.12 COMPENSATE CURRENT OF PROPOSED SWELL METHOD

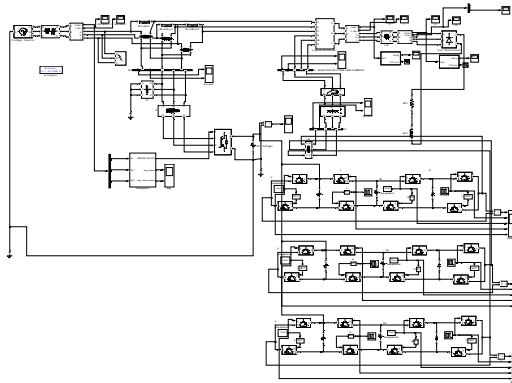


FIG.6.13 EXISTING CIRCUIT DIAGRAM

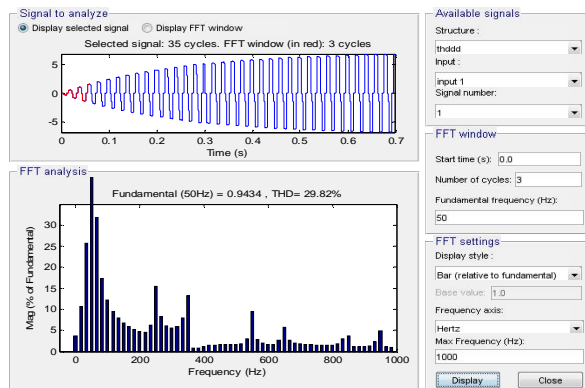


FIG.6.14 EXISTING THD VALUE

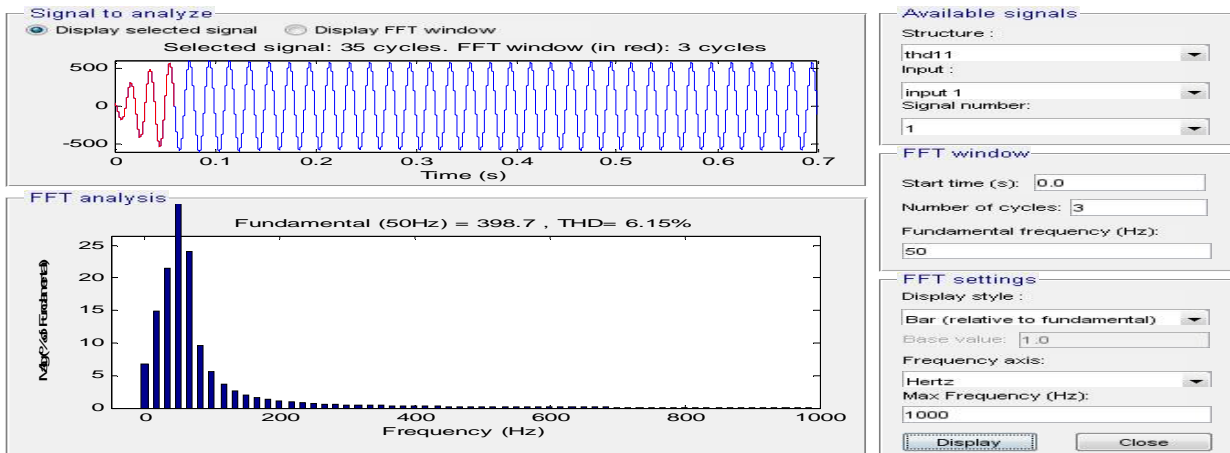


FIG.6.15 PROPOSED THD VALUE

VI. CONCLUSION

Voltage sags/swells are major problems in power systems due to the increased integration of sensitive loads into them. UPQC 15 MLI systems are able to compensate these voltage sags/swells. Because the multi cell converters are very interesting for high-power/medium-voltage applications, and also considerably improve the output voltage frequency spectrum, in this project configuration of UPQC 15 MLI based on asymmetrical CM converter has been proposed to improve the quality of UPQC 15 MLI output voltage and to be used in the distribution systems with voltage in range of kilovolts. In the proposed configuration of UPQC 15 MLI, number of required high-frequency switches is reduced by 50 percent.

Therefore, the cost, size and power loss are decreased. Also, new methods based on the SRF have been used to detect the voltage sag/swell and determine the reference series injected voltage of UPQC 15 MLI. As depicted in simulation results, the pre-sag compensation strategy and the proposed SRF based detection and determination methods show excellent performance and good dynamic response time.

REFERENCES

- [1] "Performance Analysis of Improved Double Flying Capacitor Multicell Converter", Amal Philomiya L1, Saravanan.C2, Narasimman.P, International Journal of Emerging Technology and Advanced Engineering, (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 7, July 2013).
- [2] "A Modified Three-Phase Four-Wire UPQC Topology With Reduced DC-Link Voltage Rating", Srinivas BhaskarKaranki, NageshGeddada, IEEE transactions on power electronics, vol. 23, no. 6, November 2008
- [3] "Voltage Sag and Swell Compensation with UPQC 15 MLI Based on Asymmetrical Cascade Multicell Converter ", S. MasoudBarakati, IEEE transactions on power delivery, vol. 23, no. 2, April 2008.
- [4] "Performance Analysis of Improved Double Flying Capacitor Multicell Converter", AmalPhilomiya, Saravanan., Narasimman, ESEVIER11 September 2006..
- [5] M.R.Banaei, S.H.Hosseini, S.Khanmohamadia and G.B.Gharehpetian, "Verification of a new energy control strategy for dynamic voltage restorer by simulation", Elsevier Journal of Simulation Modeling Practice and Theory, vol. 14, no. 2, pp. 112–125, Feb. 2006.
- [6] S.H. Hosseini, A.KhoshkbarSadigh and G. Gharehpetian, "Flying capacitor multicell converter based DVR with energy minimized compensation strategy", in Proc. of 6th Int. Conf. ELECO, Nov. 2009, Bursa, Turkey, pp. 1–5.
- [7] S.H. Hosseini, A. KhoshkbarSadigh and A. Sharifi, "Estimation of flying capacitors voltages in multicell converters", in Proc. 6th International Conference ECTI-CON, Pattaya, Thailand, May 2009, pp. 110–113.
- [8] A.KhoshkbarSadigh, E.Babaei, S. H.Hosseini and M. Farasat, "Dynamic voltage restorer based on stacked multicell converter", in Proc. of ISIEA, Oct. 2009, Kuala Lumpur, Malaysia, pp. 1–6. [9] A. KhoshkbarSadigh, S. H. Hosseini, S. M. Barakati and G. Gharehpetian, "Flying capacitor multicell converter based dynamic voltage restorer", in Proc. of 41st NAPS, Oct. 2009, Mississippi State, USA, pp. 1–6.
- [9] A.KhoshkbarSadigh, S.H. Hosseini, S.M. Barakati and G. Gharehpetian, "Stacked multicell converter based DVR with energy minimized compensation strategy", in Proc. of 41st NAPS, Oct. 2009, Mississippi State, USA, pp. 1–6.
- [10] C.S.Lam, M.C.Wong and Y.D.Han, "Voltage swell and over-voltage compensation with unidirectional power flow controlled dynamic voltage restorer", IEEE Trans. Power Delivery, pp. 2513–2521, Oct. 2008.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 3, March 2016

- [11]J. Lamoree, L. Tang, C. DeWinkel, and P. Vinett, "Description of a micro-SMES system for protection of critical customer facilities", IEEE Trans. Power Delivery, vol. 9, no. 2, pp. 984–991, Apr. 1994.
- [12]S.A. Saleh, C. R. Moloney and M. A. Rahman, "Implementation of a dynamic voltage restorer system based on discrete wavelet transforms", IEEE Trans. Power Delivery, vol. 23, no. 4, pp. 2366–2375, Oct. 2008.
- [13]P.R.Sánchez, E.Acha, J. E. O. Calderon, V. Feliu and A. G. Cerrada, "A Versatile control scheme for a dynamic voltage restorer for power-quality improvement", IEEE Trans. Power Delivery, vol. 24, no. 1, pp. 277–284, Jan. 2009.
- [14]B.Wang and G.Venkataramanan, "Dynamic voltage restorer utilizing a matrix converter and flywheel energy storage", IEEE Trans. Industry Applications, vol. 45, no. 1, pp. 222–231, Jan./Feb. 2009.
- [15]M.A.Pérez, P.Cortés and José Rodríguez, "Predictive control algorithm technique for multilevel asymmetric cascaded H-bridge inverters", IEEE Trans. Industrial Electronics, vol. 55, no. 12, pp. 4354–4361, Dec. 2008.