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Design and FPGA Implementation of Digital Circuits Using Reversible Logic

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ABSTRACT: Interconnections are increasingly the dominant contributor to delay, area and energy consumption in CMOS digital circuits. Reversible logic can decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. Multiplexing is the generic term used to designate the operation of sending one or more analog or digital signals over a common transmission line at dissimilar times or speeds and as such, the scheme used to do that is called a Multiplexer. In digital electronics, multiplexers are similarly known as data selectors as they can “select” each input line analog switches are encased made in a single form of IC package individuals conflicting to the “mechanical” type selectors into day era, such reversibility has become essential part of digital world to make digital circuits more efficient. Reversible logic proposes a new method to reduce interconnections and power for various multiplexers.

KEYWORDS: Reversible logic, Fredkin gate, Digital Circuits, MVL and Latch.

I. INTRODUCTION

Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there are equal number of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved.

Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one-to-one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa.

QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates. QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation. Due to high error rates in nano-scale manufacturing, QCA and other nanotechnologies target reducing device error rates.

This paper is organized as follows. Section II presents the conservative logic gates, Section III presents design of testable reversible latches, Section IV describes QCA, Section V presents design of testable reversible flip-flop, Section VI discusses the application of the proposed two vectors, all 0s and all 1s, Section VII provides some discussions and conclusions.

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II. CONSERVATIVE LOGIC GATES

In order to design the sequential circuits, the conventional logic gates are appropriately designed from the reversible gates. The reversible gates used to design the conventional logic are so chosen to minimize the number of reversible gates used and garbage outputs produced. The design of AND function using Fredkin gate. The design of NAND and NOR function using New Gate respectively. Feynman Gates can be used for copying the outputs and to avoid the fan out problem in reversible logic. In the Feynman gate, there are exactly two outputs corresponding to the inputs and a '0' in the second input will copy the first input to both the outputs of that gate. Hence it can be concluded that Feynman gate is the most suitable gate for single copy of bit since it does not produce any garbage output. The Feynman gate as copying output and NOT function respectively. May stuck at 0 or 1 leading to accessing wrong address, no address, or multiple addresses.

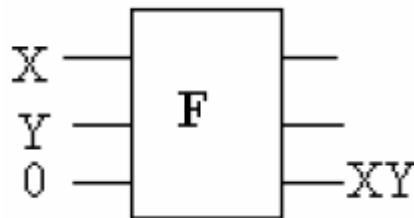


Fig.1 Fredkin Gate as AND Gate

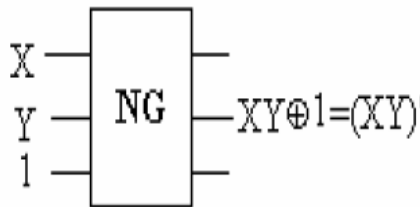


Fig.2 New Gate As NAND Gate

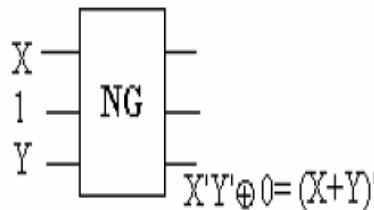


Fig.3 New Gate As NOR Gate

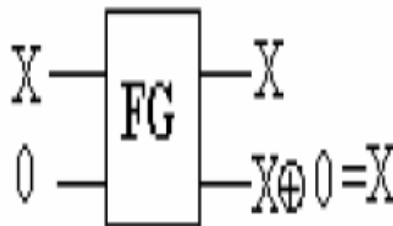


Fig.4 Feynman Gate As Copying Output

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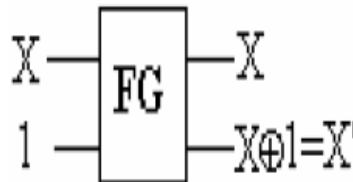


Fig.5 Feynman Gate As Not Gate

Novel Reversible Flip Flops are designed using Feynman Gate, New gate and Fredkin Gate. The designed FFs are highly optimized in terms of number of reversible gates and garbage outputs.

Reversible logic elements, both with and without the property of conservatism, can be defined in many different logic systems. For the purposes of this paper, the class of reversible elements that can be modeled as binary-valued logic circuits will be called classical reversible logic elements. Much work has been done in defining and characterizing classical reversible logic and applying the concepts toward power conservation and specific technology implementations. This section will briefly define basic results in classical reversible logic.

Gate Type	Functionality
1*1 Not	$x^+ = x$
2*2 Feynman [4]	$x^+ = x$ $y^+ = x \oplus y$
3*3 Toffoli [19]	$x^+ = x$ $y^+ = y$ $z^+ = xy \oplus z$
3*3 Fredkin [5]	$x^+ = x$ $y^+ = xy \oplus xz$ $z^+ = \bar{x}z \oplus xy$

Table.1 Gate functionality

III. DESIGN REVERSIBLE LATCHES

The characteristic equation of the D latch can be written as $Q^+ = D \cdot E + \bar{E} \cdot Q$. In the proposed work, enable (E) refers to the clock and is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is $Q^+ = D$. While, when $E = 0$ the latch maintains its previous state, that is $Q^+ = Q$. The reversible Fredkin gate has two of its outputs working as 2:1 MUXes, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F). The realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault.

In this paper, we propose to cascade another Fredkin gate to output Q as shown in Fig. The design has two control signals, C1 and C2. The design can work in two modes: normal mode and test mode.

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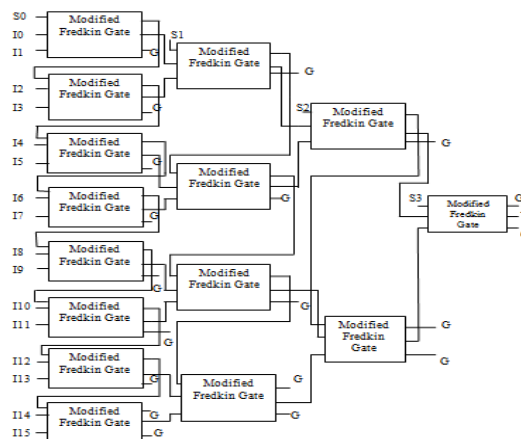
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IV. BASIC PRINCIPLES OF MVL

Depending on the assigned values to the inputs variables, MVL function will represent the value in domain $D = \{0, 1, \dots, K = L-1\}$ and then a unique truth table can be obtained. Analogous to Products of Sums (POS) or Sum of Products (SOP) which is a unique representation of the function for binary algebra, canonical Sum of Extended Products (SOEP) form is defined for universal set of operators for quaternary MVL algebra. The already mentioned operators SUC, MAX, eAND1, eAND2, eAND3 in the introduction, define a universal set for quaternary logic under the proposed algebra. Once the universal set is defined, to minimize the number of terms and literals of the MVL function postulates and theorems are needed, thus a minimal covering is determined. Also suitable algebra laws are defined to develop algorithms in a proper way and to implement software tools for performing the minimization. In binary algebra, there are many techniques for function minimization such as K maps, Espresso, QuineMcCluskey etc [17]. Depending on the MVL algebra under consideration all these binary techniques can be extended to the MVL domain. The next step for the synthesis is to design gates in either CMOS current mode or CMOS voltage mode. In voltage mode there is problem of how to define voltage levels to discriminate different logic reference levels for defining the threshold value of CMOS inverters. As this paper addresses voltage mode to design gate some characteristics must be defined to overcome this issue, for example – power consumption, frequency response, fan-in, fan-out, noise margins etc that has an effect on the W/L relation between the PMOS and NMOS gates and also on how to choose the reference voltage to discriminate among logic levels for the MVL. In recent years quaternary circuits has been studied increasingly as they have the practical advantage of transforming a four-valued signal into a two-valued signal. The next step is to define an algebra which is easy to learn and convenient to use, must have a well-known methodology which is feasible to implement from both algorithmic and gates point of views. A possible way is to extend the well-known concepts of the binary switching algebra to MVL algebra. This approach is adopted in this work.

MVL variables are denoted as A_j for notation purpose. MVL constants are represented by lower case letters such as j, k, l and the base of the digital representation is denoted by L with domain $D = \{0, 1, 2, \dots, K = L-1\}$. The Maximum operator is denoted by “+” symbol. The proposed closed MVL algebra is the ordered set with domain D in which acting one unary Successor (SUC) operator and two binary extended AND (eAND) and Maximum (MAX) operators (+, * $_j$) and two elements 0 and (L-1) with the following definitions.

V. REVERSIBLE MUX

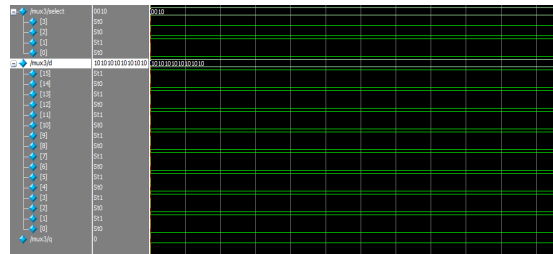


16:1 MUX

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Simulation for Reversible Mux 16:1

IV. CONCLUSION

Therefore conservative reversible logic gates are used to designed sequential circuits. The proposed system is used in the Feynman gate. This paper proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed sequential circuits based on conservative logic gates outperform the sequential circuit implemented in classical gates in terms of testability. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects.

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