

Design and Analysis of Track-And-Hold Amplifiers Using BiCMOS Technology

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ABSTRACT: The track-and-hold amplifier (THA) using fully-differential architecture to mitigate common-mode noise and suppress even-order harmonics is presented. CMOS switch and dummy switches are adopted to achieve high speed and good linearity. A cross-coupled pair is used in the input buffer to suppress the charge injection and clock feedthrough. Both the input and output buffers use an active inductor load to achieve high signal bandwidth. The THA is realized with 0.18 micro meter or 45nm SiGeBiCMOS technology using only CMOS devices at a 1.8 V voltage supply and with a core area of 0.024 mm². It is shown that both the thermal noise and shot noise contribute to the TH amplifier (THA) at ultra-high frequency. Simulations also locate the major noise contributor in the SEF THA. Approximate expressions for the output noise of the major noise contributor of the THA are derived and the numerical experiment of the output noise is presented.

KEYWORDS: Track and hold amplifier, BiCMOS switched emitter follower, ultra-high speed, noise location and noise model.

I. INTRODUCTION

The high-speed analog-to-digital converters (ADCs) is the heart of the optic equalizer [1]. The THA is a crucial building block in ADCs since it makes a great impact on the dynamic performance of ADCs. To achieve high speed operation, the open loop architecture switched emitter follower is chosen for THA [1]. Noise is one of the important factors that limit the dynamic range of THA. As a result, it reduces the achievable resolution of the circuit. Therefore it is necessary to minimize this effect in order to improve the circuit performance. Theoretical noise analysis and numerical examples for switched capacitor amplifier circuits are present in [2]. To the best of our knowledge, noise analysis in SiGe HBT SEF THA has not been reported in the literature. In this paper, we analyze the noise of major noise contributor in the hold mode of THA with the SEF configuration. Simulation and analysis show that, at ultra-high frequency, both the thermal noise and shot noise contribute to the output noise, the flicker noise can be ignored. Section 2 describes the noise in a SEF THA for ultra-high speed application.

With CMOS technology, downscaling of the conversion speed of the ADC has rapidly been developing, implying that the T/H has to process input signals at increasingly higher speed. Thus, in order to guarantee the accuracy of the T/H at such high speed of operation, a larger bandwidth becomes necessary, leading, on the other hand, to significant power dissipation, which might become the dominant factor in the whole ADC power consumption. In this brief, a power-speed high-accuracy T/H amplifier will be presented. The proposed power-switching (P-S) technique provides a rapid switching operation in order to avoid the static power dissipation of the T/H without degrading the output voltage swing. Meanwhile, by using the technique, the tracking speed and accuracy of the T/H are enhanced as well.

For the CMOS track-and-hold circuit design, the switched source follower topology is often employed. The switched capacitor technique is also suitable in the microwave and millimeter-wave (MMW) circuit design, and it consumes lower power consumption with good linearity and SFDR [15], [16]. The gain roll-off of the amplifier occurs at high frequency due to the Miller capacitance of the transistor, the loss of substrate, conductor, or radiation, especially for the MMW circuits. A common-source (CS) common-gate (CG) cascode amplifier can be adopted to reduce the Miller effect since the input impedance of the CG stage is $1/g_m$ and the voltage gain is close to 1. To maintain the certain operation bandwidth, an inductive peaking technique can be adopted in the input and output buffers to efficiently compensate the high-frequency loss [18], [20]. The inductive peaking technique can be used in

the broadband designs to extend the operation bandwidth. Moreover, the distributed amplifier (DA) can also be employed in the input buffer to improve the bandwidth and input return loss. The DA has been employed in a CMOS track-and-hold amplifier [14], and the input bandwidth can be up to the several gigahertz range.

III. TRACK-AND-HOLD STAGE

The track-and-hold stage is designed using the switched capacitor technique, and the schematic is shown in Fig. 2. Two paths are for the differential inputs, and the switch consists of one PMOS transistor (or) and a dummy PMOS transistor (or). The dummy PMOS transistors are used to eliminate the issue of charge injection when the track-and-hold stage is operated in the hold mode. To maximize the bandwidth and minimize the insertion loss of the track mode, the transistor size of the switch should be properly designed. The even harmonics can be intrinsically cancelled due to the differential operation. For the consideration of the linearity and SFDR, the odd harmonics should be carefully considered, especially for the third-order harmonic. The third-order harmonic distortion (HD3) is defined as the power ratio between the fundamental and third harmonic. The HD3 of the switch can be expressed as

$$HD3 = \frac{\omega_0 \tau_0}{4} \left(\frac{A}{V_{DD} - V_{SQ} - V_T} \right)^2$$

Where ω_0 is the input angular frequency, τ_0 is the transconductance delay of the transistor and it can be obtained based on the circuit simulation. The track-mode bandwidth of the switch is the single-end input swing is the transistor threshold voltage, and the typical value is 0.3 V and is an appropriate dc value about 0.5 V of the input signal. The calculated HD3 and transconductance delay versus total gate width is plotted in Fig. 3, where the input frequency is 5 GHz with an amplitude swing of 0.3 V_{p-p}. The HD3 and the transconductance delay decrease as the gate width increases, but the bandwidth degrades due to the parasitic capacitor of the transistor. Therefore, the design tradeoff of gate width is between the HD3 and the bandwidth. To completely investigate the design tradeoff, the 65-nm CMOS switch with a holding capacitance, C_H , of 390 fF is simulated under the sampling and holding conditions. To minimize the chip area, the holding capacitor can be designed using the input gate parasitic capacitor of the transistor. The capacitance is based on the input parasitic capacitance of the output buffer. The simulated turn-on bandwidth, insertion gain, and HD3 versus total gate width for the track-and-hold switch are plotted in Fig. 4, where the input frequency is 5 GHz with an amplitude swing of 0.3 V_{p-p} and the sampling rate is 10 GS/s. For this simulation setup of the switch, the input termination resistance is 50 Ω , and the output termination network is a 50- Ω resistor parallel with a 390-fF holding capacitor. For the dynamically sample-and-hold operation, the insertion gain increases as the total gate width increases, and the turn-on bandwidth decreases. The minimum HD3 occurs when the total gate width is close to 60 μ m. To achieve good linearity with enough bandwidth, a total gate width of 164 μ m is selected as the preliminary design.

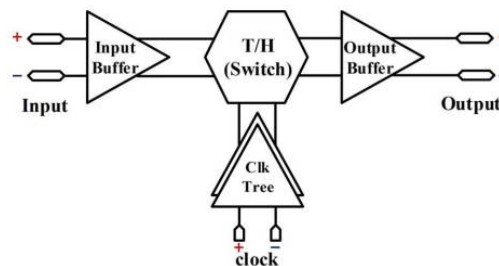


Fig 1. Block diagram of a typical track-and-hold circuit.

In this paper, design and analysis of CMOS high-speed high dynamic-range track-and-hold amplifiers are presented. The CS-CG cascode topology with an inductive peaking technique is employed to enhance the dynamic range and the bandwidth. The switched capacitance technique is used to sample and hold the input signal, and the device size is investigated to improve SFDR and THD. The design methodology of the high-speed high dynamic-range CMOS track-and-hold amplifier is completely addressed with theoretical calculations. Two track-and-hold amplifiers are successfully demonstrated in 65- and 90-nm CMOS processes. Moreover, the DA is also adopted for the 90-nm CMOS track-and-hold amplifier to highly extend the input bandwidth up to 19 GHz. The proposed CMOS track-and-hold

amplifiers feature high SFDR and low THD with compact chip area, and they can be compared with the previously reported state-of-the-art track-and-hold amplifiers. The spiral inductor and the transmission line are adopted for the peaking elements. The thin-film microstrip line (TFML) is adopted for the circuit connection to further reduce unwanted coupling effect and chip size, the top metal (M9) is designed as a signal line, and the bottom metal (M1) is designed as a grounded plane. The spiral inductor and the transmission line are adopted for the peaking elements. The thin-film microstrip line (TFML) is adopted for the circuit connection to further reduce unwanted coupling effect and chip size, the top metal (M9) is designed as a signal line, and the bottom metal (M1) is designed as a grounded plane.

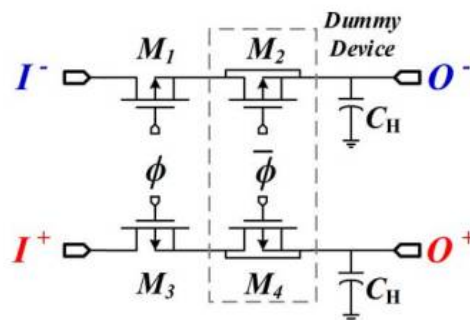


Fig 2. Schematic of the track-and-hold stage.

All the passive components, including transmission lines, inductors, capacitors, and resistors, are simulated with a fullwave electromagnetic (EM) simulator [21]. The track-and-hold amplifier is usually composed of a differential input buffer, a differential output buffer, a track-and-hold stage, and a differential clock buffer. The input and output buffers are used to maintain the voltage swing of the input signal over operation frequency, and the buffers should have good linearity, high SFDR, and broadband and flat voltage gain. In general, the voltage gain of the buffer can be close to 0 dB. The switch is often employed in the track-and-hold stage to perform the input signal tracking and sampling. The track-and-hold switch should have low turn-on insertion loss, high turn-off isolation, and good linearity. To achieve the high-speed operation, the bandwidth of the track mode should be wide enough as the switch is turned on. The clock buffer is designed to make the voltage swing of the clock signal large enough, and the track-and-hold switch can be normally operated in turn-on and turn-off states. In addition, the rising and falling times of the clock can be reduced using the clock buffer for high-speed sampling, and the signal-to-noise ratio and resolution would be further improved.

The schematic of the 45-nm CMOS track-and-hold amplifier is shown in Fig. 3, and the design parameters are summarized in Table I. The track-and-hold amplifier consists of a differential input buffer, a differential output buffer, a differential track-and-hold switch, and a differential clock buffer.

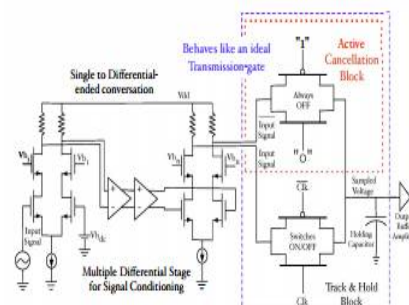


Fig 3. Schematic of the 45-nm CMOS track-and-hold amplifier designed using cascode buffers with inductive peaking.

The clock buffer is adopted to improve the input sampling clock as an ideal square waveform for the track-and-hold operation. The clock buffer is designed based on the complementary inverter. The size ratio of NMOS and PMOS should be properly designed to make sure the output clock swing is high enough with small rising and falling time. The transistor sizes of the switch are determined based on the discussion in Section II-A to minimize the charge injection,

hold-mode feed-through, and distortion. The body bias technique can also be employed in the switch to enhance the linearity due to the reduction of the nonlinear junction capacitances [25]. The input parasitic capacitances of the output buffer and are also performed as the hold-mode element to further reduce the chip size. The input and output buffers are designed using a two-stage differential pair to enhance the common-mode rejection ratio. The first stage is designed using the CS amplifier with a source resistor to enhance the linearity, and the second stage is designed using the cascode amplifier with inductive peaking to improve the voltage headroom. The transistors of the buffers are operated in the class-A region for high linearity. The drain and source resistors, and , are selected about 2:1 ratio to achieve unity dc gain. The drain and source inductances, and , are designed between 100 and 150 pH to further improve the gain roll-off at high frequency. The schematic of the 45-nm BICMOS track-and-hold amplifier is shown in Fig 4, which consists of a differential switch, a differential input buffer, and a differential output buffer.

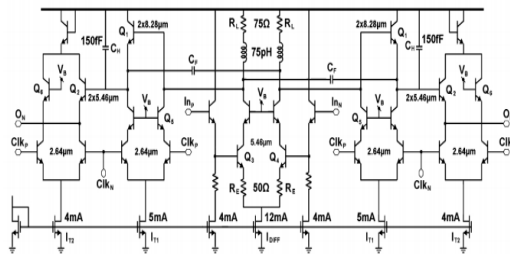


Fig 4. Schematic of the 45nm BICMOS track-and-hold amplifier designed using the distributed input buffer.

The circuit topology and design method of the switch is similar to the 45-nm BICMOS track-and-hold amplifier. The CS-CG cascode amplifier with inductive peaking is also adopted for the output buffer to enhance the voltage headroom and the bandwidth. The input buffer is designed using a two-stage DA to further improve the operation bandwidth and the input return loss. The inductances for the drain and gate artificial transmission lines should be properly designed to maximize the bandwidth with flat frequency response. The layouts of and are designed using a differential spiral inductor to reduce the chip area and enhance the common-mode rejection ratio. The loss of the switch is further compensated by the input buffer, and the voltage gain can be designed by selecting the transistor size or the dc bias of the gain cell. Several current sources, current mirror, and bypass networks are also included in the chip for the dc bias.

IV. RESULTS

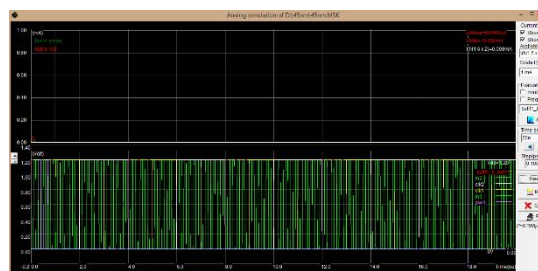


Fig 5. Schematic of the 45-nm CMOS track-and-hold amplifier designed using cascode buffers with inductive peaking.

V. CONCLUSION

Three high-speed high dynamic-range track-and-hold amplifiers have been successfully developed using 45nm CMOS processes. The cascode topology with inductive peaking has been employed in the circuit design to enhance the linearity and bandwidth. The device size and bandwidth have been investigated to obtain the design methodology. The power consumption of 45-nm CMOS track-and-hold amplifiers are 0.0388uW respectively. With the comparable dc voltage and power consumption, the proposed track-and-hold amplifiers demonstrate high SFDR and

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low THD. Moreover, they can be applied to the front-end sample and hold applications, such as a high-speed low-power hand-held oscilloscope and broadband data converter.

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