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Low Power PRPG and Decompressor using PRESTO generator

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ABSTRACT: A pseudorandom test patterns are generated using low power programmable generator with desired toggling levels and enhanced fault coverage gradient. A linear feedback shift register drives a phase shifter to produce binary sequence using preselected toggling (PRESTO) activity. Several controls of the generator are selected automatically for easy and precise tuning. For shaping the test power envelope in a fully predictable, accurate, and flexible fashion a low power(LP) test compression method is used by adapting the PRESTO-based logic BIST (LBIST) infrastructure. To deliver high quality test the test compression efficiently combines with LBIST in proposed hybrid scheme.

KEYWORDS: Built-in self-test (BIST), low-power (LP) test, pseudorandom test pattern generators (PRPGs).

I. INTRODUCTION

The primary objective of manufacturing test is to ensure reliable and high quality semiconductor products conditions and consequently test solutions may also undergo a significant evolution. Logic Built-In Self-Test (LBIST) is developed for board, system, and in-field test, is now gaining acceptance for production test as it provides very robust DFT and is used increasingly often with test compression. Combining LBIST and test data compression concept is introduced to overcome the bottleneck of test data bandwidth between the tester and the chip. Several BIST hybrid schemes deterministically stores top-up patterns to detect random pattern resistant faults on the tester in a compressed form, and use the existing BIST hardware to decompress these test patterns.

In this paper, we propose a PRPG for LP BIST applications. Using preselected toggling levels the generator aims to reduce the switching activity during scan loading.

In the burst-mode approach five consecutive clock cycles are used. For shifting purposes the first four cycles are used and the last cycle is designated for capture. The objective is before the last shift, to stabilize the power supply and applied the capture pulses. A burst clock controller slows down some of the shift cycles to reduce the voltage drop related to a higher circuit activity. By reducing the di/dt effect it gradually increase the circuit activity. Depending on the needs for gradually warming up of the circuit the controller can gate the shift clocks. Low Power (LP) test compression schemes adapt again LFSR reseeding to reduce scan-in transitions thereby reducing the number of transitions. The drawback in existing system is that this technique is applied for only large circuit.

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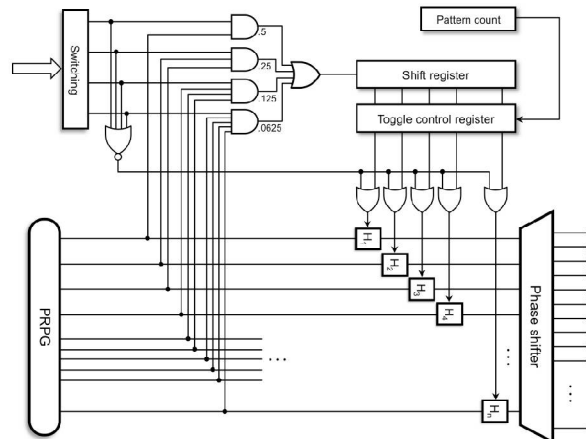


Fig. 1. Basic architecture of a PRESTO generator.

II. BASIC PRESTO ARCHITECTURE

Fig. 1 shows the basic architecture of PRESTO generator. A n -bit PRPG is connected with phase shifter to produce the actual pseudorandom test patterns. PRPG is implemented using a linear feedback shift register, between the PRPG and the phase shifter n hold latches are placed. Each hold latch is controlled by an n -bit toggle control register. The toggle control register controls the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, 0s indicates the latches in hold mode. The toggle mode is transparent for data arriving from the PRPG and their fraction determines a scan switching activity. With the content of an additional shift register the control register is reloaded once per pattern. The weights are determined by four AND gates producing 1s with the probability of 0.5, 0.25, 0.125, and 0.0625, respectively.

The OR gate allows choosing probabilities beyond powers of 2. A 4-bit Switching register is employed to activate AND gates, and allows selecting a user-defined level of switching activity. An additional 4-input NOR gate is used to switch the LP functionality off.

III. FULLY OPERATIONAL PRESTO GENERATOR

This approach splits up the shifting period of every test pattern into a sequence of alternating hold and toggle intervals. To move the generator back and forth between toggle and hold states, a T-type flip-flop is used that switches when there is a 1 on its data input, the generator enters the hold period if it is set to 0 with all latches temporarily disabled regardless of the control register content. This is done by placing AND gates on the control register outputs to freeze all phase shifter inputs. If the T flip-flop is set to 1, the control register enables the latches and pass test data moving from the PRPG to the scan chains.

Two additional parameters kept in 4-bit Hold and Toggle registers to determine how long the generator remains in the hold mode or in the toggle mode. To terminate either mode, a 1 must be given to the T flip-flop input. This weighted pseudorandom signal is produced similar to that of the weighted logic used to feed the shift register. The T flip-flop controls four 2-input multiplexers routing data from the Toggle and Hold registers, allows selecting a source of control data that will be used to change the operational mode of the generator in the next cycle.

When using the PRESTO generator with an existing DFT flow, all LP registers are either loaded once per test or every test pattern. The registers loaded only once act as test data and are triggered using a slow scan shift clock and operate at a very low speed.

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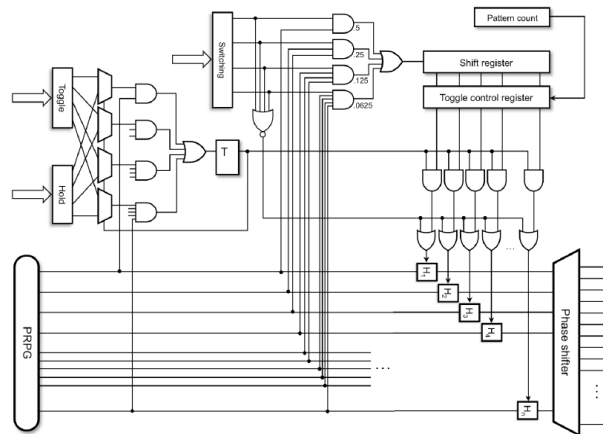


Fig 2. Fully operational version of PRESTO generator

IV. LP DECOMPRESSOR

The principle of the decompressor is to disable both weighted logic blocks (V and H) and to spread out deterministic control data and to facilitate test data decompression. A multiplexer placed in front of the shift register select the content of the toggle and control register. The Toggle and Hold registers are employed to alternately preset a 4-bit binary down counter, and to determine durations of the toggle and hold phases. When this circuit reaches the zero value, it causes a dedicated signal to go high to toggle the T flip-flop. The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state.

Both the T flip-flop and the down counter need to be initialized for every test pattern. The initial value of the T flip flop decides whether the decompressor will begin to operate either in the hold mode or in the toggle mode, while the initial value of the counter, determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases. First, the encoding procedure may completely disable the hold phase by loading the Hold register with an appropriate code, for example, 0000. If detected that there is no Hold signal, it overrides the output of the T flip-flop by using an additional OR gate. Therefore, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle produced at the end of the ring generators initialization phase reload all latches with the current content of this part of the decompressor. Finally, external ATE channels which feeding the original PRPG allows to implement a continuous flow

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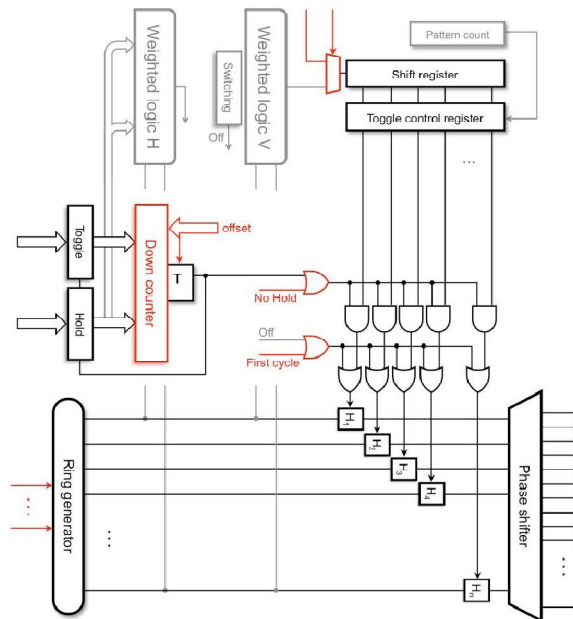


Fig. 3. LP decompressor—modules in gray are disabled. The red items have been added.

of test data decompression such as the dynamic LFSR reseeding. Given the size of PRPG, the number of scan chains and the corresponding phase shifter, the switching code, the offset, as well as the values kept in the Toggle and Hold registers, the entire decompressor will produce the decompressed test patterns having a desired level of toggling provided the scan chains are balanced. The corresponding encoding procedure, including an appropriate selection of the aforementioned parameters contains several steps.

V. ENCODING ALGORITHM

The decompressor architecture is coupled with a compression procedure. The actual toggle rate (TR) percentage, measured as a weighted transition metric, is given by

$$TR = 50(n/S)(T/(T + H)) \quad (1)$$

where n is the number of scan chains, S is the total number of scan chains, and T and H are the durations of toggle and hold periods, respectively. The actual algorithm to yield the desired values of T , H , and O can be summarized as follows,

- 1) Given a test cube and its transitions, find the earliest transition ending point e and assign a single bit toggle phase ($T = 1$) to cycle e .
- 2) Mark all transitions crossing e , as they will not end up within a single hold period.
- 3) Increase the toggle period by extending it up to the next unmarked transition starting point. Repeat this step as long as the duration of the toggle period does not exceed a certain threshold (in this paper, ten cycles).
- 4) Find the next unmarked transition ending point e' —it determines a duration H of the hold period unless H is larger than a certain threshold. In the former case go to step 6, otherwise invoke step 5.
- 5) Find the value of H that minimizes the ratio T/H and, by adding new hold and toggle phases, keeps the cycle e within a toggle period.
- 6) Set the offset period O to $e \bmod (T + H) - H$, if we

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begin with an incomplete toggle period, and $O = \text{emod}(T + H)$, otherwise.

7) Adjust the values of H , T , and O if some of the remaining unmarked transitions lie entirely within a single hold period. Ensure that the sum $T + H$ remains unchanged. The ratio T/H , on the other hand, may vary, thus its minimizing can guide this step toward an optimal solution.

If a scan chain is disabled, then a single expression, produced during the first shift-in cycle, represents all of its cells. On the other hand, if a cell belongs to an active scan chain, then its equation is formed by XOR-ing: 1) the corresponding outputs of the ring generator if they are enabled through the hold latches; and 2) expressions produced during the first shift-in cycle on the disabled ring generator outputs.

This expression will be used provided a scan cell is in the toggle mode. If it enters the hold mode, then its equation is going to be the same as that of the preceding and nearest cell which is in the toggle mode and belongs to the same chain. Since we only use 3-input XOR gates to create a phase shifter, there are seven different scenarios with at least one XOR tap enabled. One can proceed with the test cube encoding after prepared all necessary equations. This is carried out in a manner similar to that of the conventional EDT flow. Another notable difference between the presented approach and the traditional EDT scheme is the way compression aborts are reported. Typically, a test cube is regarded uncompressible if it cannot be encoded when merged as the first component of a test pattern. Here, the test cube is first employed, with other cubes, to form a template, which in turn modifies equations. All compressed test cubes are removed from the cube pool, which is subsequently refilled. The algorithm continues by creating a new set of templates as long as the pool is not empty.

VI. EXPERIMENTAL RESULTS

This section presents experimental results obtained for the PRESTO generator and LP decompressor. The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling levels and it allows to load the scan chains with patterns and low transition counts. Therefore it

significantly reduced the power dissipation. The objective of the second group of experiments was to evaluate the tests produced by a PRESTO generator and determine their fault coverage for various requested toggling rates. The results for one of the industrial designs deployed in this paper is similar to outcomes for a BIST-ready design. The performance of the PRESTO generator remains highly predictable. In particular, with the increasing switching activity single stuck-at fault coverage increases as well. The table I and II presents the area consumption of the PRESTO generator and LP decompressor, table III, IV, V, presents the power consumption of the PRESTO, fully operational and LP decompressor circuits.

TABLE I
AREA CONSUMPTION FOR FULLY OPERATIONAL PRESTO

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	42	3,840	1%	
Number of 4 input LUTs	38	3,840	1%	
Number of occupied Slices	51	1,920	2%	
Number of Slices containing only related logic	51	51	100%	
Number of Slices containing unrelated logic	0	51	0%	
Total Number of 4 input LUTs	38	3,840	1%	
Number of bonded IOBs	24	97	24%	
Number of BUFMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.74			

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TABLE II
AREA CONSUMPTION FOR LP DECOMPRESSOR

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	51	3,840	1%	
Number of 4 input LUTs	32	3,840	1%	
Number of occupied Slices	52	1,920	2%	
Number of Slices containing only related logic	52	52	100%	
Number of Slices containing unrelated logic	0	52	0%	
Total Number of 4 input LUTs	32	3,840	1%	
Number of bonded IOBs	23	97	23%	
IOB Flip Flops	3			
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.57			

TABLE III
POWER CONSUMPTION OF PRESTO GENERATOR

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		43
Vccint 1.20V:	10	13
Vccaux 2.50V:	10	25
Vcco25 2.50V:	2	5
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	2	5
Signals:	0	0
Quiescent Vccint 1.20V:	10	12
Quiescent Vccaux 2.50V:	10	25

TABLE IV
POWER CONSUMPTION OF FULLY OPERATIONAL PRESTO GENERATOR

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		43
Vccint 1.20V:	10	13
Vccaux 2.50V:	10	25
Vcco25 2.50V:	2	5
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	2	5
Signals:	0	0
Quiescent Vccint 1.20V:	10	12
Quiescent Vccaux 2.50V:	10	25

TABLE V
POWER CONSUMPTION FOR LP DECOMPRESSOR

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		41
Vccint 1.20V:	11	13
Vccaux 2.50V:	10	25
Vcco25 2.50V:	1	3
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	1	3
Signals:	0	0
Quiescent Vccint 1.20V:	10	12
Quiescent Vccaux 2.50V:	10	25

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VII. CONCLUSION AND FUTURE WORK

A PRESTO based LP generator can produce pseudorandom test patterns with scan shift-in switching activity precisely selected through automated programming. The same features can be used to control the generator, so that the resultant test vectors can either yield a desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels, or they can offer visibly higher coverage numbers if run for comparable test times. This LP PRPG is also capable of acting as a fully functional test data decompressor with the ability to control scan shift-in switching activity through the process of encoding. The proposed hybrid solution allows one to efficiently combine test compression with logic BIST, where both techniques can work synergistically to deliver high quality test. LP test scheme allows for trading-off test coverage, pattern counts, and toggling rates in a very flexible manner. The future work is to test some benchmark circuits using the generated test patterns and to design an encryptor and decryptor circuit and keys are generated using this test patterns.

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