

VLSI Implementation of a Parallel Turbo-Decoder for Wireless Communication

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ABSTRACT: Wireless sensor network can be considered to be energy constrained wireless scenarios, since the sensors are operated for extended periods of time, while relying on batteries that are small, lightweight and sine expensive. Energy constrained wireless communication application is done with the help of lookup table-log-BCJR (LUT-Log-BCJR) architecture.. In our existing system the conventional LUT-Log-BCJR architecture have wasteful designs requiring high chip areas and hence high energy consumptions Energy constrained applications. This motivated our proposed System the LUT log BCJR is designed with Clock gating technique achieves low-complexity energy-efficient architecture, which achieves a low area and hence a low energy consumption, and also achieving a low energy consumption has a higher priority than having a high throughput. we use most fundamental add compare select (ACS) operations and It having low processing steps, so that low transmission energy consumption is required and also reduces the overallenergy consumption. Our demonstrated implementation has a throughput of 1.03 Mb/s.

KEYWORDS: Lookup table architectures, Clock gating technique, Throughput, ACS block, Transmission energy.

I. INTRODUCTION

Turbo codes received a lot of interest from the research community, as they offer a performance unmatched by any other code so far. Turbo codes are also on the verge of finding their way in numerous cutting edge applications like cellular and satellite communications. A turbo decoder is composed of modules that work in an iterative scheme. Different alternatives exist for the algorithm incorporated in these decoder modules.

Recent Application-Specific Integrated Circuit (ASIC)[1]based turbo decoder architectures have been designed for achieving a high transmission throughput, rather than for low transmission energy. For example, turbo codes have facilitated transmission throughputs in excess of 50 Mbit/s in cellular standards, such as the 3rd Generation Partnership Project 3GPP [2] Long Term Evolution (LTE) and recent ASIC turbo decoder architectures have been designed for throughputs that are in excess of 100 Mbit/s. This has been achieved by employing the Max-Log-BCJR [3] turbo decoding algorithm, which is a low-complexity approximation of the optimal Logarithmic Bahl-Cocke-Jelinek-Raviv (Log-BCJR) algorithm.

The Max-Log-BCJR algorithm appears to lend itself to both high-throughput scenarios, as well as to the above mentioned energy-constrained scenarios. This is because low turbo decoder energy consumption is implied by Max-Log-BCJR algorithm's low complexity. However, this is achieved at the cost of degrading the coding gain by 0.5 dB compared to the optimal Log-BCJR algorithm [4], increasing the required transmission energy E_{tx} by 10%. This disadvantage of the Max-Log-BCJR outweighs its attractively low complexity, when optimizing the overall energy consumption $E_b \cdot \text{prof}$ [5] sensor nodes that are separated by dozens of meters. In Section 2 deals with the proposed algorithm. Section 3 describes about the proposed decoder architecture. Section 4 deals with the results and discussion. Section 5 describes with the conclusion.

II. PROPOSED ALGORITHM

LOG-BCJR algorithm with clock gating technique

There are two main advantages of inducing Log-BCJR algorithm. Firstly, the original BCJR algorithm consists of many multiplication operations which lead to very complex circuits while implementing in hardware. Log-BCJR algorithm avoids the multiplications by transforming the algorithm into the logarithmic domain, where multiplications become additions. Secondly, the values of soft decisions in the normal domain could have a very large dynamic range and theoretically unlimited, which leads to a large amount of memory space in practice. To transfer them to logarithmic domain reduces the dynamic range of the soft decisions and consequently all the internal variables in the algorithm. Hence significantly this approach reduces the memory requirement to implement the algorithm. We use notation y to represent the systematic bits in the encoder including the termination bits, which means $y = [a, e]$, and use y_a to represent the received uncoded sequence LLRs in our BCJR decoder $\{y_n\}_{n=1}^N$.

The conventional LUT-Log-BCJR architecture, which employs the sliding-window technique to generate the LLR sequence b^1 as the concatenation of w equal-length sub-sequences. Each of these windows is generated separately, using a forward, a pre-backward and a backward recursion. These three different recursions are performed concurrently for three different windows. For $w=5$. This schedule results in the completion of the windows in their natural order, starting with that containing the first LLR b^1 and ending with the one containing the last LLR b^1 .

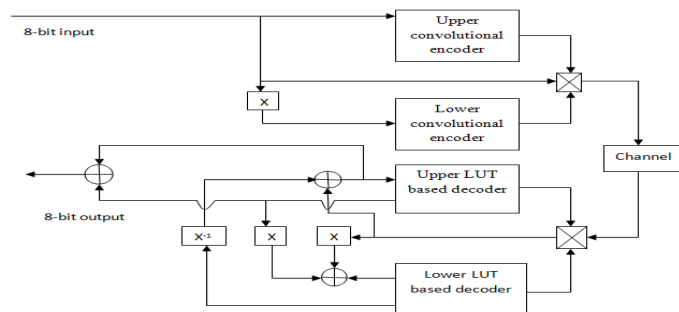


Fig. 1 Conventional lookup table architecture

When the forward recursion is performed for a particular window, one pair of its corresponding a priori LLRs b^1 and b^2 is read from Mem 1 and processed per clock cycle, in the ascending order of the bit index. The forward recursion of the LUT-Log-BCJR algorithm can be performed in two pipelined steps using the corresponding dedicated hardware components.

Clock gating is a technique which is used to control power dissipated by clock input. The disadvantage of the clock gating is that the enable signal is generated by user software. If the protocol can generate the enable signal automatically by itself, the user software will be no need. Any application core can be modeled as a Finite State Machine (FSM) which includes several states like Idle, Ready, Run and so on. The state and the transition of the design will be mapped to the sequential circuit and the combinational circuit respectively.

III. PROPOSED ARCHITECTURE

In the proposed system the lookup table log based architecture is designed with Clock gating technique which leads to reduction in power consumption and energy consumption. The circuit is converted into digital

hardware. The proposed system consists of a novel architecture suits for the energy-constrained scenarios, which avoids the wastage of energy in the conventional architecture. The main work is to redesign the timing of the conventional architecture in a manner that allows the components to be efficiently merged. This produces an architecture comprising only a low number of low-complexity functional units, which are collectively capable of performing the entire algorithm. More wastage is avoided, since the critical paths of the functional units are naturally short and equally lengthened. This eliminates the requirement for additional hardware used for the purpose of managing.

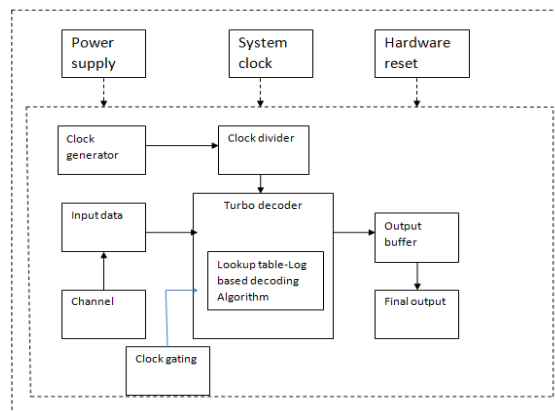


Fig. 2 Proposed system architecture.

IV. RESULTS AND DISCUSSION

At the encoder side the 8-bit data is been generated with the help of Linear Feedback Shift Register, the obtained output is encrypted and finally sent through the communication channel. For the purpose of encryption we use a constant 8-bit code to do the process of “AND”ing with the original bit.



Fig. 3 Waveform of generating random input

In the proposed architecture the clock divider is used to distribute the clock signal to each and every block equally. By implementing this the waiting time of the block for the clock signal can be reduced. This includes clock and reset as input and the clock_divided output signal.



Fig.4 Waveform of clock divider.

The proposed architecture is implemented at the decoder side and carries out the further decoding operation.

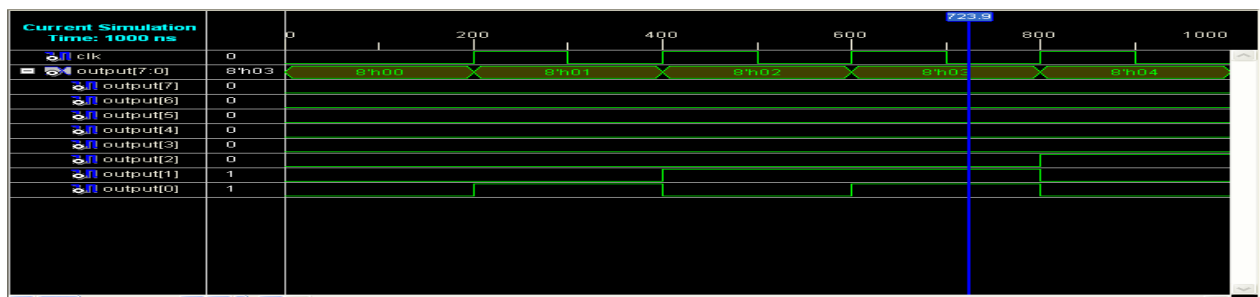


Fig 5 Waveform of counter.

The turbo-encoder that includes the above designed block such as 8-bit input data generation, clock divider and counter for the process of encoding. In this design the input bits are encrypted using XOR operation. Further the code is sent through the channel for the turbo decoder. This turbo encoder uses an interleaver for error detection and correction purpose. The final output waveform

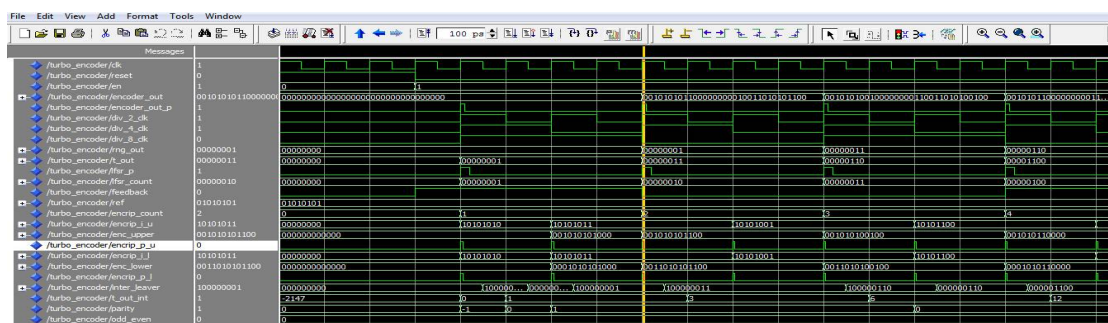


Fig. 6 Output waveform of turbo encoder

V.CONCLUSION

We demonstrated that upon aiming for a high throughput, conventional LUT-Log-BCJR architectures may have a disadvantageous designs requiring high chip areas and hence high energy consumptions. However, in energy-constrained applications, achieving a low energy consumption has a higher priority than having a high throughput. This motivated our low-complexity energy-efficient architecture, which achieves a low area and

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hence a low energy consumption by decomposing the LUT-Log-BCJR algorithm into its most fundamental ACS operations. In addition, the proposed architecture may be readily reconfigured for different turbo codes or decoding algorithms. We validated the architecture by implementing an LTE turbo decoder, which was found, in Table III, to have an order-of-magnitude lower area than conventional LUT-Log-BCJR decoder implementations and an approximately 71% lower energy consumption of 0.4 nJ/bit/iteration. Compared to state of the art Max-Log-BCJR implementations, our approach facilitates a 10% reduction in the overall energy consumption at transmission ranges above 58 m. Furthermore, we demonstrated that our implementation has a throughput of 1.03 Mb/s, which is appropriate for energy-constrained applications, such as in environmental monitoring WSNs.

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