

Online BIST Architecture with Modified SRAM Cells for Testing VLSI Circuits

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ABSTRACT: VLSI circuits are tested using BIST technique which avoids the requirement of external testing equipment. This method achieves simultaneous testing of the circuits under online mode. The aim of proposed project is to design the logic module with SRAM cells to store input test vectors and to reduce the switching activity with reduced testing time and concurrent test latency. The proposed scheme is suitable for all types of IC's.

KEYWORDS: Built-In-Self Test, Active Test Set Generator and Comparator Circuit, Very Large Scale Integrated Circuits

I. INTRODUCTION

BIST technique provides high fault coverage. BIST techniques are typically classified into offline and online. In online mode the circuit operates parallel and makes testing process faster than the previous method. TG is a test pattern generator circuit which is designed to generate random test patterns to test faults in IC and test patterns are moved to MUX with the help of selection line and MUX passes the input vector to the circuit under test (CUT) and AGC is a active test set generator and comparator circuit simultaneously passes the active test set to response verifier and CUT also passes the output response to the response verifier which compares both the vectors and if both the vectors match then it indicates that hit of vector occurs if not then the IC is a faulty one.

AGC: AGC is a active test set generator and comparator circuit which acts as a database to store active test set vectors to verify with the output of circuit under test during testing process.

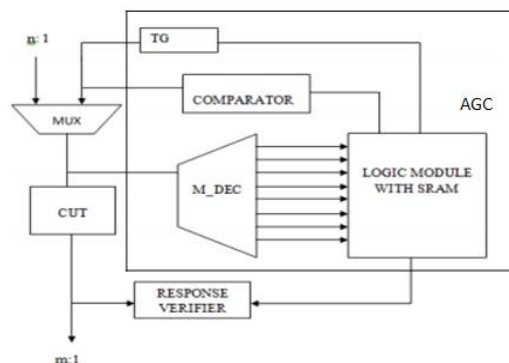


Fig 1. Block Diagram of AGC Unit

CUT: The circuit operates under both the normal mode and test mode. Under normal mode $T/N=0$ and under test mode $T/N=1$. X is a active test vector and then X is verified using response verifier circuit if X matches

then X is removed from the circuit. When all input test vectors perform a hit then it indicates that circuit is a faulty circuit.

LOGIC MODULE: Logic module generates the test patterns to detect the faults and indicate the result to the outputs. As the test pattern generator is a circuit area is limited. Therefore storing and then generating test patterns by ATPG on the CUT using the hardware test pattern generator is not possible. The test pattern generator is a type of register which generates random patterns which act as test patterns. The main aim of the register design is to have low area to generate many different patterns (from 0 to 2^n).

Logic module has the following cases:

- 1) reset of the module
- 2) hit of a vector
- 3) tge operation

RESET OF MODULE: When the circuit is reset to generate the test patterns with tge is enabled. It has two cases,

- 1) Low order bits to drive input of decoder
- 2) High order bits to drive input of comparator.

HIT OF VECTOR: During normal mode, the inputs to the CUT are driven as normal inputs. The n inputs are driven to the CBU as follows: the w low-order inputs are passed to the inputs of the decoder; the k high-order inputs are passed to the inputs of the comparator circuit. When a vector belongs to the current circuit reaches the inputs of the CUT, the comparator is enabled and one of the output of the decoder is enabled.

TGE OPERATION: When all the cells value are equal to 1 then the value of the w-stage counter is all 1. The activation of the rve signal to the counter to overflow and in the next clock cycle through the unit flop delay the tge signal is enabled and all the cells value to all the outputs of the decoder are enabled and are set to zero.

MODIFIED DECODER: Tge is enabled all outputs of decoder = 1.

Cmp is disabled all outputs are disabled.

Tge is enabled and comparator is enabled.

II. RELATIVE WORK

1. Structural on-line self-test was performed to detect permanent faults and avoid their accumulation in the circuit[1]. This method improves concurrent BIST techniques based on a deterministic active test set. Here, the test patterns for testing are especially generated with a specified number of smaller bits. This results in very low test latency, which reduces the fault accumulation. Experiments with a large number of circuits show that the hardware overhead is comparatively lower than the overhead for previously used testing methods. Dormant faults and subsequent fault accumulation can decrease the system reliability and also require additional on-line testing techniques.

2. Concurrent Error Detection (CED) in a popular method of asynchronous controllers as Burst-Mode machines[3]. These clock-less circuits, including the use of redundancy to check hazard-free operation, and to explain how they limit the applicability of traditional CED methods, such as duplication in the testing method.

3. This method of modular CIS sub-array is proposed with new account and to control scheme. It needs only one micro-bump per sub-array and instead of per-pixel or per-column and to release the design rule restriction of the 3D stacking process in the testing of VLSI circuits. The proposed structure with in-pixel two-dimensional (2D) decoding function makes high spatial resolution, without affecting the frame rate of testing process[7].

4. A input-vector monitoring concurrent BIST technique with self-testing RAM for combinational circuits are termed as R-CBIST. This technique compares the other input vector monitoring concurrent BIST techniques proposed previously with aim of hardware overhead, and the time taken for the concurrent test to be completed is called as concurrent test latency. R-CBIST can be used to test ROM because it results in small hardware overhead and whereas there is no need to stop the ROM normal operation in VLSI testing process.

5. A vector hit occurs only if the input vector matches any one of the active test vectors in response verifier. In this method[9], the LFSR is performed to hit proceeds to the next state in the circuit by modifying

the number of active test set vector and the corresponding MISR is enabled to one to activate the modified decoder.

III. MODIFIED SRAM CELLS

SRAM is a type of semiconductor memory cell that uses bistable latching circuit to store each bit in the memory cell. Two types of SRAM cells are there one is static (SRAM) and another dynamic (DRAM). The dynamic RAM (DRAM) must be periodically refreshed. SRAM exhibits a data stability, but it is volatile in the conventional sense amplifier and that data is automatically lost when the memory cell is turned off. The power consumption of SRAM varies widely depending on how frequently it is used and it is termed as power-hungry as DRAM, when it is used at high frequencies, and some IC's can consume many watts at full bandwidth of power. Static RAM in applications such as moderately clocked microprocessors, consumes little power and can have a less power consumption of a few micro-watts.

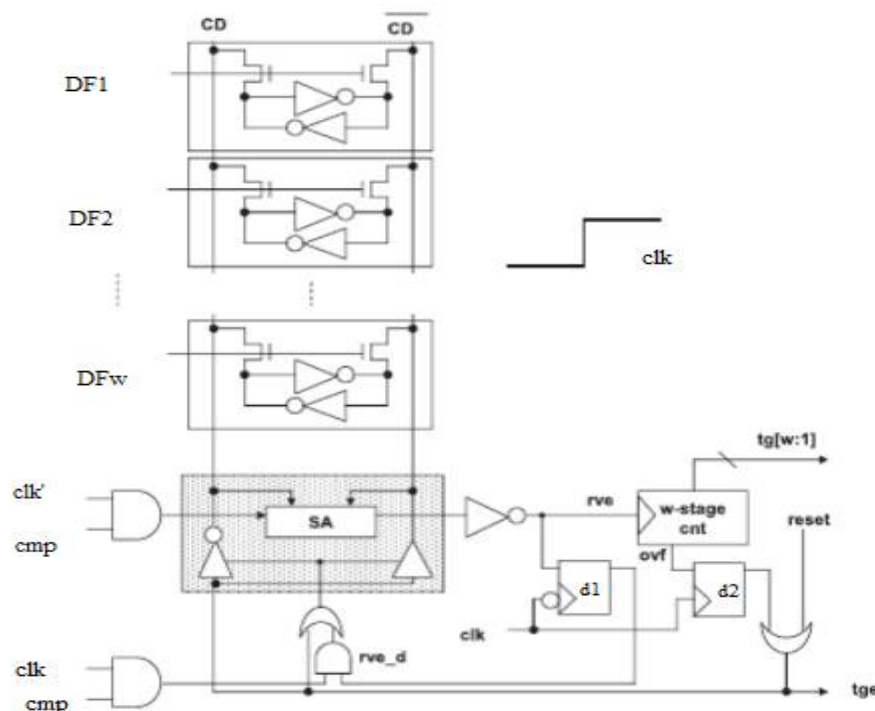


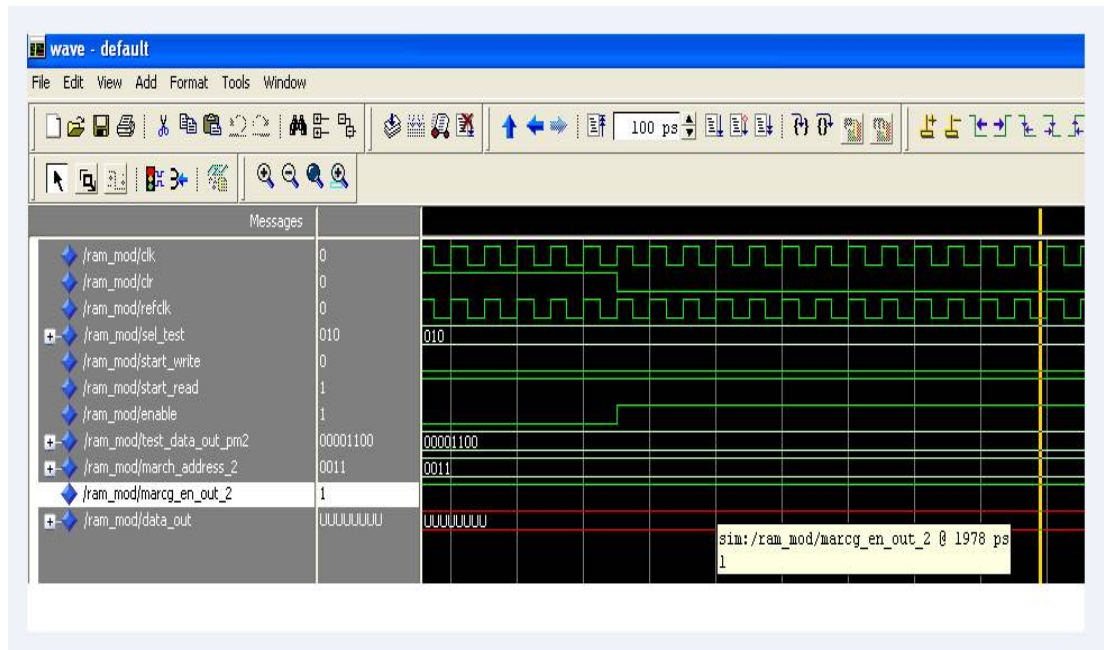
Fig 2. Modified SRAM cell Design

A 10T SRAM cell consists of 10 transistors from which four are pull-up transistors (PUS1, PUS2, PUT1 and PUT2), four are pull down transistors (PDS1, PDS2, PDT1 and PDT2) and two are access transistors (PQR and PXY). The two pulldown transistors i.e. PDS1 and PDT1 are connected to VGND. This VGND signal is connected to gnd during the read_operation else to VDD. The access transistors are connected to pseudo nodes (PQ and PQb i.e. nodes between two pull-up transistors) but not to the storage nodes (i.e. Q and Qb). Due to this operation, the storage nodes are changed from the BLs and therefore during the read_operation of the circuit, the current flows through the storage nodes and hence maintain the read mode stable. Whereas in case of the write_operation, the VGND is connected to VDD and any one of the bit-lines e.g. BL is in gnd. Suppose the

node Q is storing '1' value and node Qb is storing '0' value. When a high supply voltage is supplied, the node Q value is pulled down to '0' value and then due to discharging through the access transistor the pull-up transistor i.e. PGL and PUL2.

IV. EXPERIMENTAL RESULTS

The input data are transmitting through multiplexer module. A decoder is a combinational logic circuit that takes a binary input, usually in a binary coded form, and produces a one-bit output logic, on each of a number of output lines. The logic state (1 or 0) values appear on any of the output lines depends on a particular code value appearing on the input lines. In our proposed work, the decoder input data or information is addressed and that can be transmitted through the through SRAM cell to the destination address.



V. CONCLUSION

Input vector monitoring concurrent BIST method performs testing during the normal operation of the circuit without imposing a need to set the circuit into offline to perform the testing process, therefore they can have some problems appearing in offline BIST techniques like delay in testing process and more power consumption. The evaluation criteria is the hardware overhead and the CTL, i.e., the time required for the test to complete, while the circuit operates in normal mode. A concurrent BIST architecture for online testing based on the use of a SRAM-cell like structure for storing the data whether an input vector has appeared or not during normal operation of the circuit. The proposed scheme is more efficient than previous method of input vector monitoring concurrent BIST techniques in testing of VLSI circuits

REFERENCES

[1]Ioannis,CostasEfstathiou "Concurrent self test with partially specified patterns for low test latency and overhead," IEEE Transaction on very large Scale integration system, vol. 22, no.7, July 2014.

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- [2] S. Almukhaizim and Y. Makris, "Test challenges for 3D integrated circuits using ring oscillators," IEEE Trans. Comput., vol. 56, no. 6, pp. 785–798, Jun. 2007.
- [3] I. Voyiatzis and C. Halatsis, "Test pin methodology, architecture and circuits for testing in 3D stacking ic systems," IEEE Trans. Dependable Secure Comput., vol. 2, no. 2, pp. 150–156, Apr. 2005.
- [4] R. Sharma and K. K. Saluja, "Theory, analysis and implementation of an on-line BIST technique," vol. 34, no. 9, May 1993.
- [5] K. K. Saluja, R. Sharma, and C. R. Kime, "Concurrent comparative built-in testing of digital circuits," Dept. Electr. Comput. Eng., Univ. Wisconsin, Madison, WI, USA, Tech. Rep. ECE-8711, 1986.
- [6] J. Rajski and J. Tyszer, "Test responses compaction in accumulators with rotate carry adders," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 12, no. 4, pp. 531–539, Apr. 1993.
- [7] M. A. Kochte, C. Zoellin, and H.-J. Wunderlich, "Concurrent self-test with partially specified patterns for low test latency and overhead," in Proc. 14th Eur. Test Symp., pp. 53–58, May 2009.
- [8] J. Rajski and J. Tyszer, "Test responses compaction in accumulators with rotate carry adders," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 12, no. 4, pp. 531–539, Apr. 1993.
- [9] S. Almukhaizim, P. Drineas, and Y. Makris, "Entropy-driven parity tree selection for low-cost concurrent error detection," IEEE Trans. Comput. Aided Design Integr. Circuits Syst., vol. 25, no. 8, pp. 1547–1554, Aug. 2006.
- [10] I. Voyiatzis, A. Paschalis, D. Gizopoulos, N. Kranitis, and C. Halatsis, "A concurrent BIST architecture based on a selftesting RAM," IEEE Trans. Rel., vol. 54, no. 1, pp. 69–78, Mar. 2005.