

Design and Implementation of 4 - QAM VLSI Architecture for OFDM Communication

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ABSTRACT: In this paper, 4 - QAM (Quadrature Amplitude Modulation) is preferred for OFDM (Orthogonal Frequency Division Multiplexing) based wireless communication system. Among various digital modulation schemes, the choice of QAM is to provide both phase and amplitude modulation. The use of 4 – QAM in this project overcomes the drawbacks of higher order QAM's like 16 QAM, 64 QAM, etc. It has higher data rate with lesser bandwidth and thereby reducing the area and power consumption. The noise in 4 – QAM could be overcome by the use of OFDM.

KEYWORDS: Quadrature Amplitude Modulation (QAM), Orthogonal Frequency Division Multiplexing (OFDM).

I. INTRODUCTION

Communication system uses several digital modulation techniques like PSK (Phase Shift Keying), ASK (Amplitude Shift Keying) and QAM (Quadrature Amplitude Modulation), etc. Above all these, the present digital communication system prefers QAM because it has the capability of modulating both the amplitude and phase of the carrier signal [1]. Hence it is a combination of both ASK and PSK. QAM uses the same frequency band, where each carrier may be adjusted independently and transmitted through the same frequency since the carrier signals of QAM are orthogonal. QAM provides higher data rate for transmission. It is used in many applications such as radio communication, TV Broadcasting, Wi-MAX, OFDM (Orthogonal Frequency Division Multiplexing) and satellite communication.

The Inter Symbol Interference (ISI) caused by digital modulation technique can be eliminated by using OFDM[2]. It is a digital multi-carrier modulation scheme that extends the concept of single subcarrier modulation by using multiple subcarriers within the same signal channel. It is less sensitive to frequency selective fading. The basic principle of OFDM is gaining a wide spread popularity within the wireless transmission community. Furthermore OFDM is one of the main techniques proposed to be employed in the 4th Generation wireless system. QAM, Quadrature amplitude modulation is widely used in many digital data radio communications and data communications applications. A variety of forms of QAM are available and some of the more common forms include 16 QAM, 32 QAM, 64 QAM, 128 QAM, and 256 QAM. Here the figures refer to the number of points on the constellation, i.e. the number of distinct states that can exist.

[3] Proposed design for a 16-QAM transmitter and receiver based on the Virtex4 FPGA Kit. They focused on carrier synchronization, time synchronization, and adaptive equalization. They designed a complete baseband IF 16-QAM system. In [4] the design and implementation of 4/8/16/32/64 Quadrature Amplitude Modulation (QAM) and demodulation in FPGA using Partial Re-configuration was carried out. Partial reconfiguration is a technique or the ability of a reconfigurable hardware to modify logic blocks dynamically without interrupting the system by downloading smaller bit files. Control register was introduced to switch between different QAM modulations. Virtex 6 was used to implement modem. But in this concept, power optimization in implementation is not achieved. The 4-QAM reduces the consumption of area and when implemented in

hardware in FPGA boards, the number of registers used will be less [5]. This is the most required characteristic feature from VLSI technology.

Paper is organized as follows. Section II describes the methodology of designing the modulator and also the concept of constellation diagram. Algorithm concept for the multiplier is described in Section III. Section IV presents experimental results showing simulation. Finally, Section V presents conclusion.

II. RELATED WORK

QAM is a method for sending two separate (and uniquely different) channels of information. The carrier is shifted to create two carriers i.e., sine and cosine. The serial to parallel converter accepts the data to be transmitted assembles them in blocks of M-bits and then separates them into N-channels. In case of 4-QAM the four bits are separated into 2 bits each and then sent to the binary multiplexer which is shown in Fig.1.

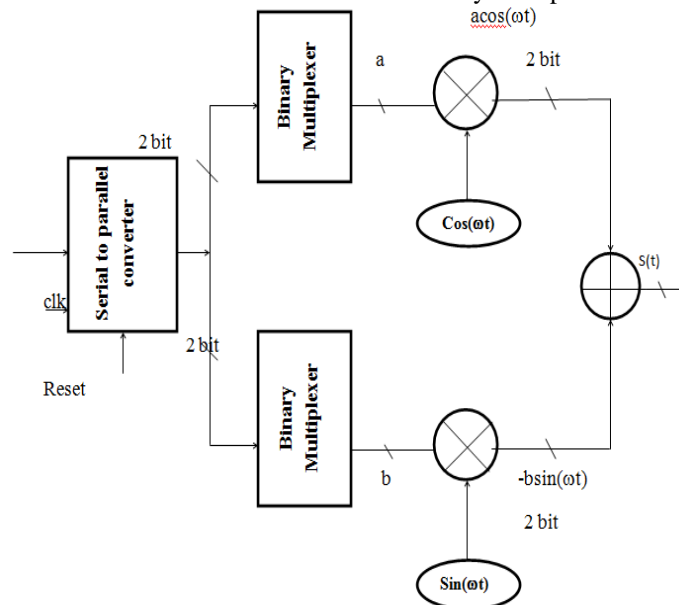


Fig.1.QAM modulator

The carrier waves are modulated in amplitude by a multilevel signal which through a multilevel binary converter generates the levels often 'a' and 'b' according to the number of binary input. The two modulated inputs are applied to two separate balanced modulators each of which are supplied with the sine or cosine carriers i.e., Modulator - 1 is supplied with a cosine carrier and Modulator - 2 is supplied with sine carrier. The result of the sum of these signals is a signal modulated both in phase and quadrature. It is denoted by S(t) and expressed in Equation.1.

$$S(t) = a\cos(\omega t) - b\sin(\omega t) \quad (1)$$

As this work concentrates on reducing the power consumption and delay, Booth multiplier is used. Booth multiplier is superior in all the aspects like speed, delay, area, complexity, power consumption whereas Array multiplier and Wallace tree multiplier are less efficient than the Booth multiplier. Some of the parameters are tabulated in Table.1. For low power requirement and less delay requirement, Booth Multiplier is used. The output signals from the modulator (multiplier) is summed up using the adder circuit. Out of several adders, the Carry Increment Adder is preferred since it compromises delay, area and power consumption. The coding is developed for each of the blocks in QAM modulator and are merged together. The simulated result is interpreted in Xilinx Vivado.

Parameter	Array Multiplier	Wallace Tree Multiplier	Booth Multiplier
Speed	Less	High	Highest because the cycle length is small as possible
Time Delay	More	Less	Lesser
Power Consumption	Highest	High	Low
FPGA Implementation	Less Efficient	Not Efficient	Most Efficient

Table.1. Comparison of Multipliers

The architecture diagram of a QAM modulator is mounted according to the discrete levels produced by the converter. Thus in a QAM modulator of two bits have only four points in the constellation, so this modulator is called as 4 QAM. There are several ways to implement the QAM constellation. The format of the constellation is determined by the conversion of angle which is given in Fig.2.

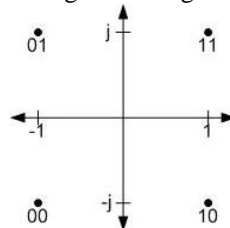


Fig.2. Constellation Diagram of 4 QAM

The input of encoding a number of binary bits is that the output generates two binary numbers one on phase and another on quadrature.

III. ALGORITHM

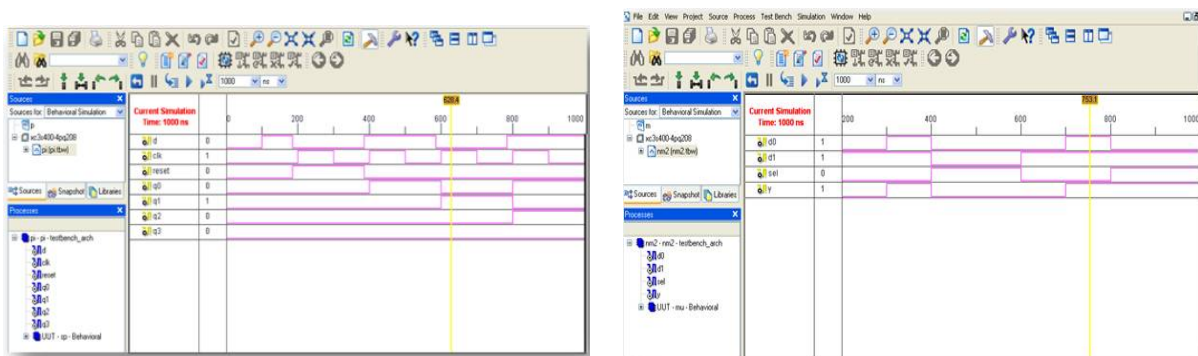
The Booth algorithm steps are summarized as follows.
 Find $3 \times (-4)$, with $m = 3$ and $r = -4$, and $x = 4$ and $y = 4$
 $m = 0011$, $-m = 1101$, $r = 1100$
 $A = 0011\ 0000\ 0$
 $S = 1101\ 0000\ 0$
 $P = 0000\ 1100\ 0$

Perform the loop four times:

P = 0000 1100 0. The last two bits are 00.
 P = 0000 0110 0. Arithmetic right shift.
 P = 0000 0110 0. The last two bits are 00.
 P = 0000 0011 0. Arithmetic right shift.
 P = 0000 0011 0. The last two bits are 10.
 P = 1101 0011 0. $P = P + S$.
 P = 1110 1001 1. Arithmetic right shift.
 P = 1110 1001 1. The last two bits are 11.
 P = 1111 0100 1. Arithmetic right shift.
 The product is 1111 0100, which is -12.

IV. EXPERIMENTAL RESULTS

Figures show the simulation results which are simulated in Xilinx software. Fig 3 (a) shows result of serial to parallel converter (b) is the simulated result of 2:1 multiplexer and (c) is the combined result of serial to parallel converter and multiplexer.



(a)

(b)



(c)

Fig.3.Simulated Results (a) Serial to Parallel converter (b) 2:1 Multiplexer (c) Combined output of serial to parallel converter and 2:1 multiplexer.

The final output in the Fig.4. is the modulated output which is obtained by combining all the blocks of the modulator which are serial to parallel converter, 2 to 1 multiplexer, multiplier and adder.



Fig.4.Simulation Result of 4-QAM Modulator

V. CONCLUSION

The VHDL coding is developed for each block in the above shown block diagram. Then, the blocks are combined one by one and the final modulated output is obtained. Thus 4 QAM VLSI architecture is designed which is the most appropriate digital modulation scheme for OFDM based wireless broadband communication system since it contains higher data rate with less bandwidth. Hence it reduces the circuit complexity, area and power in the reconfigurable hardware. Also the noise interference is minimized with OFDM technique, the 4th generation wireless communication system. The implementation of this architecture provided advantages of technology mapping in terms of time, area and power consumption.

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