

A Combination of Low Power TPG and LFSR with FPGA Implementation

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ABSTRACT: In our project, we propose a novel architecture which generates the test pattern to reduce switching activities. The more power consumption can create problems such as immediate power endurance that cause circuit damage, difficulty in performance authentication, and reduce the product field and life time. LP-TPG (Low Power Test Pattern Generator) structure consists of m-bit counter, low power linear feedback shift register (LP-LFSR), NOR-gate structure, gray counter, and XOR-array. Different types of techniques are presented in the literature to control the power consumption. These paper includes algorithms for test scheduling with minimum power, techniques to reduce more power, techniques for reducing power during BIST(Built-In Self-Test) technique. The generated test patterns are used to test the synchronous pipelined 4x4 and 8x8 Braun array multipliers.

KEYWORDS: FPGA,BIST,LP-LFSR,TPG,XOR-array

I. INTRODUCTION

Power dissemination has become a design objective in many applications such as wireless communication and high performance computing, thus leading to production of numerous low-power designs. At the same time, power dissemination is also becoming a dangerous parameter during manufacturing test, as the design can consume more power during test than during functional mode of operations. As manufacturing harvest are often affected by test power, test methodologies have emerged over the past decade.

We discuss issues arising from excessive power consumption during test application as well as provide structural and algorithmic solutions that can be used to increase the low power test problems .In the literature, techniques that reduce power utilization[1] during test application are generally referred to as power-aware testing, power- constrained testing, or low power testing. Test currently ranks among the most important issues in the development process of an IC. These terms will be interchanged for use throughout the chapter whenever fit with the advance in semiconductor manufacturing technology, a VLSI device can now contain tens to hundreds of millions of transistors. The issues that center on test are manufacturing harvest, product quality, and test cost. To address these test issues, Design-for- Testability (DFT) techniques have become broadly used in industry since the 1990's. Traditionally, these techniques are mainly employed to correct the circuit's fault coverage, test application time, test development efforts. The recent advances in low power design techniques and manufacturing technologies have spurred the rapid growth of electronic products into consumer markets using laptops, mobile phones, audio and video based multimedia products, energy-efficient pc's, etc. These new products make power management a critical issue that needs to be considered circuit design and test development. The main aim for considering power consumption during test is that generally, a circuit consumes much more power in test mode than in normal mode. The test power will be more than twice the power consumed in normal functional mode. There are many reasons that could explain this increase in test power. First, TPG tools tend to generate test patterns with a high toggle rate in order to decrease pattern count. Second, parallel testing is often used to reduce test application time, particularly for SOC device [2]. This parallelism

increases power dissipation during test. Third, The DFT circuitry inserted in the circuit to check test issues is often idle during normal operation but may be intensively used in testmode.

II. REVIEW OF PREVIOUS WORK

Several techniques are available to shrink the switching techniques of test pattern, which reduce the power in test mode. LP-LFSR can reduce the average power compared to traditional LFSR. A low power can be achieved by using single input change pattern generators. It is proposed that the LFSR [2] is used to generate random single input change sequences. It is proposed that single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. The normal and high powers are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high. Girard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched. S.K.Guptha proposed a BIST [3], TPG for low switching activity in which there is clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by initial LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce power.

III. ANALYSIS OF POWER FOR TESTING

In CMOS technology, the power dissemination can be classified into static and dynamic. Static power dissemination is mainly due to the leakage current. Dynamic power dissemination is due to switching transient current and charging and discharging of load capacitances [4]. Some important parameters for calculating the power consumption of CMOS circuits are discussed in equation(1).

$$E_i = [V_{dd}]^2 C_0 F_i S_i \quad (1)$$

Where V_{dd} is the supply voltage, C_0 is the load capacitance, F_i is input frequency, S_i is static power. The average power consumption of internal circuit can be given in equation(2),

$$P_i = [V_{dd}]^2 C_0 F_i S_i \quad (2)$$

IV. BIST APPROACH

BIST is a mechanism that allows a semiconductor device to test itself. Since testing is built into the hardware, it is faster and valuable. The BIST architecture required three additional appliances such as a pattern generator, a response reviewer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a LFSR [5]. A response reviewer is a compressed with stored responses or an LFSR used as an indication analyzer. A controller provides a control signal to energize all the blocks. BIST has some major disadvantages where architecture is based on the LFSR. The circuit introduces more switching activities in the CUT. It causes more power dissemination, the average and peak power of a circuit during test. The techniques can minimize the average power compared to traditional LFSR. A low power can be obtained by using single input change pattern generators. It is proposed that the LFSR is used to generate random single input change sequences. It is proposed that single input change test vectors can be inserted between two adjustment vectors generated by LFSR. It is proposed that single input changing data is inserted between two neighboring seeds. Still, the switching activities will be large when clock frequency is high.

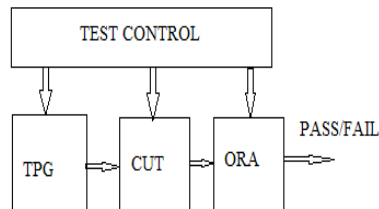


Figure:4.1. Block diagram of BIST

CUT - Circuit Under Test
TPG - Test Pattern Generator
ORA - Output Response Analyzer

As shown in the above figure, test control is used to send the input clock signal to all the blocks which includes TPG, CUT, ORA to energize them. Input signals from TPG are passed to CUT to test and the ORA is used to analyze the output signal.

V. BASIC FAULT MODELS

- The stuck-at fault model- A signal is stuck at a 0 or 1 value, independent of the inputs to the circuit.
- The bridging fault model- Depending on the logic circuit employed, this may result in a wired-AND or wired-OR logic function.
- The transistor faults- This model is used to explain faults for CMOS logic gates. At transistor level, a transistor maybe stuck-short and stuck-open. In stuck-short, a transistor behaves as it is always conducts and stuck-open is when a transistor never conducts current. Stuck-short will produce a short between power supply and ground.
- The open fault model- Here a wire is assumed to be damaged, and one or more inputs are disconnected from the output that should drive them.
- The delay fault model- In which the signal eventually assumes the correct value, but more slow comparing to normal.

VI. CLASSIFICATION OF STRATEGIES

6.1. Weighted Pseudorandom testing: Here, pseudorandom arrangements are applied with certain 0s and 1s distribution in order to handle the random test pattern resistant fault which is imperceptible by the pseudorandom testing. Thus, the test length can be effectively shortened.

6.2. Pseudo exhaustive Testing: This type divides the DUT into several smaller sub circuits and tests each of them completely. All detectable flaws within the sub circuits can be detected [3]. However, such a method involves additional design effort to partition the circuits and deliver the test responses as well as test patterns. BIST is a set of structured-test techniques for combinational and sequential logic, multipliers, memories, and other embedded logic blocks. BIST is the habitually used design technique for self- testing of circuits.

6.3. Pseudorandom Testing: It involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a confined order. The test length and the contents of the patterns are used to impart fault coverage.

6.4. Exhaustive Testing: This testing pattern involves the application of all possible input combinations to the design under test (DUT). It GUARANTEES that all detectable faults that avert from the sequential behavior will be detected. The procedures are often applied to complex and well abandoned small modules such as PLAs.

6.5.Stored Patterns: This pattern approach tracks the pre-triggered test patterns to achieve certain test goals. It is used to amplify structure level testing such as the switch-on self- test of a computer and microprocessor functional testing using micro programs.

VII. PROPOSED METHOD

Historically, verification engineers uses pseudo random test pattern generation method to verify the functionality of their design. Purely random stimulus takes too long to generate interesting scenarios, so it will consume more time and power. Specifying the interesting subset of all possible stimulus with the constraint blocks and generating the interesting scenarios is known as constraint random pattern generation. By specifying the constraints, one can easily develop tests that can find hard-to-reach corner cases.This will reduce the power consumption in the digital circuit and speed up the verification cycle to catch the bug quicker. Also it will help to achieve the concept of time to market.

In addition to this, the development of Intellectual Property (IP) cores for the FPGAs for a variety of standard functions including processors, facilitate a multimillion gate FPGA to be configured to contain all the components of a platform based FPGA. Processors are far more flexible than the hard-core processors and they can be enhanced with custom hardware to advance them for specific application. Power dissipation is a challenging problem for today’s System-on-Chips (SOCs) design and test.

7.1.Test pattern generator

Because of easiness of the circuit and less area occupation, LFSR is used at the maximum for generating test patterns. We proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of mutated low power linear feedback shift register (LP-LFSR), graycounter,m-bit counter, XOR-array and NOR-gate structure XOR-array.

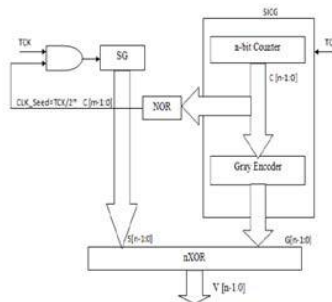


Figure:7.1.1:LP-TPG

The m-bit counter generates 2^m test in sequence and is initialized with Zeros. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to NOR-gate structure and gray code generator. When the NOR-gate output is one the clock signal is applied to activate the LP-LFSR and on the other hand, when all the bits of counter output are Zero, the NOR-gate output is one. Which generates the next seed as shown in fig:5.2.1. The data generated from the gray- code generator is Exclusive-ORED with the seed generated from LP-LFSR. The patterns generated from the Exclusive-OR array are the final output patterns.

7.2. Braun array multiplier

Multipliers are broadly used in DSP operations such as convolution for filtering, correlation and filter banks for multi rate signal processing.Without multipliers, no calculations can be done in DSP applications. For that reason, multipliers are picked for testing in our proposed design. Braun array multiplier is chosen among different multipliers as it follows simple conventional method. Also, pipelined Braun array multiplier is picked

as it is faster in speed than non-pipelined multiplier. To obviate carry propagation delay at every stage, the carry bits are propagated to the next stage. At the last stage, ripple carry adder is utilised to get the product term of p4 to p7.

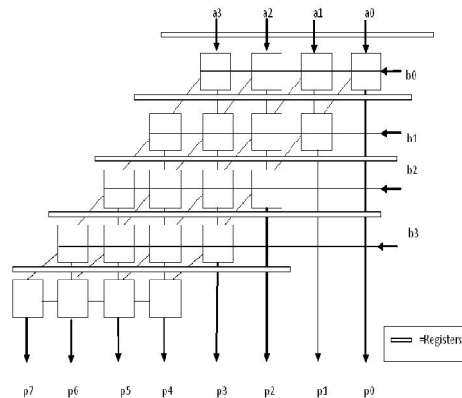


Figure7.2.1: Braun array multiplier

7.3. LP-LFSR

LFSR are used widely in data shrink circuitry, encryption circuitry, BIST, communication circuitry and fault correction circuitry. We consider only LFSR, which consist of D-flip-flops connected serially. The output of these is XORed together and fed back to the first flip-flop. Here the length of the LFSR (the number of flip-flops), which is denoted by N and the number of taps are XORed, which is denoted by M. Power consumption in the serial architecture is high as all the flip-flops are changed in every clock cycle and only one bit of information is produced per clock cycle. The output can be chosen from the input or output of any flip-flop. When the output of successive cycles are generated in one cycle then the LFSR is anti-output.

7.3.1. Algorithm for LFSR

Input patterns from the system and the expected output values are fed into the output response analyser to check whether the compared output is fault free.

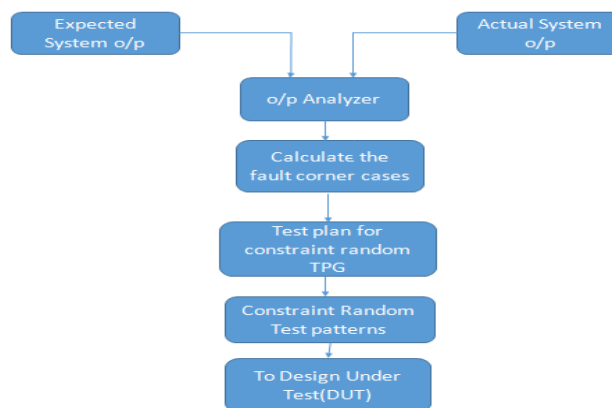


Figure:7.3.1.1:Flow chart for LFSR

The signal coming from the output analyzer is faulty and is thus sent to the next block to calculate the fault corner cases. Then the planning of constrained pseudo random TPG takes place and then for detecting the bug we pass signal to the TPG to test the CUT.

VIII. IMPLEMENTATION DETAILS

To certify the effectiveness of the proposed method, we choose TPG using conventional LFSR for comparison with proposed system. The generated test patterns from above two techniques are used to test the synchronous pipelined 4x4 Braun array multipliers.

Power analyzer tool was used for the power analysis. The average test power consumption was compared with the TPG using conventional LFSR.

IX. RESULT AND DISCUSSION

9.1. Simulation Results

The following chapter consists of all the software and hardware results observed in the project. The results include snapshots of top module with the inputs, outputs and intermediate waveforms which is shown in fig 7.1.1 and fig 7.1.2..

9.1.1. Pseudorandom test

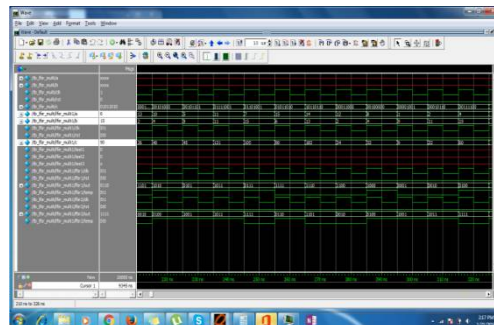


Figure: 9.1.1.1. Simulated output

9.1.2. Constrained pseudorandom test

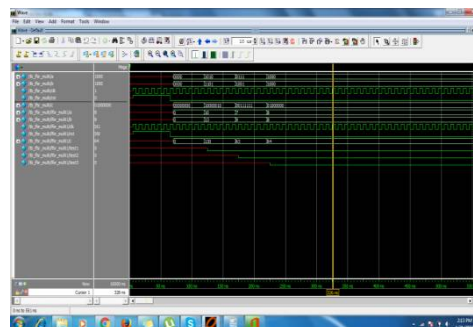


Figure: 9.1.2.1: Simulated output

IX. CONCLUSION

An effective low power test pattern generator (LP-TPG) method had been proposed to reduce the test power and uses a modified constrained pseudo-random pattern generator to produce seeds and then operates with the single input changing generator and an exclusive-OR array, thus constrained pseudo-random signal input changing sequences are generated, which greatly minimize the switching activities and test power. LP-TPG also reduces the instantaneous power violation compared to conventional LFSR.

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