

# Low Power Implementation of Launch-Off-Shift and Launch-Off-Capture Using T-Algorithm

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**ABSTRACT:** The testing architecture is mainly used in all type of real world application architectures and thus the architecture is to modified based on the enhancement purpose.The VLSI technology is to optimize the any type of testing architecture.So the modification process is used to the VLSI technology.Nowadays the design and testability process is mainly important for the any large screening VLSI circuits. In existing system they develop the different DFT mechanisms,one for launch –off shift ,one for launch –off capture and one for mixed at speed testing.Because more power consume the launch- off capture and launch –off shift operation in VLSI testing circuits.Our proposed system is T– algorithm based enhance test sequence architecture.T-algorithm is used to identify the fault in the circuit and reduce the clock function.A scan sequence for one block is likely to detect fault in other blocks.So we optimize the test pattern using modified algorithm.It does not require scan enable to change the speed.It reduce the power consumption.

**KEYWORDS:** T-algorithm,Launch off capture,Launch off shift

## I. INTRODUCTION

The purpose of testing is to discover errors. Testing is the process of trying to discover every conceivable fault or weakness in a work product.It provides a way to check the functionality of components, sub-assemblies, assemblies and/or a finished product. It is the process of exercising software with the intent of ensuring that the Software system meets its requirements and user expectations and does not fail in an unacceptable manner. There are various types of test. Each test type addresses a specific testing requirement. High-quality screening of VLSI circuits by targeting performance-related faults.It is scan based testing sequence using T-algorithm.The scanning sequence first target the faults and detect the fault in the circuit using T-algorithm.It reduce peak power.

## II. RELATED WORK

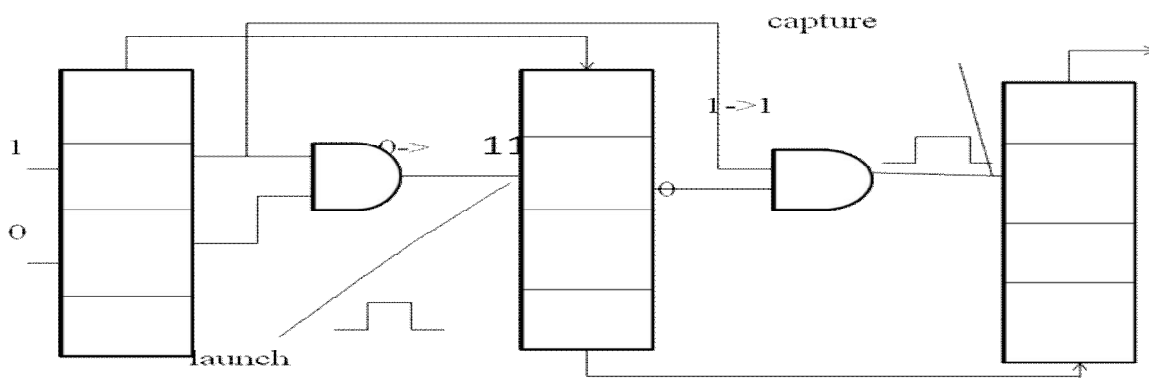
### DESIGN FOR TESTABILITY METHOD:

The proposed system is used to the T-algorithm, to optimize the testing architecture for the required test patterns and to develop the accuracy for testing architecture. The proposed system consists of the secure testing architecture and includes the sticky comparator architecture. So the modification process applied by the sticky comparator and over all architecture. The proposed technique to check the scanning results for the testing process. Inserting scan into a secure design implies new approaches of the technique eventually; applying ones of these counter measures has also proven that at a suitable cost, scan and security can live together. In this paper we do not give the expected outputs. But in the scan circuit to generate the expected values by using TPG. Here linear feedback circuit used for TPG (Test pattern generator). The proposed

approach is based on the idea of withholding information. The idea is to compare test responses within the chip. Both input vectors and expected responses are scanned into the circuit and the compare between expected and actual responses is done at vector level. It does not provide information on the value of every individual scan bit for security purposes. In this paper we proposed a novel DfT technique for scan design to ensure security not including relying on costly test infrastructures to switch from mission to test modes. Design for testability (DfT) makes it possible to: Assure the detection of all faults in a circuit Reduce the cost and time associated with test development Reduce the execution time of performing test on fabricated chips we will focus on DfT techniques for digital logic, although it is relevant for memory and analog/mixed-signal components as well. An example chip level DfT technique is called Built-in self-test (BIST) (used for digital logic and memory.) At the system level, DfT includes boundary scan and analog test bus. The DfT techniques discussed focus on improving testability of SAFs. DfT for other fault models, e.g., delay faults, is described in the literature.

**LAUNCH-OFF-CAPTURE :**

The test pattern is to apply the launch and capture process during the testing operation. To implement the launch off capture block into the load state. Region interface registers can be restored back to their load state upon launch and capture. DfT support that can restore the load state in interface registers in between the launch and capture operations in the design regions.



Main transition fault ATPG methodologies are Launch on Capture and Launch on Shift (also known as broadside-load and skewed-load respectively). They both launch transition at the input of combinational block in different way for the same fault detection. Two vectors V1 and V2 are used to perform transition delay fault testing. Here describes the LOC waveform. As illustrated, last shift of scan chain initialize the inputs of combinational block and first functional clock is used to launch transition in the combination block. Then scan enable signal would assert. Example, for scan chain having N scan-length, in LOC, first vector of N bit is loaded in to scan chain by N slow clock. Then two fast clocks (functional clock) are used to launch and capture transition into and from the combinational block. Again scan chain unloads with N slow clocks. Here scan enable signal transit from high to low after last shift of loading process. Capture-safety, defined as the avoidance of any timing error due to unduly high launch switching activity in capture mode during at-speed scan testing, is critical for avoiding test induced yield loss. Although point techniques are available for reducing capture IR-drop, there is a lack of complete capture-safe test generation flows. The paper addresses this problem by proposing a novel and practical capture-safe test generation scheme, featuring reliable capture-safety checking and effective capture-safety improvement by combining X-bit identification & X-filling with low launch switching- activity test generation. This scheme is compatible with existing ATPG flows, and achieves capture-safety with no changes in the circuit-under-test or the clocking scheme.

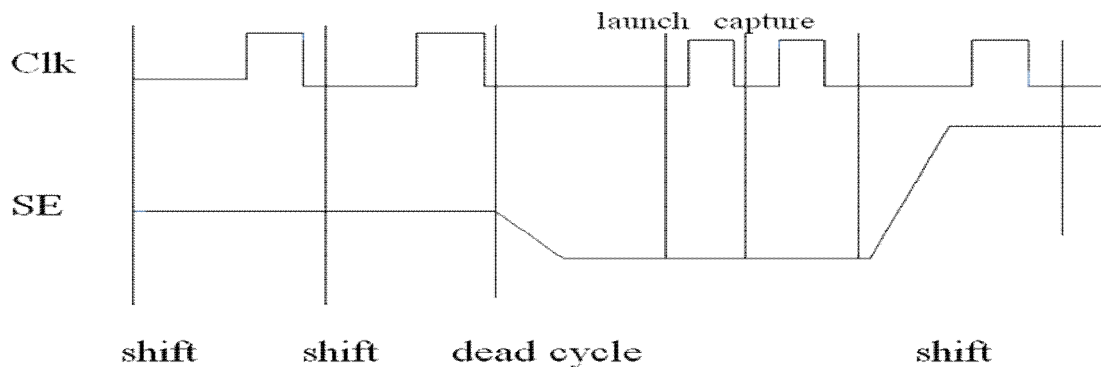
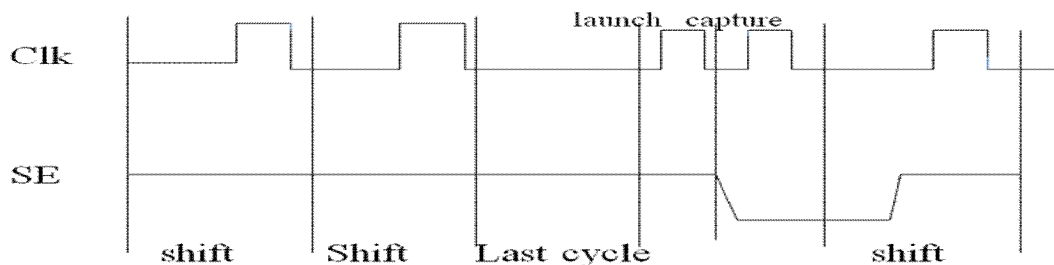


Fig: Timing Diagram of Launch-Off Capture

Scan testing has been the most widely adopted test strategy, which uses the full-scan methodology for circuit design, automatic test pattern generation (ATPG) for test data creation, and automatic test equipment (ATE) for test execution. Recently, at-speed scan testing has become mandatory in achieving high test quality for deep submicron (DSM) circuits by detecting timing-related defects. The concept of at-speed scan testing based on the launch-off-capture (LOC) clocking scheme. In shift mode (SE = 1), a test vector is applied by operating scan chains as shift registers over multiple shift clock pulses, with SL as the last shift clock pulse. In capture mode (SE = 0), two capture pulses are applied: C1 (launch capture) for launching a transition at the start-point of a path and C2 (response capture) for capturing the circuit response to the launched transition at the end-point of the path. Note that the test cycle is equal to the rated clock cycle in at-speed scan testing, which is very short for a high-speed design. Conventionally, high quality and low cost have been two basic requirements for scan test vectors. Test quality can be improved by increasing fault coverage, using realistic fault models, and testing for small-delay defects; while test cost can be reduced by test compression. Over the past decade, low test power, especially in the context of heat dissipation, has also become an important requirement. Recently, a new requirement, called capture-safety, has emerged and is rapidly becoming mandatory for at-speed scan test vectors. It is also referred to as supply-voltage noise-safety or power-safety. The launch capture (C1) may cause high launch switching activity (LSA). This may lead to excessive IR-drop, which significantly increases path delay so that timing errors occur at C2 only during at-speed scan testing. Such test-induced yield loss is rapidly worsening due to shrinking feature sizes, growing gate counts, increasing clock frequencies, and decreasing supply voltages. Capture-safety is required for at-speed scan test vectors to avoid test-induced yield loss. This paper proposed a novel and practical capture-safe test generation scheme, featuring a set of metrics for reliable capture-safety checking and a hybrid flow for effective capture-safety improvement. Its major advantage is that no circuit modification or clocking change is needed. Experiments have validated the metrics and demonstrated the effectiveness of the flow. Experiments on more industrial circuits are being conducted to fully quantify the correlation between capture-safety and the new metrics. This also helps in reducing over-pessimistic calls in metric-based capture-safety checking.

**LAUNCH-OFF-SHIFT:** The test pattern is to shift the next level using the Launch off Shift operation. As the LOS scheme launches transitions mainly followed by shift operation. The shadow registers can replace the

bidirectional stitching for the restoration of the load state in LOS testing. A special stitching and the associated DfT support are required only for the interface registers in order to enable a proper rewind operation. Main transition fault ATPG methodologies are Launch on Capture and Launch on Shift (also known as broadside-load and skewed-load respectively). They both launch transition at the input of combinational block in different way for the same fault detection.

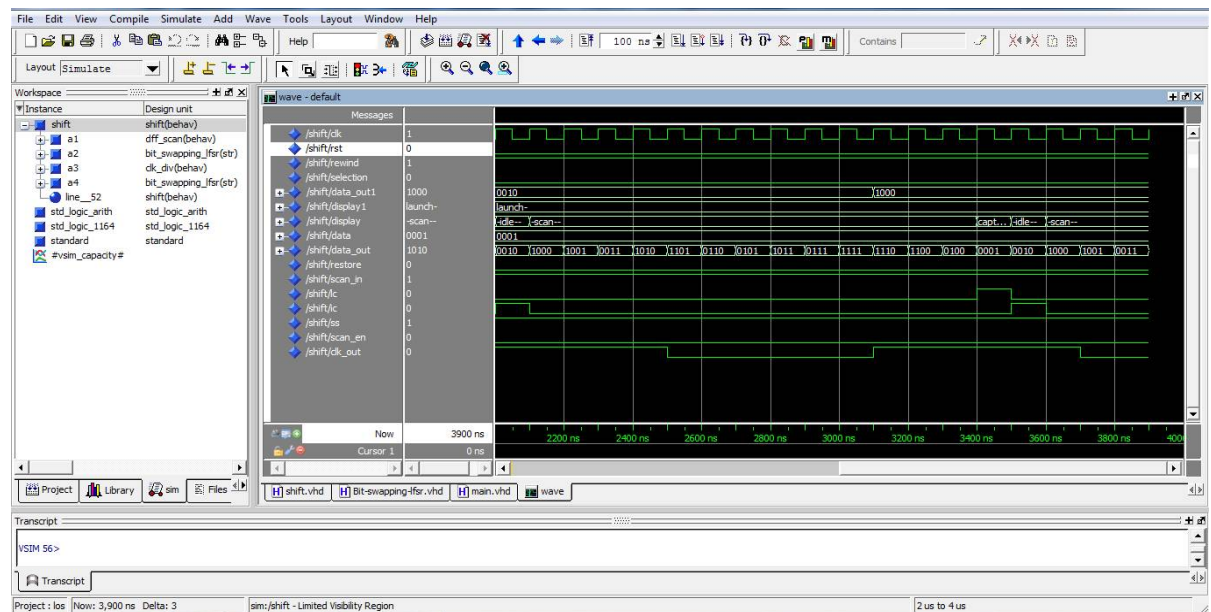
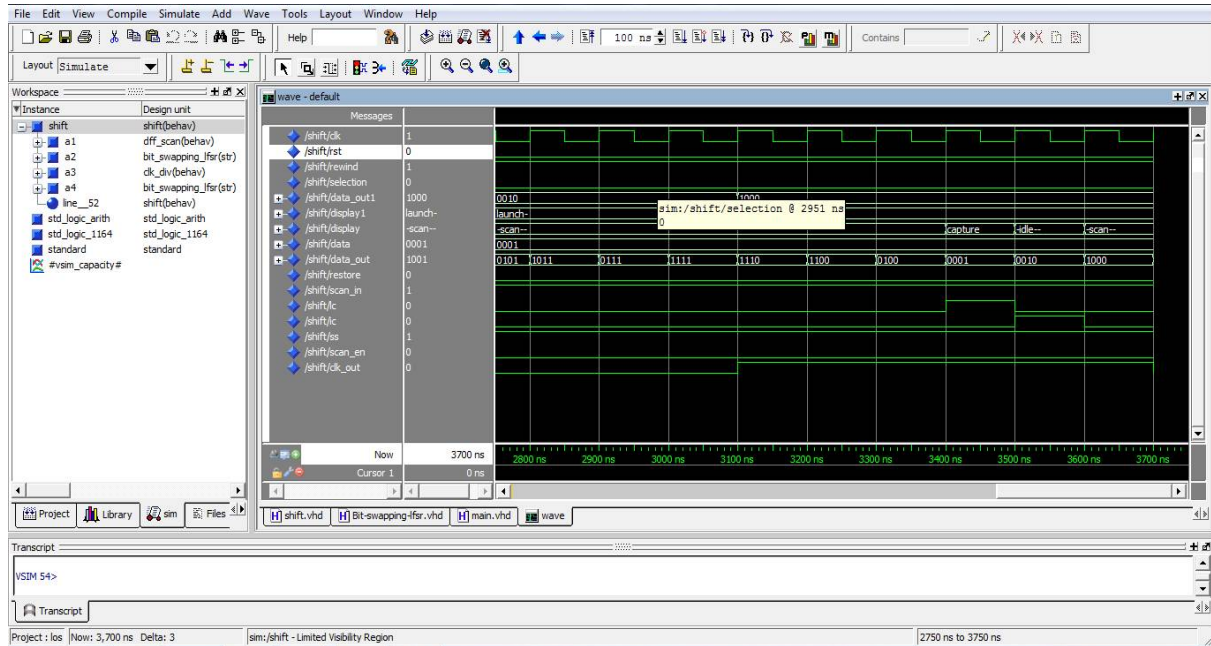


**Fig: Timing Diagram of Launch –Off-Shift**

Two vectors V1 and V2 are used to perform transition delay fault testing. Here describes the LOS waveform. As illustrated, last shift of scan chain initialize the inputs of combinational block and first functional clock is used to launch transition in the combination block. Then scan enable signal would assert. Example, for scan chain having N scan-length, in LOS, first vector of N bit is loaded in to scan chain by N slow clock. Then two fast clocks (functional clock) are used to launch and capture transition into and from the combinational block. Again scan chain unloads with N slow clocks. Here scan enable signal transit from high to low after last shift of loading process. So, launch clock always occur in function mode and launching of transition would be along function path. Launch- off-shift (LOS) and Launch-Off-Capture (LOC). In LOS, the transition is launched during the last shift cycle from the scan path (non-functional). The scan enable (SEN) is high during the last shift and must go low to enable response capture during the capture cycle. The time period for SEN to make this transition corresponds to the functional frequency. This is not applicable for very low cost ATE, which have a limitation of one at-speed signal port. In LOC method, the at- speed constraint on the SEN signal is relaxed and the transition is launched from the functional path. The controllability of launching a transition at the target gate is less as it depends on the functional response of the circuit under test to the initialization vector. In the first method, referred to as launch-off-shift (LOS), the transition at the gate output is launched in the last shift cycle during the shift operation. The paths of transition launch in LOS method for a multiplexed-DFF design; similar approach can be applied to an LSSD. The transition is launched from the scan-in pin (SD) of any flip-flop in the scan chain.

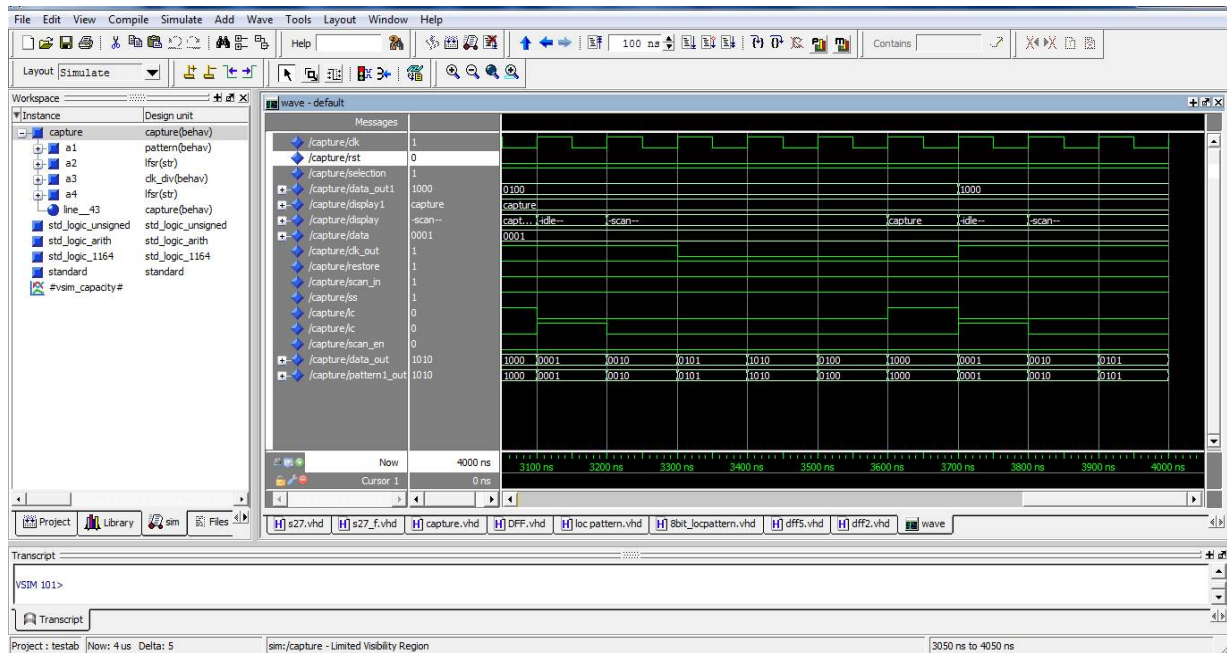
III. EXPERIMENTAL RESULTS

LAUNCH-OFF SHIFT:





LAUNCH-OFF CAPTURE:



IV. CONCLUSION AND FUTURE WORK

DfT support used reduces a set of patterns optimized for cost and quantity. T-algorithm process mainly used to reduce the clock function due to the LOC and LOS process and to optimize the circuit power consumption. The proposed scheme reduces the delay time (1.167NS) and power (9mW). The future enhancement is to achieve the fault coverage of the LOC approach, by replacing regular scan cells with enhanced scan cells; simultaneously the volume of test data can be reduced.

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