

Performance Evaluation and Stability Analysis of SRAM Cells

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ABSTRACT: Cell stability and area are among the major concerns in SRAM cell designs. This paper compares the performance of various SRAM cell topologies, which include the conventional 6T-cell, 7T-cell, 8T-cell, 9T-cell and the 10T-cell implementations. Even though 9T and 10T cell implementation result in a reported 13% and 30% area increase, respectively, these two topologies allow for better cell stability due to their read-disturb-free operation, which is beneficial as process technologies continue to scale down.

KEYWORDS: static random access memory (SRAM), Low power (LP), Dynamic random access memory (DRAM), Central processing unit (CPU)

I. INTRODUCTION

SRAM cell is a basic storing unit of volatile semiconductor memory that stores binary logic '1' or '0' bit. It uses bi-stable latching circuitry made of Transistors/MOSFETS to store each bit and it works without refreshing. SRAM cell is much faster to provide a direct interface with the CPU at speeds that are not attainable by other cells. SRAM cell is much reliable and more power efficient as compared with other storing cells (like DRAM cell). Due to these advantages, SRAM cell can be used as a basic storing element of various memories that are used in personal computers, workstations, routers and peripheral equipment, internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. The growing demand of portable battery operated systems has made energy efficient processors a necessity. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. We know that, on-chip memories determine the power dissipation of SoC chips. Hence it is very important to have low power and energy efficient and stable SRAM which is mainly used for on chip memories. The main objective of this work is evaluating performance in terms of power consumption, delay of various SRAM cells in 130nm technology and comparing them with basic 6T SRAM cell. Literature review and study of various SRAM cells is done. Transient analysis of all the SRAM cells is done and output is shown. The power and delay of all the SRAM cells are measured.

II. EXISTING SRAM CELLS

2.1 CONVENTIONAL 6T SRAM CELL

The memory cell is the basic building block of any static memory system. Fig 2.1 shows a conventional 6-transistor static memory cell in CMOS technology [7]. The circuit is a flip-flop comprising two cross-coupled inverters and two access transistors, M5 and M6. The access transistors are turned on when the word line is selected and connect the memory cell to the column bit lines (BL or BL'). They act as transmission gates allowing bi-directional current flow between the flip-flops and the two bit lines. Both the bit lines carry complementary data and connect all the memory cells in a single column. For performing a read or write operation on the memory cell, the word line should be high to connect the memory cell and the bit lines. The fact that each memory cell has two bit lines is used to distinguish between a memory read or write operation. The following two subsections discuss the read and write operations of a memory cell in brief.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 4, March 2016

2.1.1 READ OPERATION

Before the read operation begins, the bit lines, BL and BL' are precharged to a high value, usually V_{DD}. When the word line is selected, the access transistors are turned on. This will cause a current to flow from V_{DD} through the PMOS pull-up transistor of the node storing 1 and the access transistor onto the bit line B, charging the capacitance of line BL, C_{BL}. On the other side, current will flow from the precharged BL bar line through M5 and M1 to ground, thus discharging C_{BL}. From the above description we note that the voltage across C_{BL} will rise and that across C_{BL'} will fall. Thus, a differential voltage V_{BB} develops between the bit lines BL and BL'. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

2.1.2 WRITE OPERATION

For a write operation, one of the bitlines is lowered to 0 V and the other one is raised to V_{DD}, and of course the cell should be selected by raising the word line. Depending on the value we are writing into the cell one of the bitlines is pulled low and the other is pulled high.

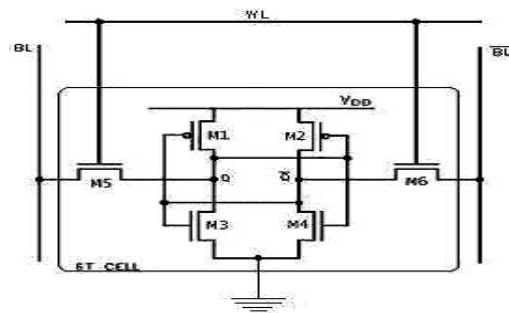


Figure 2.1 Conventional 6-T Static RAM Cell

The 0 on one of the bitlines will overpower the PMOS pull-up and the flip-flop would change its state. However, during a read operation a 1 on the bitline should not overpower the NMOS pull down. If this happens read operation would destroy the state of the memory cell and operation is no longer valid. These requirements would dictate the W/L ratios of all the transistors in the memory cell. Typically, the inverters are designed so that the pull-up and pull down transistors are pitch matched. The access transistors are however made two to three times wider than the other transistors.

2.2 7T SRAM CELL

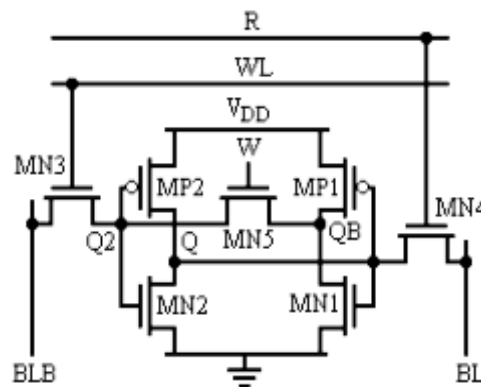


Figure 2.2 7-T Static RAM Cell

7T SRAM reduced the activity factor α_{BL} for reduction of dynamic power while writing to a cell given by $P_{WRITE} = \alpha_{BL} \times C_{BL} \times V^2 \times F_{WRITE}$. But static power consumption in a SRAM cell is more critical than dynamic power consumption (during read and write operation due to bitline charging and discharging), since whole part of the cache remains idle most of the time except the row being read from or written to. Moreover, the 7T SRAM cell needs dual-Vt transistors requiring advanced technology and additional masking cost. In addition to that, its transistor sizing constraint for meeting its functionality poses additional area penalty. Read/Write operation: Both BL and BLB are precharged high before and after each read/write operation. The write operation in 7T cell starts by turning off MN5. Complement of data to be written to node Q is applied to BLB and MN3 is turned on by asserting WL high, leaving MN4 off. BL and MN4 do not take part in write operation. During standby mode MN3 and MN4 are kept off applying WL and R low, MN5 is kept on asserting W high. Read operation of 7T cell is similar to that of 6T cell. BLB discharges through the critical read path consisting of MN3, MN5 and MN1 during read operation with QB storing "0". BL discharges through the read path MN4 and MN2 during read operation with QB storing "1".

2.3 8T- SRAM DESIGN

This cell shows poor stability at very small feature sizes, the hold and read static noise margins are small for robust operation. This cell employs two more transistors to access the read bit line. The transistor configuration (i.e. M1 through M6) is identical to a conventional 6T SRAM cell. Two additional transistors M7 and M8 (thus yielding an 8T cell design) are employed to reduce the leakage current. To overcome the problem of data storage destruction during the read operation, an 8T-cell implementation for which separate read/write bit and word signal lines are used as shown in Figure 2.3, to separate the data retention element and the data output element. In turn, the cell implementation provides a read-disturb-free operation.

Write access to the cell occurs through the write access transistors and from the write bit lines, BL and BLB. Read access to the cell is through the read access transistor and controlled by the read word line, RWL. The read bit line, RBL, is precharged prior to the read access. The word line for read is also distinct from the write word line. However, for the 8T structure, the read bit line leakage is greater, especially in deep submicron/Nano ranges. When the column for Read (RBL) is not accessed, the leakage current through M7 may cause a severe voltage drop at the read bit line, leading to large Power dissipation, thus error may appear at the output.

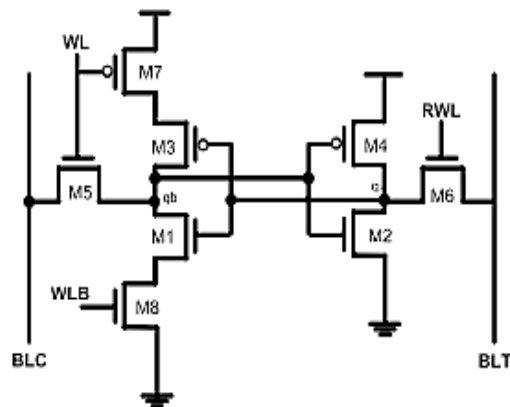


Figure 2.3 8T – SRAM cell

The circuit diagram (Fig 2.3) shows our proposed SRAM cell. In this cell, M5 is write access transistor and M6 is for read access. Having individual access transistors in our cell, it is possible to increase size of write access transistor to improve write-ability and choose minimum size for read access transistor to enhance read stability, whereas in 6T there is a conflict while sizing the access transistors. In the proposed SRAM cell, the added PMOS and NMOS transistors (M7, M8) become OFF during write operation.

This interrupts VDD and GND connections of the left inverter in the cell. Thus left inverter becomes weaker during write operation, and a relatively stronger write access transistor can easily write the input to our cell. In 8T,

before read operation bit-line of read (BLT) is precharged to VDD, and then by asserting RWL signal, M6 become ON and according to the stored data at node q, the capacitance of BLT bit-line is discharged or remains unchanged.

III. PROPOSED METHOD

3.1 6T MODIFIED SRAM CELL

Fig. 3.1 is depicting the circuit diagram of modified 6T SRAM Cell. The transistors NMOS_3, PMOS_4 and NMOS_2, PMOS_1 form cross coupled inverters. Reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation that “a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path.”

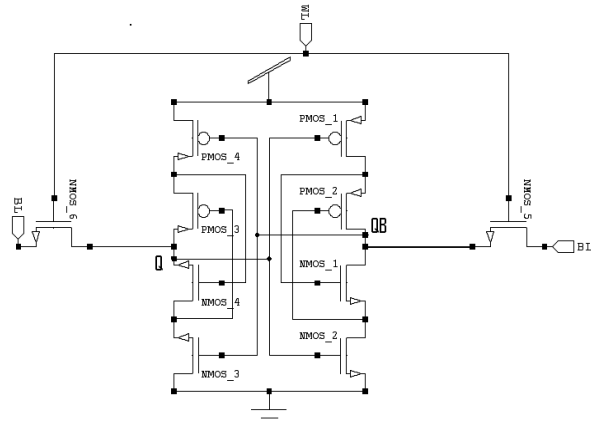


Figure 3.1 6T – MOD SRAM cell

3.2 9T SRAM CELL

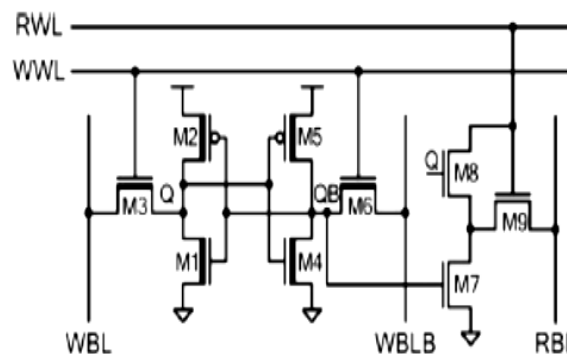


Figure 3.2 9T – SRAM cell

Fig. 3.2 depicts the proposed 9T SRAM cell and its layout. The cell consists of a 6T SRAM part (the write-access transistors with a cross-coupled latch) and a dedicated read port. The read port comprises three NMOS transistors (M7, M8, and M9) for realizing equalized bitline leakage and improving bitline sensing margin in a single-ended read bitline (RBL). The write access paths and the data storage latch are implemented with HVT devices for leakage reduction while the read port employs LVT devices for performance. A write operation is enabled by activating a write word line (WWL) and completed when the data loaded at WBL and WBLB is written into Q and QB. A read operation starts by enabling a read word line (RWL) and is followed by conditional RBL discharging. If Q holds logic 0, M7 is turned on and discharges RBL to GND. If, on the contrary, Q stores logic 1, M8 is activated and provides pull-up current from RWL (=V) to RBL, slowing down the discharging speed of RBL.

3.3 10T SRAM CELL

The schematic of the 10T sub threshold bit cell.[6] Transistors are identical to a 6T bit cell except that the source of M1 and M2 tie to a virtual supply voltage rail V_{dd}. Write access to the bitcell occurs through the write access transistors, M5 and M6, Transistors from the write bitlines, WBLT and WBLC. Transistors M8 through M10 implement a buffer used for reading. Read access is single-ended and occurs on a separate bitline, RBL, which is precharged to prior to read access. The wordline for read also is distinct from the write wordline. One key Advantage to separating the read and write wordlines and bit lines is that a memory using this bit cell can have distinct read and write ports.

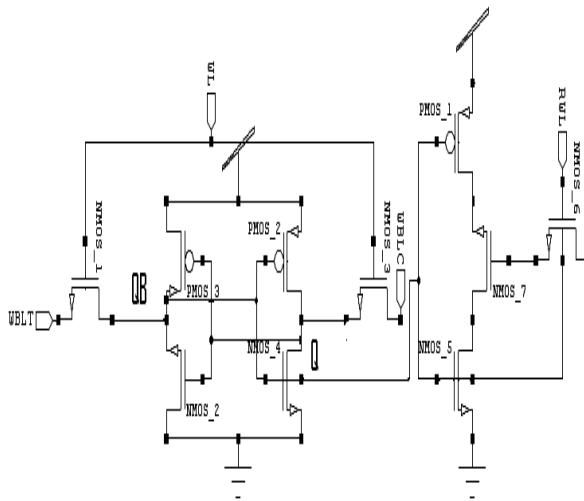


Figure 3.3 10T – SRAM cell

IV. RESULTS

The existing design is simulated using TANNER tools using 130nm CMOS technology.

4.1 OUTPUT OF 6T-SRAM CELL

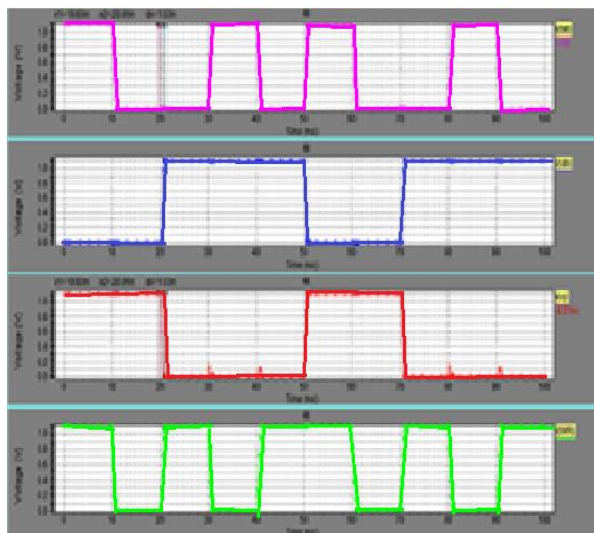


Figure 4.1 Output of 6T-SRAM

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

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4.2 OUTPUT OF 7T-SRAM CELL

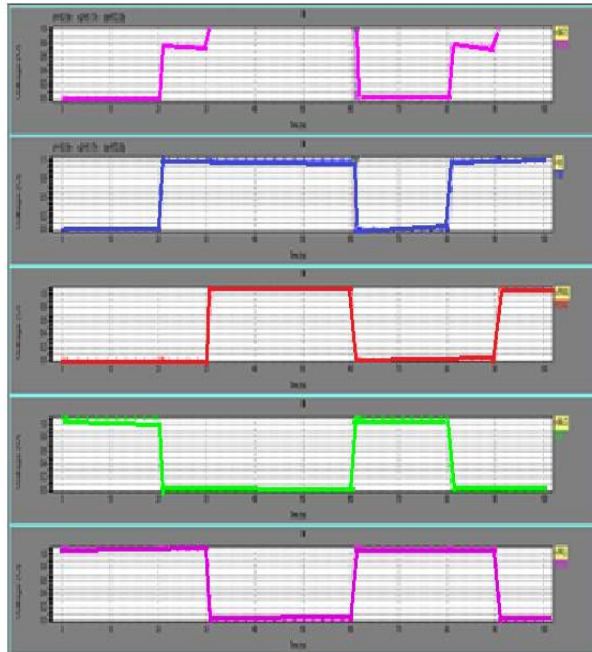


Figure 4.2 Output of 7T-SRAM

4.3 OUTPUT OF 8T-SRAM CELL

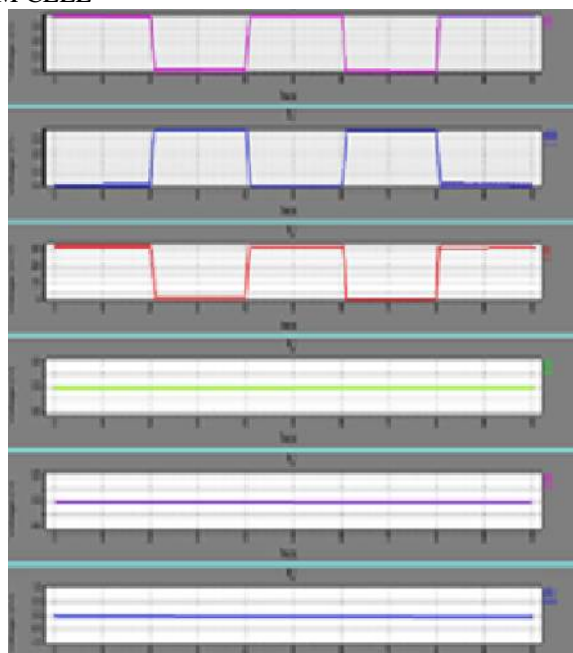


Figure 4.3 Output of 8T-SRAM

4.4 OUTPUT OF 6T-MOD SRAM CELL

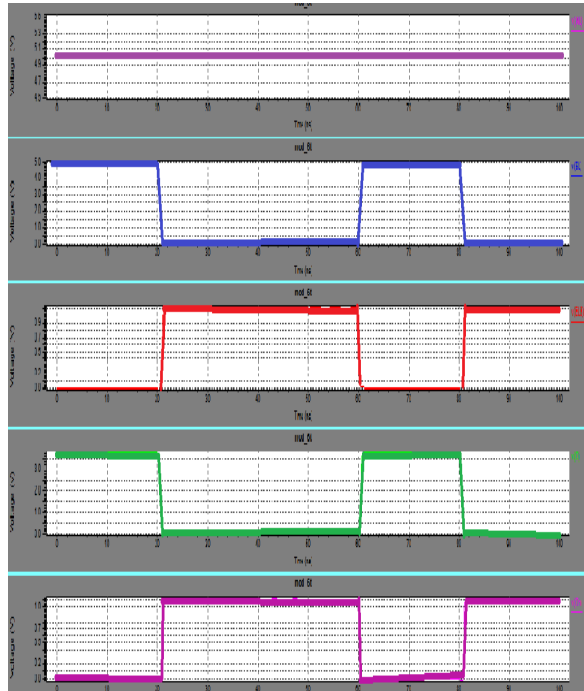


Figure 4.4 Output of 6T- MOD SRAM

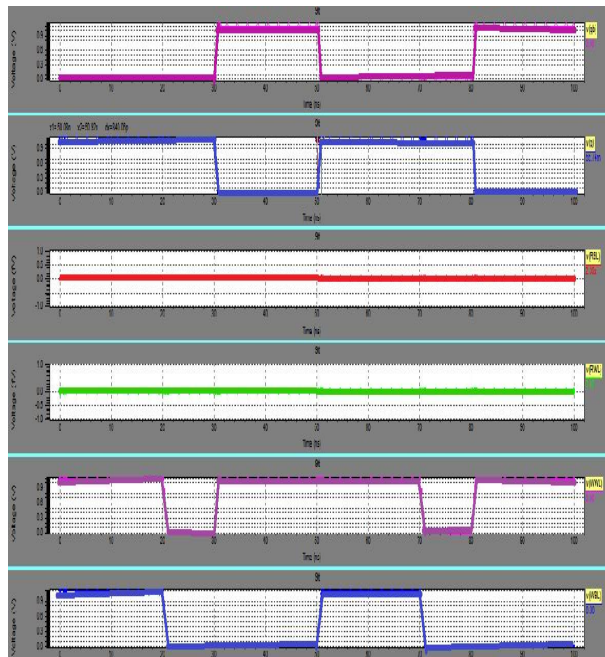


Figure 4.5 Output of 9T-SRAM

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4.6 OUTPUT OF 10T-SRAM CELL

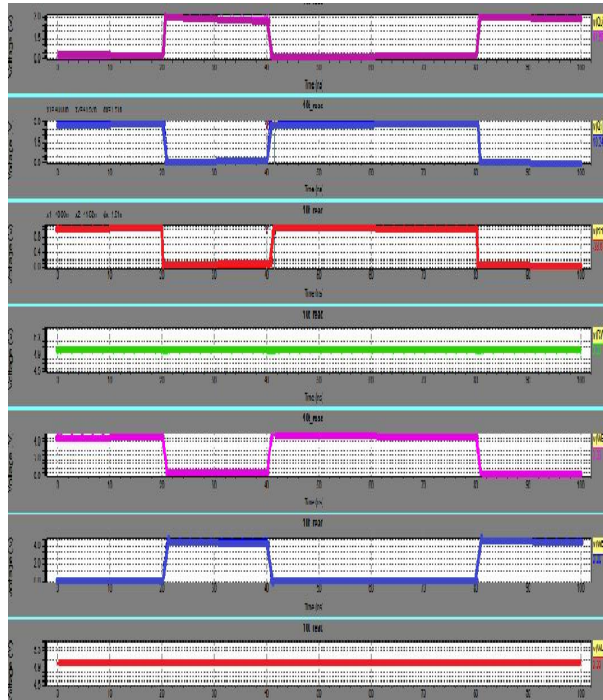


Figure 4.6 Output of 10T-SRAM

4.7 POWER AND DELAY COMPARISON OF SRAM CELLS

Table 4.7 power and delay comparison of SRAM CELL

PARAMETER	CONVENTIONAL 6T CELL	7T-SRAM CELL	8T-SRAM CELL	6T-SRAM MOD CELL	9T-SRAM CELL	10T-SRAM CELL
Average Power (Watts)	1.09×10^{-6}	1.635×10^{-7}	6.52×10^{-8}	6.20×10^{-5}	6.076×10^{-7}	3.90×10^{-7}
Read delay	1.145ns	1.1ns	0.757ns	0.925ns	1.26ns	1.091ns
Write delay	0.97ns	1.035ns	0.672ns	1.006ns	0.756ns	0.654ns

Table 4.7 tests the values of average power & delay of read and write operation of 6T,7T,8T,9T and 10T SRAM cell variation.

V. CONCLUSION

The stability performances of various SRAM cell topologies have been presented. As process technologies continue to advance, the speed of SRAMs will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cells. Due to stability concerns, the dual port designs that implement read-disturb-free feature such as that seen in the 9T and 10T cell implementation might become more practical in the future SRAM cell implementation.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Special Issue 4, March 2016

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