

A Study of Interleaved Buck Converter PFC with Slope Compensation

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ABSTRACT: One of the major challenges of AC/DC converters that require power factor correction is to maintain the efficiency across the line. This paper deals with the study of an interleaved buck power factor corrector topology. Interleaved topology consists of two buck converters working in parallel. The study is based on the parameters such as converter efficiency, power factor correction, etc. Slope compensation method is used to improve the power factor (PF) of the input. It is used to maintain the stability of the current loop and ensure that no subharmonic oscillation is produced when the duty is greater than 50%. Simulation results obtained are also provided. PF values are greater than 0.94.

KEYWORDS: Clamp current mode control, Single phase buck converter, Inter leaved buck converter, Power factor corrector (PFC), Slope compensation

I. INTRODUCTION

Since many of the electric equipment are working with DC input, the AC-DC power conversion has a vital role in the electrical industry. During the conversion due to the phase shift or distortions, there are chances to affect the performance of the converter and the power quality. To solve these issues power factor corrector is needed. By introducing power factor corrector to the input source, the input current will be sinusoidal and it will be in phase with the source voltage [1]-[2]. The energy conversion efficiency should be greater than 80% at a light load to full load to save energy.

Conventionally boost converter type topologies are used for power factor correctors. The conversion efficiency decreases by 1%-2% at low line input. And for high input voltages the switching loss, core loss and electromagnetic interference (EMI) rises. But in buck converters can conquer the formerly stated defects of the boost converter because of the low output voltages for buck PFCs [3]-[5]. Furthermore, the common-mode noise is very low for buck PFC.

Clamping current model which is derived from the peak current mode control is adopted in interleaved PFC for the power factor correction. In clamping current mode control, the operation requires constant frequency and limited maximum duty cycle. Compared with different common controls, clamping current mode control is easy and affordable. There are some advantages like lower differential-mode noise, cancelled ripple current, and decreased current harmonics because the control is interleaved between the switches of two phases.

The paper is organised as follows. Section I gives a brief introduction of the topic. In Section II, the topology of conventional and interleaved buck PFC is discussed. Clamped current mode control is explained in Section III. Simulation results are included in the Section IV. Concluding remarks of this paper are presented in Section V.

II. TOPOLOGY

Single Phase Buck PFC

The figure 1 shows a buck PFC is the studied topology in [6]. It can be operated in both continuous and discontinuous modes of operation which is described first in [4]. The buck PFC will not shape the line current during the time intervals when the input voltage is lower than the output voltage. The resulting conduction angle is a function of both the

incoming line and output voltages. In the reference design mentioned above, the output voltage is set to 80 VDC. This is low enough to allow conduction angles sufficient to achieve a PF (Power Factor) of at least 0.9 over an input voltage range from 90 VAC to 264 VAC. Clamped current control method is used for controlling the circuit.

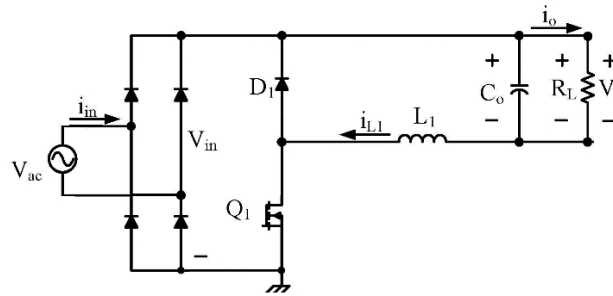


Fig 1.Single phase Buck PFC

Interleaved Buck PFC

Interleaved Buck PFC is composed of two parallel buck converters. Q₁ and Q₂ are the two power switches, D₁ and D₂ the freewheeling diodes and L₁, L₂ are the inductors. A single capacitor C_o is used for both the converters. In this the switching pulses given to the two switches are 180° phase shifted. Compared to the single phase buck PFC this circuit can handle higher power conversion and diminish the ripple currents of input and output. The speed of the transient response and power density can be raised at the same rated power inductances and capacitances can be reduced. It can be operated in both the cases duty cycle D>0.5 and D<0.5.

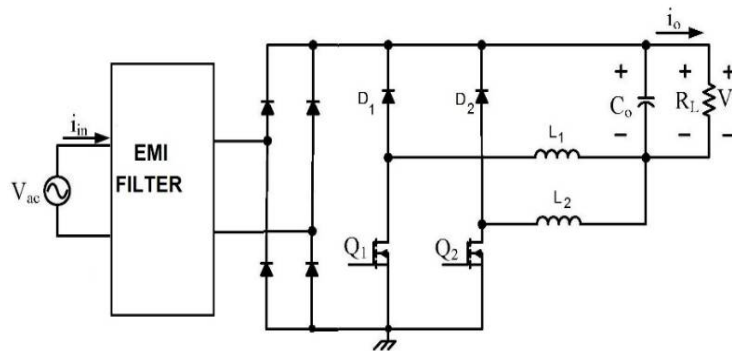


Fig 2.Interleaved Buck PFC

The PFC inductor is designed for an inductance value that ensures DCM operation at high input voltage. With an appropriate value of inductance, operation at low line should then result in CCM operation over most of the conduction angle at full load. The inductance required is given by:

$$L_{PFC} = \frac{1}{2f_{sw}} \frac{(V_{in(pk)} - V_{bulk})}{V_{in(pk)}} \left(\frac{V_{out}}{V_{in(pk)}} \right)^2 \tag{1}$$

Where the instantaneous line voltage equals the bulk voltage, f_{sw} the switching frequency V_{in(pk)} peak line voltage. The value of bulk capacitance required is dictated by requirements on the allowable ripple voltage and hold uptime.

III. CLAMPED CURRENT MODE CONTROL

Clamping current mode control is similar to that of peak current mode control. Inductor current is taken from the circuit and compared with reference signal during each switching period. But the maximum duty cycle (D) of clamping current mode control is limited in this method. Therefore, clamping current mode control is normally applied to the small power application. This is low cost, simple, high efficient method with high power factor. Figure 3 shows the diagram of clamping current mode control applied to single-phase Buck PFC. It can be seen that feedback error signal V_e is sent to the PWM generator to be compared with the combined signal of sensed current and ramp current.

In figure 3 (a) shows the current clamp control of single phase Buck PFC and (b) shows the control of interleaved Buck PFC.

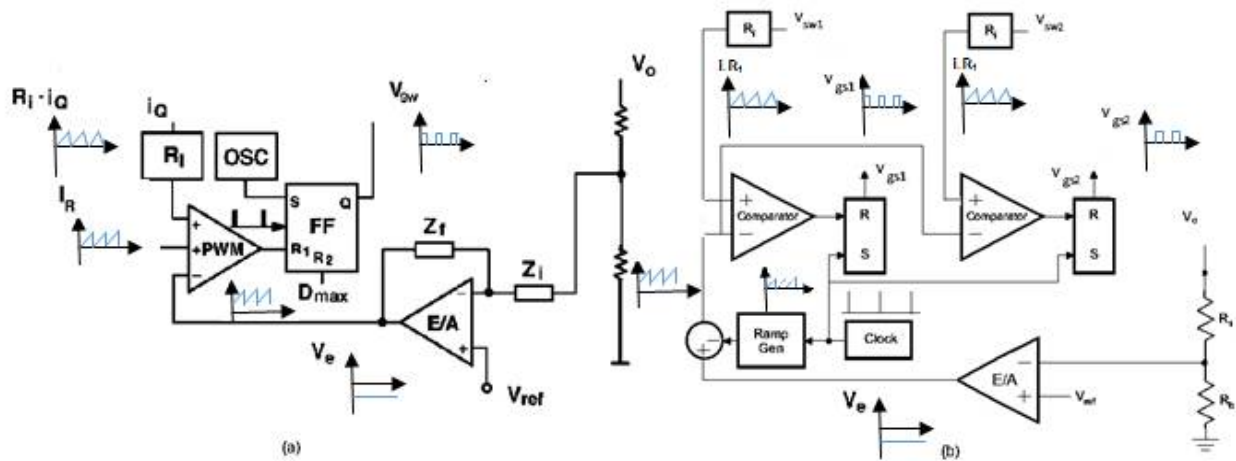


Fig 3. Clamped current model

Slope Compensation

Current controlled switch mode power supplies (SMPS) allow pulse by pulse current control and monitoring. This makes them more reliable and more robust than voltage controlled supplies. A Pulse Width Modulation (PWM) signal can control the output current through feedback from both the switching circuit and the load circuitry. One issue with current controlled SMPS is that at duty cycles of 50% or greater, the circuit can become unstable, oscillating at half of the switching frequency due to sudden variations in the load current. This is where Slope Compensation is used to filter out, or dampen, the feedback signal variability and restore stable operation. The slope compensation acts as a buffer to supply or reduce voltage to the sensing circuitry to reduce the variability and stabilize the PWM signal while maintaining a constant current supply.

Slope compensation is implemented by adding a saw-tooth ramp of the same frequency as of the control circuit to the sensed inductor current ramp so that the system can still be stable at duty cycle above 0.5.

Slope compensation ramp

From the above discussion it is concluded that to ensure the stability of the current loop, the slope of the external ramp S_e , should be at least 50% of the maximum down slope of the inductor current $S_{f,max}$

$$s_e > k_s s_{f,max} \quad k_s \geq 0.5 \tag{2}$$

k_s is the normalized slope of the external ramp. From figure 4, the slope compensation of the ramp is given by

$$s_e = \frac{I_R}{D_{max} T_s} = \frac{I_{RM}}{T_s} \tag{3}$$

The down slope of the inductor current is constant. i.e.

$$s_{f,max} = s_f = \frac{V_o}{L} \tag{4}$$

And now the amplitude of the compensation ramp can be obtained as

$$I_{RM} = \frac{k_s V_o}{L f_{sw}} \tag{5}$$

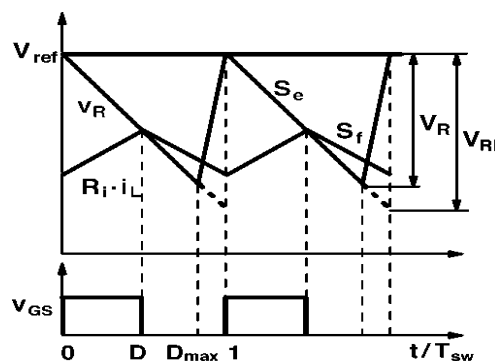


Fig 4. Slope compensation method

IV. SIMULATION RESULTS

The circuit was designed for interleaved buck converter and it can be operated as single phase buck PFC and interleaved buck PFC. The circuit diagram of a 300 W, 80V output, 85-264V input was simulated by using MATLAB SIMULINK software and obtained the results.

Table 1. Key design parameters

Design Parameters	Attributes
Line frequency	60Hz
Switching frequency	65kHz
Inductor	90μH
Output capacitor	1800μF
Input Voltage	85 V_{rms} -264 V_{rms}
Output Voltage	80V

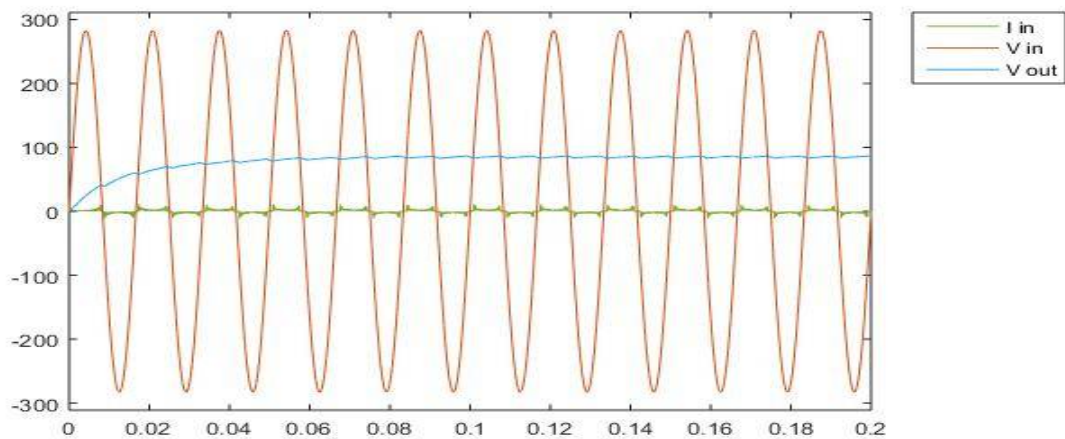


Fig 5. Input-Output voltage and current waveforms

Figure 5 shows the input current (I_{in}), input voltage (V_{in}), and output voltage (V_{out}) waveforms of interleaved buck PFC. The measured waveforms are in good agreement with the corresponding calculated waveforms. The PF value is considerably very small at a low input voltage between 85 and 115 V_{ac} inputs. It is due to the fact that the input current conduction angle is very small when the input voltage is low. Figure 6 shows the inductor currents of i_{L1} and i_{L2} .

Here a constant normalized slope of 0.6 is given to the circuit. Therefore, the input current does not form the shape of a sine wave. As it increasing, the input current follows the input voltage to achieve the function of the PFC. The PF values are almost greater than 0.94 in all the input voltage range by adjusting the slope compensation (k_s). And the circuit shows high efficiency. By applying an adaptive slope compensation the circuit can improve the shape of the input current.

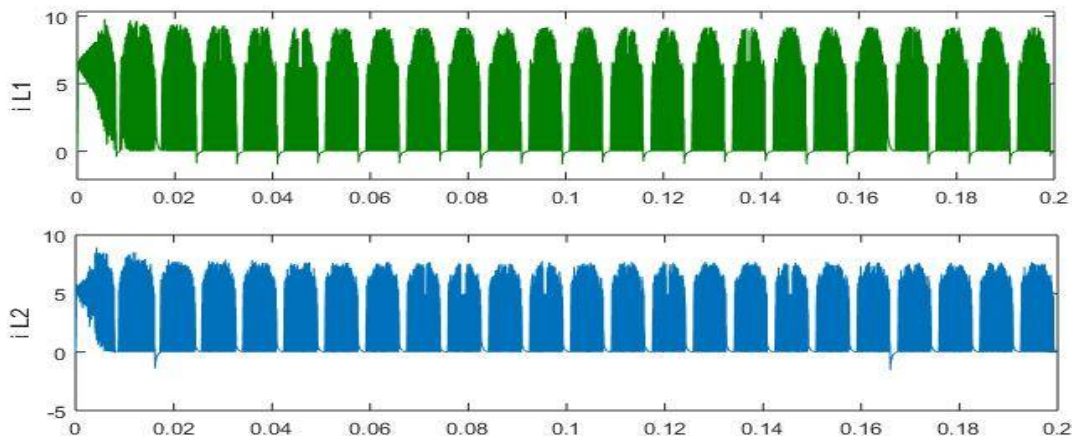


Fig 6. Inductor current waveform

It is shown in Table 2 that, with increasing k_s , the power factor(PF) increases and the Total Harmonic Distortion(THD) decreases. A single value of k_s cannot ensure the correction of PF in the whole input voltage range. The value of k_s should be varied with the input voltage. By this, the PF can be improved.

Table 2: CDF, DF, PF and THD Versus k_s at $V_{in}=200V_{rms}$

k_s	Current Distortion Factor(CDF)	Displacement Factor(DF)	Power Factor(PF)	Total Harmonic Distortion(THD)(%)
0.6	1.084	0.78199	0.847	85.85
1	1.0881	0.78199	0.85	85.10
1.5	1.1106	0.78199	0.868	79.89
2	1.1187	0.78199	0.8748	78.84
3	1.1657	0.78199	0.9115	67.38
5	1.2042	0.78199	0.9417	59.99
10	1.2110	0.78199	0.94706	57.72

V.CONCLUSION

An analysis of the interleaved buck power factor converter has been presented. The design is focused on the slope of the external current ramp. It was shown that, with a constant slope of the external current ramp in the whole input voltage range, an optimum design cannot be achieved. The slope of the external ramp should be variable and increase with increasing input voltage. Simulation results obtained on a 300W, 80V output CCB PFC converter, were provided. It was shown that the buck PFC maintains a high efficiency across the entire input voltage range.

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