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Design and Implementation of High Speed 256-Bit Modified Square Root Carry Select Adder

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ABSTRACT: Adders are the most widely used digital component. Carry Select Adder (CSLA) is one of the fast adders which is used for the fast arithmetic operations. The carry-select adder is simple but rather fast, having a gate level depth of $O(\sqrt{n})$. The area and the power consumption of the Ripple carry adders of CSLA are more. By modifying structure of CSLA in gate level, the power and the area of the adder is reduced. The square root CSLA is modified with BEC for reduction of area and power consumption. The modified square root CSLA is designed for 8-bit, 16-bit, 32-bit, 64 bit, 128-bit and 256-bit. The performance of modified square root CSLA improved than the regular CSLA. The proposed design is implemented in Xilinx ISE.

KEYWORDS: Binary to Excess-1 Converter (BEC), Ripple Carry Adder (RCA), Carry Select Adder (CSLA), Modified Square root CSLA (Modified SQRT CSLA).

I. INTRODUCTION

Digital adders are the heart of the processors. The carry propagation adder constitutes many full adders and other components and consumes large area and generates large delay and giving the low performance. But designing of a low area, high speed, less power consuming data path logic system are one of the most substantial areas of research in VLSI system design. Addition operation is the core of computer arithmetic. Arithmetic components are the necessary units of the microprocessor. In digital adders the speed is limited by the time delays. To overcome these problems the various adders are used. One of the adder used is the CSLA. It is classified into two types linear CSLA and non-linear CSLA. The speed of the CSLA is reduced due to the use of the Ripple Carry Adder (RCA) and the CSLA is not efficient due to the use of the more amount of the RCA occupying the large amount of the area. Here in the linear CSLA the huge amount of the RCA is replaced by the Binary to Excess Converters (BEC) reducing the little amount of time delay and the area of the CSLA and increasing the performance. CSLA is used to rectify the problems of carry propagation delay by generating multiple carries and then select a carry to generate the sum [5]. It uses multiple pairs of RCA to generate partial sum and carry by considering carrying 0 and carry in 1, then the final sum and carry are selected by the multiplexers (Mux). Now a day's mobile electronics require the reduce area and decreased use of the components for the portability and the battery life. The Carry Select Adder is used in the many system to overcome the problem of the carry propagation delay by generating multiple carries.

II. COMPONENT LEVEL EXPLANATION

1. BINARY TO EXCESS-1 CONVERTER:

The main aim of this work is to implement the use of the BEC instead of the RCA in order to reduce the area consumption and power consumption than the regular CSLA. To replace a N-bit RCA, N-1 bits of BEC are required which is more efficient than the regular RCA. Since the RCA has the more delay time the BEC are used in the design. The structure of the 4-bit BEC is shown in the figure 1.

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Functional Symbols:

- & - AND
- ~ - NOT
- ^ - E-XOR

2. EVALUATION OF DEALY AND AREA OF THE BASIC ADDER:

The E-XOR gate is implemented using the basic gates such as AND, OR and the Inverter (NOT) shown in the figure 2. This implementation is also known as AOI implementation. The gates that present between the dotted lines perform the parallel operations. The area evaluation is done by counting the total number of AND, OR and Inverter (NOT) gates required for each logic block having the delay and the area equal to 1 unit.

3. COMPARISION BETWEEN RCA AND BEC:

4-bit RCA:

RCA is made up of the full adders connected in a cascade in which the output from the one full adder is the input to another adder. Therefore the gates require for the building of 4-bit RCA is given by TABLE 1,

4-bit BEC:

The 4-bit BEC can be obtained by the Boolean equations from the Fig 1. Therefore the gates required for the building of a 4-bit BEC is given by,

TABLE 1:
AND, OR AND INV GATES IN 4-bit RCA

AND	28
OR	16
INV	16

TABLE 2:
AND, OR AND INV GATES IN 4-bit RCA

AND	09
OR	03
INV	07

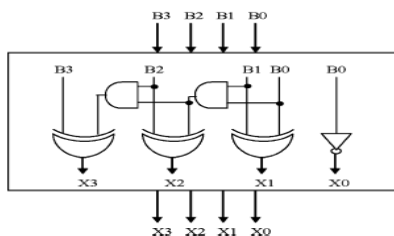


Figure 1. Binary to Excess-1converter

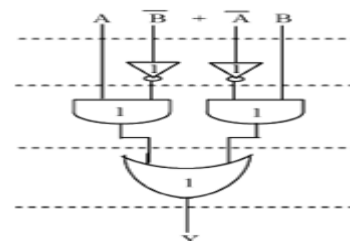


Figure 2. Design of E-XOR using AOI

The Boolean equations of the BEC are given by

- $X0 = \sim B0$
- $X1 = B0 \wedge B1$
- $X2 = B2 \wedge (B0 \& B1)$
- $X3 = B3 \wedge (B0 \& B1 \& B2)$

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4. ARCHITECTURE OF REGULAR CSLA AND MODIFIED SQRT CSLA:

Regular 16-bit Sqrt CSLA:

The carry select adder generally consists of two Ripple Carry Adders one with the input $c_{in}=1$ and other with the input $c_{in}=0$. From the Figure 3, the CSLA uses the multiple ripple carry adders with the inputs $c_{in}=1$ and $c_{in}=0$. We have used both the half adder and full adder for the input $c_{in}=0$ and only the full adder for the input $c_{in}=1$. The Regular 16-bit Sqrt CSLA includes many ripple carry adders of various sizes consuming the large amount of the space in the design. Figure 3 shows the structure of the Regular 16-bit Sqrt CSLA. In Regular CSLA there is only one RCA is present to perform the least significant addition RCA[1:0], the other RCA perform calculation twice one time with the assumption of the carry being zero $c_{in}=0$ and carry being one $c_{in}=1$. Then the final sum and carry are fed into the Multiplexer (MUX).

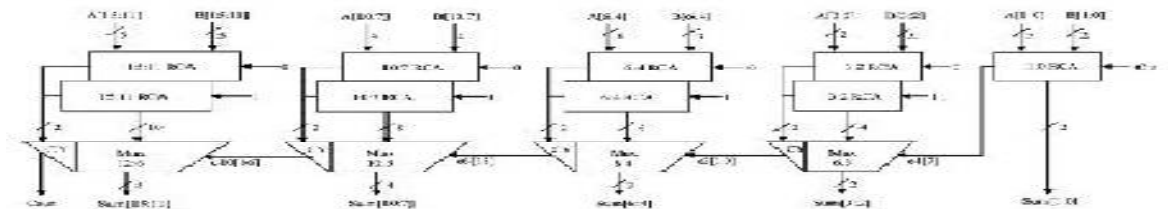


Figure 3. 16-bit Regular Sqrt CSLA

Modified 16-bit Sqrt CSLA:

The architecture of modified 16-bit Sqrt CSLA is as similar to the Regular 16-bit Sqrt CSLA. The only change made is the Ripple Carry Adder (RCA) is replaced by Binary to Excess-1 Converter (BEC) in order to achieve the low power consumption and the less area. In the modified Sqrt CSLA the number of gates used is less when compared to the regular Sqrt CSLA. Thus BEC replaces the RCA with $c_{in}=1$ instead of using dual RCAs to reduce area and power consumption of the conventional CSA. To replace the N-bit RCA, an N+1 bit BEC is required.

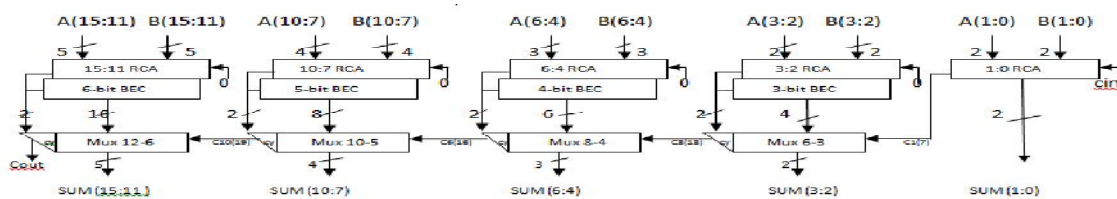


Figure 4. modified 16-bit Sqrt CSLA

Modified 32-bit Sqrt CSLA:

The modified 32-bit Sqrt CSLA is as same as the regular CSLA the only change made is the RCA is replaced by the BEC with the carry input $c_{in}=1$ in order to reduce the power and the area of the CSLA.

Modified 64-bit and 128-bit Sqrt CSLA:

The modified 64-bit Sqrt CSLA is constructed using two 32-bit modified Sqrt CSLA. The 128-bit Sqrt CSLA is constructed using the two 64-bit Sqrt CSLA with the carry input $c_{in}=1$ and the power is reduced very much and the area consumed is also very less

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Modified 256-bit SQR T CSLA:

The 256-bit SQR T CSLA is constructed using the two 128-bit SQR T CSLA with the carry input cin=1 and the cout of first 128bit module is given as input to the second 128 bit module. The power is reduced very much and the area consumed is also very less.

6. DELAY AND AREA ANALYSIS OF 128-bit SQR T CSLA:

The area of the modified SQR T CSLA is very less when compared to the regular SQR T CSLA. From the simulation results the area of the modified 128-bit SQR T CSLA is greatly reduced when compared to the area occupied by the regular 128-bit SQR T CSLA. The delay and the area analysis of various bits of modified SQR T CSLA are given below:

AREA OF REGULAR 16-bit SQR T CSLA:

Number of Slices: 25 out of 4656 2%
Number of 4 input LUT: 45 out of 9312 2%
Number of IO's: 50

Device Utilization Summary				Device Utilization Summary			
Logic Utilization	Used	Available	Utilization	Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	56	66,560	1%	Number of 4 input LUTs	116	66,560	1%
Number of occupied Slices	30	33,280	1%	Number of occupied Slices	62	33,280	1%
Number of Slices containing only related logic	30	30	100%	Number of Slices containing only related logic	62	62	100%
Number of Slices containing unrelated logic	0	30	0%	Number of Slices containing unrelated logic	0	62	0%
Total Number of 4 input LUTs	56	66,560	1%	Total Number of 4 input LUTs	116	66,560	1%
Number of bonded IOs	51	633	8%	Number of bonded IOs	99	633	15%
Average Fanout of Non-Clock Nets	2.51			Average Fanout of Non-Clock Nets	3.02		

Fig 5. 16-bit modified SQR T CSLA Fig 6. 32-bit modified SQR T CSLA

Maximum combinational path delay: 15.397ns

Maximum combinational path delay: 24.163ns

Device Utilization Summary				Device Utilization Summary			
Logic Utilization	Used	Available	Utilization	Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	227	66,560	1%	Number of 4 input LUTs	455	66,560	1%
Number of occupied Slices	126	33,280	1%	Number of occupied Slices	252	33,280	1%
Number of Slices containing only related logic	126	126	100%	Number of Slices containing only related logic	252	252	100%
Number of Slices containing unrelated logic	0	126	0%	Number of Slices containing unrelated logic	0	252	0%
Total Number of 4 input LUTs	227	66,560	1%	Total Number of 4 input LUTs	455	66,560	1%
Number of bonded IOs	195	633	30%	Number of bonded IOs	387	633	61%
Average Fanout of Non-Clock Nets	2.52			Average Fanout of Non-Clock Nets	2.53		

Fig 7. 64-bit modified SQR T CSLA Fig 8. 128-bit modified SQR T CSLA

Maximum combinational path delay: 74.755ns

Maximum combinational path delay: 74.755ns

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of 4 input LUTs	928	66,560	
Number of occupied Slices	496	33,280	
Number of Slices containing only related logic	496	496	
Number of Slices containing unrelated logic	0	496	
Total Number of 4 input LUTs	928	66,560	
Number of bonded IOs	771	633	

Fig 9. 256-bit modified SQR T CSLA

Maximum combinational path delay: 143.274ns

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III. SIMULATION RESULTS

The design implemented in this paper is programmed using the Verilog HDL and compiled using the Xilinx ISE and implemented using the Isim software. The simulation results shows there is a reduction of power in increase of each bit. The power consumption of the 256-bit modified SQRT CSLA is 0.418 watts. The simulation results show that peak memory used by the 256-bit modified SQRT CSLA is 167MB which is very low when compared to the regular CSLA.

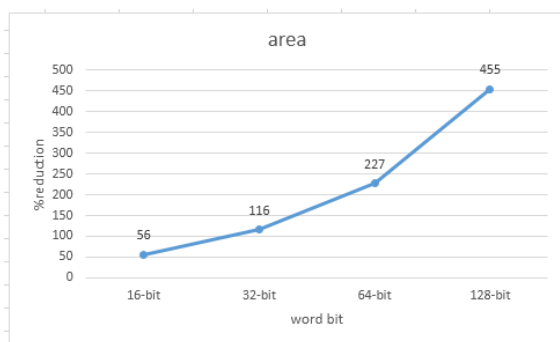


Fig 9. Area analysis

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Average Fanout of Non-Clock Nets:      3.05
Peak Memory Usage: 339 MB
Total REAL time to MAP completion: 3 secs
Total CPU time to MAP completion: 3 secs
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Fig 10. Non Clock Nets

IV. CONCLUSION

The simple approach is implemented in this paper to reduce the area, power consumption and delay of regular SQRT CSLA. The synthesis results show that the modified 256-bit SQRT CSLA has a decrease in area and power with the increase in the number of bits. From the analysis of the graph, delay is reduced and the number of the input is also decreased. The utility of the power of the 256-bit modified SQRT CSLA is also less. The total RAM used in the 256-bit modified SQRT CSLA is 339MB and is low when compared to the regular SQRT CSLA. In this paper the simulation is done using SPARTAN3 family, latest versions will yield better results. The novelty of our approach is been justified by the calculated comparison made with that of the results obtained by Xilinx simulation

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