

## International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

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Vol. 7, Issue 4, April 2018

# Common Mode Voltage Reduction in a Three Level Neutral Point Clamped Inverter Using Modified SVPWM

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**ABSTRACT:** In this paper, a new method to reduce the common mode voltage (CMV) at output terminal of the three level neutral point clamped (NPC) inverter is proposed. Space vector pulse width modulation (SVPWM) technique is used to generate gate pulses for the three level NPC inverter. In conventional SVPWM for three level NPC inverter, 27 voltage vectors are used. But in the proposed method only 19 voltage vectors are used in order to reduce the CMV. By using the modified method, the CMV can be reduced to about one-sixth of the DC input voltage. This technique is mainly suitable for high power, medium voltage applications. The effectiveness of the proposed method is verified using matlab simulation results.

**KEYWORDS:** Multilevel inverters, Space vector pulse width modulation, Neutral point clamped inverter, Common mode voltage .

### I. INTRODUCTION

Multilevel inverters are gaining high popularity and increased application, particularly in high power and medium voltage applications [1]-[2]. By using multilevel inverters, problems like motor bearing damage, electromagnetic interference (EMI), switching losses, high dv/dt, breakdown of winding insulation, and motor leakage current in two level inverters can be reduced [3]-[4]. The main advantages of these inverters are improving quality of voltage waveforms and an increase in the dc-link voltage for a given blocking voltage capacity of the semiconductors [5]. Multilevel inverters give smooth output waveforms when the levels are increased simultaneously [6]-[8].

There are mainly three multilevel inverter topologies which are neutral point clamped (NPC) inverters, flying capacitor (FC) inverters and cascaded H-bridge (CHB) inverters. Among these, common mode voltage (CMV) in NPC inverter is a major problem [9]. CMV is mainly caused due to switching action of rectifier and inverter. It is zero sequence voltages superimposed with switching noise. If not mitigated, they can cause problems like leakage current through motor bearings which can cause flash over of bearing lubricant and corrosion of ball bearings, high shaft voltages which can cause insulation issues and finally mechanical failure of the drive system [10]-[11].

In this paper a modified space vector pulse width modulation (SVPWM) technique is proposed to reduce the CMV in three level NPC inverter. The proposed SVPWM technique utilises only 19 voltage vectors as compared with the conventional SVPWM which utilises 27 voltage vectors. The proposed SVPWM technique shows a remarkable reduction in CMV, as much as  $V_{dc}/6$  as compared with the conventional SVPWM technique. The validity of the proposed method is verified by simulation results.

Paper is organized as follows. Section II describes the related work on the structure of three phase three level NPC inverter, its space vector diagram and the CMV obtained. The proposed SVPWM method for three phase three level NPC inverter which utilises only 19 voltage vectors is explained in Section III. Section IV presents simulation results showing results of CMV using conventional and modified SVPWM method. Finally, Section V presents conclusion.

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## II. RELATED WORK

### CMV In Three Level NPC Inverter

Fig. 1 shows the structure of three phase three level NPC inverter. It is composed of two capacitors for a common DC-link, four active switches  $S_{A1}$ ,  $S_{A2}$ ,  $S_{A3}$  and  $S_{A4}$  and two clamping diodes  $D_{A1}$  and  $D_{A2}$  in each phase leg. The switches  $S_{A1}$  and  $S_{A3}$  and  $S_{A2}$  and  $S_{A4}$  are two complementary pairs in phase A. Similarly the switches  $S_{B1}$  and  $S_{B3}$  and  $S_{B2}$  and  $S_{B4}$  are complementary pairs in phase B and switches  $S_{C1}$  and  $S_{C3}$  and  $S_{C2}$  and  $S_{C4}$  are complementary pairs in phase C.

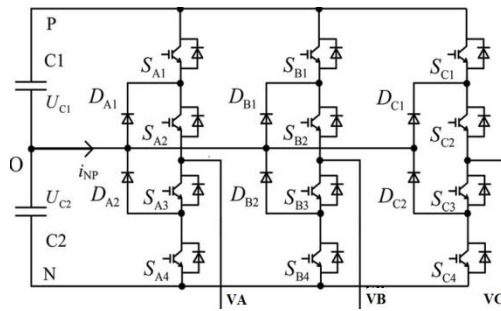


Fig. 1. Structure of three level NPC inverter

The conventional SVPWM which utilizes all the 27 voltage vectors is shown in Fig. 2. The 27 voltage vectors include six long vectors, six medium vectors, twelve small vectors and three zero vectors. The space vector diagram is a hexagon which is divided into six triangular sectors. Each triangular sector is further divided into four triangular regions [12]. The reference voltage vector is obtained by the nearest three voltage vectors which is given by the equation

$$V_{ref} T_s = V_a T_a + V_b T_b + V_c T_c \quad (1)$$

$$T_s = T_a + T_b + T_c \quad (2)$$

where  $T_a$ ,  $T_b$  and  $T_c$  are the dwell times of vectors  $V_a$ ,  $V_b$  and  $V_c$  respectively.

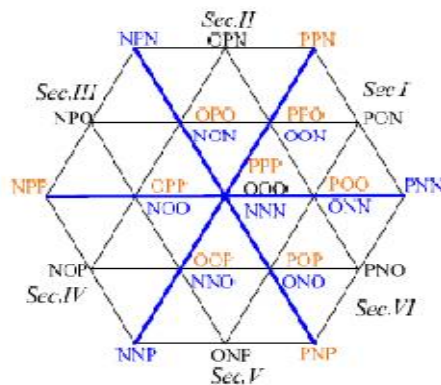


Fig. 2. Conventional SVPWM for three level NPC inverter

The switching states of three level NPC inverter and its pole voltage for phase A is shown in Table 1.

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Table 1: Switching States of Each Leg of the Inverter

Symbol	Switching States				Terminal Voltage
	S1X	S2X	S3X	S4X	
P	ON	ON	OFF	OFF	E
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-E

The CMV of the NPC inverter is expressed as the three phase pole voltages and is expressed as :

$$V_{CMV} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \quad (3)$$

where  $V_{AO}$ ,  $V_{BO}$  and  $V_{CO}$  are the pole voltages of the inverter [6]. In conventional SVPWM, the CMV of three level NPC inverter varies between  $-V_{dc}/3$  to  $V_{dc}/3$  with a voltage step of  $V_{dc}/6$  [12].

### III. PROPOSED METHOD FOR REDUCING CMV

In the proposed method, instead of using all the 27 voltage vectors in conventional SVPWM, only 19 voltage vectors are utilised in the modified SVPWM in order to reduce the CMV. The space vector diagram of the three level NPC inverter using modified SVPWM is shown in Fig. 3. In the modified SVPWM six long vectors, six medium vectors and only six small vectors and one zero vector is utilised in order to reduce the voltage level of CMV. So with the modified SVPWM technique, the CMV of the inverter varies between  $-V_{dc}/6$  and  $V_{dc}/6$  with a step change of  $V_{dc}/6$ .

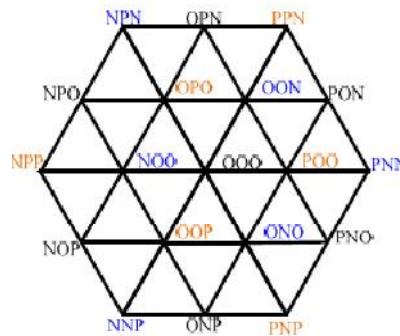


Fig. 3. Modified SVPWM for three level NPC inverter

### IV. SIMULATION RESULTS

The proposed method is verified by using matlab simulation model and its results. The parameters used for the simulation of the three level NPC inverter is shown in Table II.

Table 2 : Parameters For Simulation Of NPC Inverter

Parameters	Values
DC input voltage	400 V
DC link capacitance	200F
Switching frequency	5 kHz
Rated output frequency	50 Hz

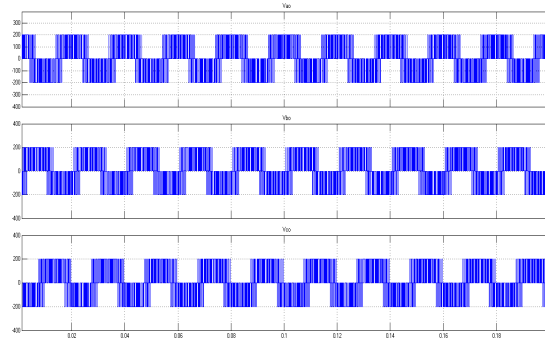
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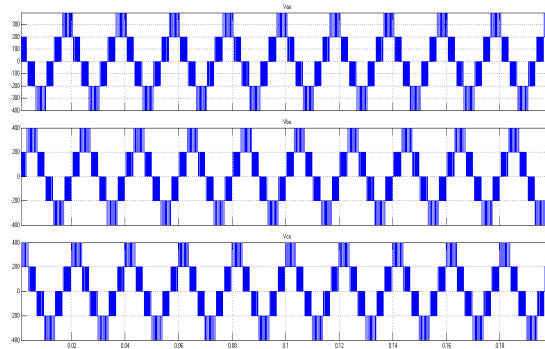
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Fig. 4 shows the outputs obtained when the NPC inverter is operated with conventional SVPWM. The pole voltage of the inverter is shown in Fig. 4(a).



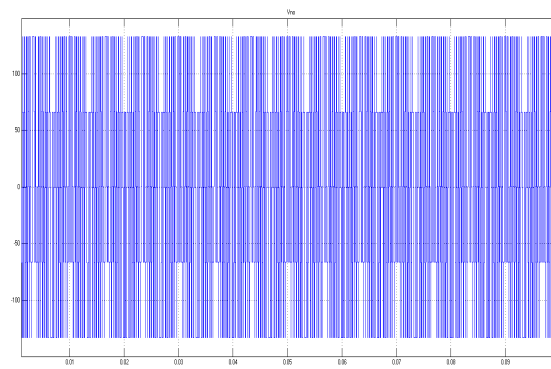
(a)

Fig. 4(b) shows the line to line voltage of the inverter, the magnitude of which are +400 V, +200 V, 0 V, -200 V and -400 V.



(b)

The CMV of the inverter with conventional SVPWM is shown in Fig. 4(c) which has voltage levels of +133.33 V, 66.66 V, 0 V, -66.66 V and -133.33 V.



(c)

Fig. 4 Output of NPC inverter using conventional SVPWM (a) Pole voltage (b) Line to line voltage (c) Common mode voltage

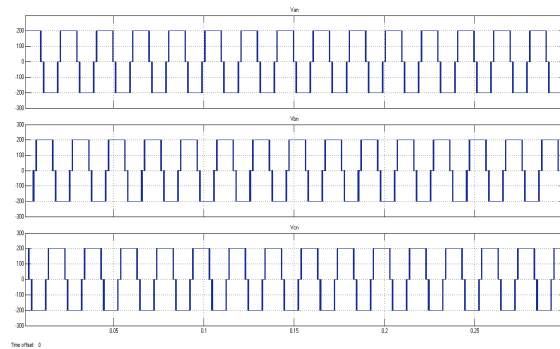
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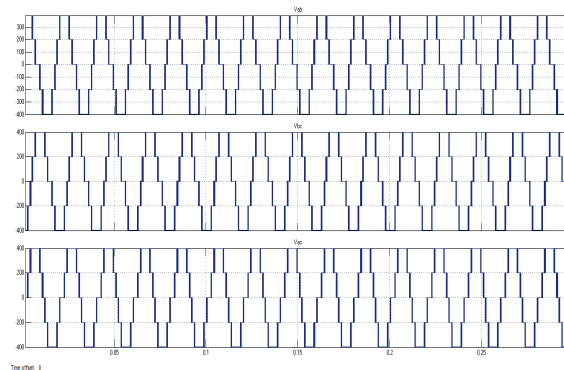
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Fig. 5 shows the outputs obtained when the NPC inverter is operated with modified SVPWM. The pole voltage of the inverter is shown in Fig. 4(a).



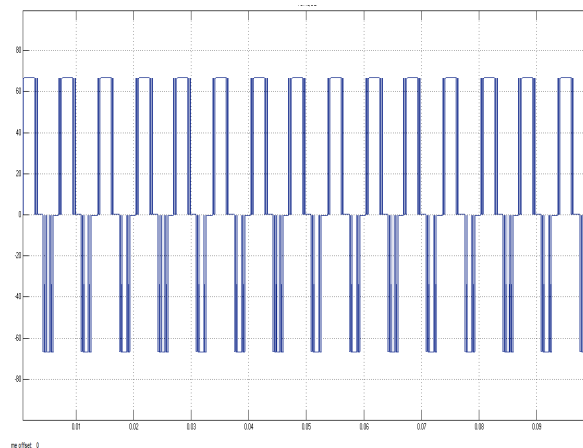
(a)

Fig. 4(b) shows the line to line voltage of the inverter, the magnitudes of which are same as that obtained from conventional SVPWM.



(b)

The CMV of the inverter with modified SVPWM is shown in Fig. 4(c) which has voltage levels of +66.66 V, 0 V and -66.66V.



(c)

Fig. 4 Output of NPC inverter using regular SVPWM (a) Pole voltage (b) Line to line voltage (c) Common mode voltage

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## V. CONCLUSION

This paper has proposed a modified CMV reduction technique for the three phase three level NPC inverter which is applicable for medium voltage and high power industrial drives. The CMV of the NPC inverter using modified SVPWM has reduced the common voltage to  $V_{dc}/6$ , 0 and  $-V_{dc}/6$ . The proposed method has been verified by matlab simulation results.

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