

VLSI Architecture for Reversible Multiplier-less Finite Impulse Response using Reversible Gate

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ABSTRACT: In present improvement, the reversible logic configuration entrancing more consideration because of its low power utilization. Reversible logic is extremely huge in low-control circuit design. The basic reversible gate utilized for reversible logic amalgamation are Feynman Gate, Fredkin gate, Toffoli gate and peres gate and so forth. In this paper, a proficient engineering of FIR channel structure is displayed. For accomplishing low power, reversible logic method of operation is actualized in the plan. It additionally gives brief thought to manufacture snake circuits utilizing the essential reversible gate like peres gate and TSG gate.

KEYWORDS: Finite Impulse Response, Distributive Arithmetic, Reversible Gate

I. INTRODUCTION

A digital filter can be defined as a filter which operates on digital signals, such as sound represented inside a computer. Keeping in mind the end goal to change over a yield computerized motion into simple shape, it is important to play out extra flag handling to acquire the perfect result and is demonstrated in Figure 1.

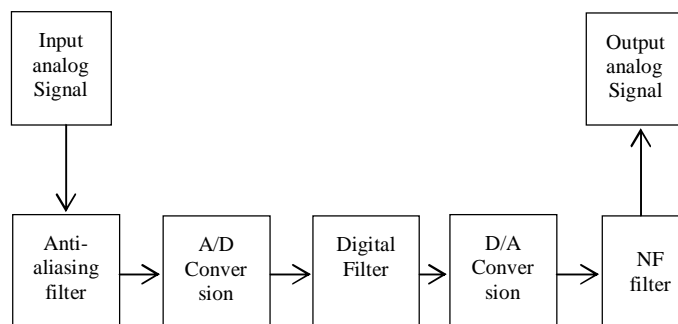


Figure 1: Digital Filter

Higher execution is workable for high volume applications by constraining the scope of parameters [1]. Standard channel items strike a harmony between advanced channel structures and programmability by offering a line of configurable channels. At the end of the day, these items are capacity particular, with advanced designs and programmable parameters [2]. Reasonable Differences exist in Frequency-Domain Versus Time Domain. Contemplating simple channels, most designers are agreeable in the time area. For instance, the operation of a RC low-pass channel can undoubtedly be imagined as a capacitor charging and releasing through a resistor [3]. Similarly, it is anything but difficult to imagine how a negative-input dynamic channel utilizes stage move as a component of recurrence, which is a period area operation. An advanced channel is better conceptualized in the recurrence area. The channel execution essentially plays out a convolution of the time area motivation reaction and the tested flag. A channel is composed with a recurrence space motivation reaction which is as near the sought perfect reaction as can be

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produced while given with the imperatives of the execution. The recurrence space drive reaction is then changed into a period area motivation reaction which is changed over to the coefficients of the channel.

In modern FPGAs, CLBs with more than 4 inputs are integrated into the single slices. Multiplexers in CLB can be also used for realization of logic function with more than 4 inputs; they allow combined output of LUTs CLBs for realization of main logic in FPGA. It typically consists of 4-input Lookup Tables (LUT), multiplexers and flipflops. LUT is used for realization of combinational logic. It is a 16-bit configurable memory which is capable to realize all 4-input combination logical functions. The output of the LUT can be registered to realize sequential functions. In modern FPGAs are also CLBs with more than 4 inputs integrated. Multiplexors in CLB can be also used for realization of logic function with more than 4 inputs; they allow the combination of the outputs of LUTs in FPGA is higher.

Channels can be characterized in a few distinct gatherings in light of various criteria. The two noteworthy sorts of advanced channels are: limited motivation reaction (FIR) computerized channel and unending drive reaction (IIR) computerized channel.

II. FIR FILTER

The term limited motivation reaction emerges on the grounds that the channel yield is processed as a weighted, limited term whole, of past, present, and maybe future estimations of the channel input, i.e.,

$$y(n) = \sum_{k=-M_1}^{M_2} b_k x(n-k) \quad (1)$$

Where both M_1 and M_2 are finite

One of the simplest FIR filters that may be considered is a 3-term moving average filter of the form

$$y(n) = (x[n+1] + x[n] + x[n-1]) \quad (2)$$

A FIR channel depends on a sustain forward distinction equation– Feed-forward implies that there is no criticism of past or future yields to frame the present yield, simply input related terms.

The fundamental qualities of Finite Impulse Response (FIR) channels are:

- Linear phase characteristic
- High filter order (more complex circuits)
- Stability
- There is also a need to be able to store filter coefficients in memory
- FIR designs by windowed sink or frequency sampling are simple
- FIR equiripple designs allow better control of frequency breakpoints and of pass band and stop band ripple.
- It is more complicated to implement, but that was solved 30 years ago...
- More coefficients: closer to desired response
- Wider transition band: less ripple in pass band, more stop band attenuation.

III. REVERSIBLE LOGIC GATE

Quantum Computation and Quantum records is the observe of statistics processingmission that may be carried out the use of Quantum mechanical systems. Its miles relatively newand rising place in the subject of computing that taught us to suppose physically aboutcomputation. This technique yields many new and interesting capabilities for statisticsprocessing and verbal exchange [4]. Quantum Computing may be a total change in how thecomputer will function and feature. The explorations in this field may additionally sooner or later result inrecords processing devices with skills far past today's computing andcommuniqué structures.

Reversible Computation is essential element necessary for Quantum Computation. The general benefit of creating the computation reversible on a Classical pc isthat heat dissipation is decreased and new strategies like Quantum Computing can beapproached with this foundational exchange in the manner processing is executed. Suchaggregate of Classical and Quantum computers would be necessary, seeing that ourbelief is classical.

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The number one objective of this thesis is to gain perception into the Reversible Computation and its use in Quantum Computing and to take a look at Quantum information Processing [5]. But the primary task that changed into diagnosed to be pursued as a focal issue round which the principles of Reversible and Quantum Computation had been to be constructed is: determining the function of growth in the quantity of “ancilla” bits and “rubbish” bits irreversible computing in comparison with traditional performance with respect to the implementation of basic circuits. Additionally to discover how reversible circuit can be optimized in terms of variety of gates, garbage bits and logical complexity.

IV. DISTRIBUTED ARITHMETIC TECHNIQUE

Distributed arithmetic (DA) design approach is considered to develop low complexity hardware structures for inner-product computation involving a constant vector [6]. DA was first studied by Croisier et al. (1973). Subsequently, White (1989) developed mathematical formulation to perform inner product computation using DA and developed structures to perform computations of DA algorithm using logic and memory resources. The inner product computation of a constant vector A with an input vector X of length P each is expressed as:

$$Y = \sum_{i=0}^{P-1} A_i X_i \quad (3)$$

Where $\{A_i\}$ and $\{X_i\}$ are the i^{th} component of vector A and X , respectively, suppose, X_i is a W -bit 2 's-complement binary fraction scaled such that $|X_i| < 1$, then $\{X_i\}$ each expressed as

$$X_i = -x_{i,0} + \sum_{j=1}^{W-1} x_{i,j} 2^{-j} \quad (4)$$

Where, $x_{i,0}$ is the sign bit, and $x_{i,W-1}$ is the least significant bit (LSB). Substituting (3) in (4), we have

$$Y = \sum_{i=0}^{P-1} A_i (-x_{i,0} + \sum_{j=1}^{W-1} x_{i,j} 2^{-j}) \quad (5)$$

$$Y = -\sum_{i=0}^{P-1} A_i x_{i,0} + \sum_{i=0}^{P-1} A_i \sum_{j=1}^{W-1} x_{i,j} 2^{-j} \quad (6)$$

The memory read operation of $F(x_j)$ on the LUT produces C_j . The LUT stores 2^W possible values of C_j corresponding to P -point bit-vector x_j . The bit-vector x_j is used as the address to read the corresponding C_j value from the LUT. Therefore, the DA computation is broadly split into two parts; (i) LUT read operation, and (ii) successive shift accumulation. From the P -point input-vector X , W input bit-vectors (bit-slice vectors) of size P -bit each are obtained, where W is the bit-width of each component of X [7].

These bit-slices are fed to the address line of the LUT storing 2^W possible values of C_j in LSB to MSB order. The LUT read values corresponding to successive bit-slices of input-vector X are shift accumulated in an adder unit. The block diagram of DA computation is shown in Figure 2. The LUT and accumulator structure of DA easily fit into the FPGA fabric as the FPGA provides 4-input LUTs. Keeping this in view, several DA based designs have been proposed in the literature for efficient implementation of most commonly used DSP algorithms such as digital filtering and transforms involving inner product computations [Chen (1985);

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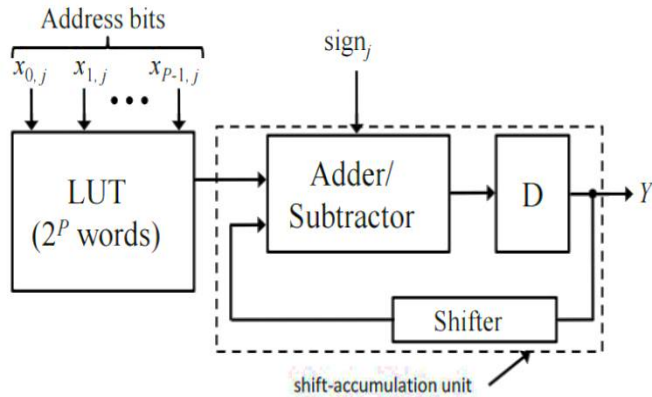


Figure 2: The block diagram of DA computation of inner-product of two P-point vectors [8]

V. PROPOSED ALGORITHM

The multiplier based and multiplier less finite impulse response (FIR) shown in figure 3 and figure 4 respectively. In multiplier based technique are used to input sample is passing through the delay flip flop and so on. All input is multiplier the filter coefficient and add the output of the multiplier.

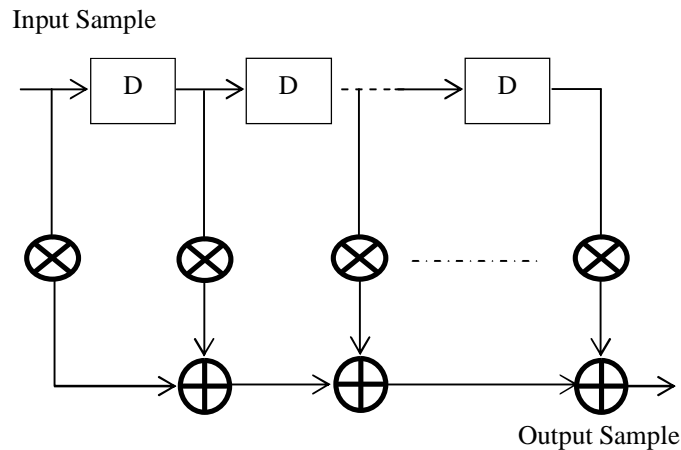


Figure 3: Multiplier based FIR Filter

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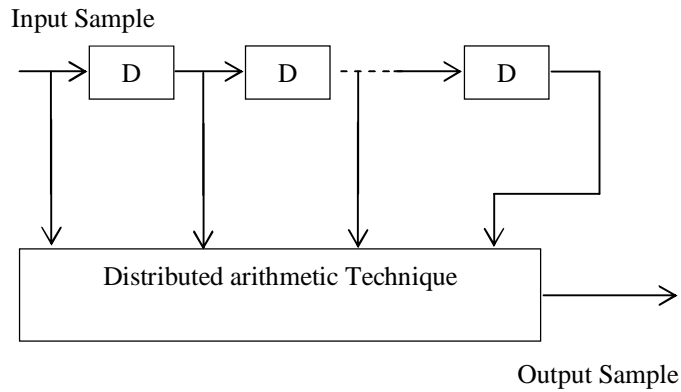


Figure 4: Multiplier-less FIR Filter

VI. SIMULATION RESULT

Multiplier based FIR filter and multiplier less distributive arithmetic technique based FIR filter is implemented Xilinx 14.1i with register transfer level (RTL) and verified VHDL test bench.

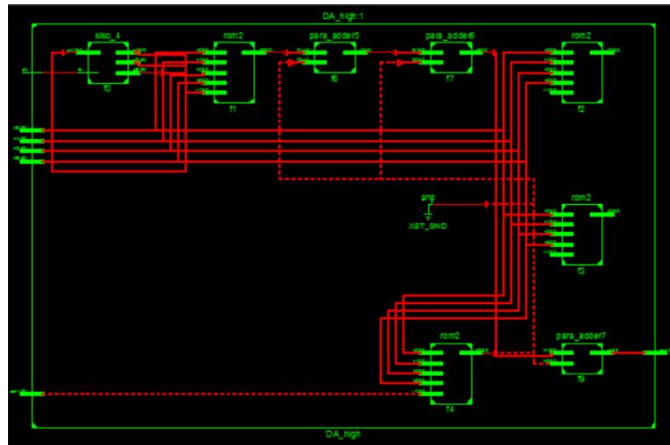


Figure 5: RTL view of multiplier less distributive arithmetic based FIR filter

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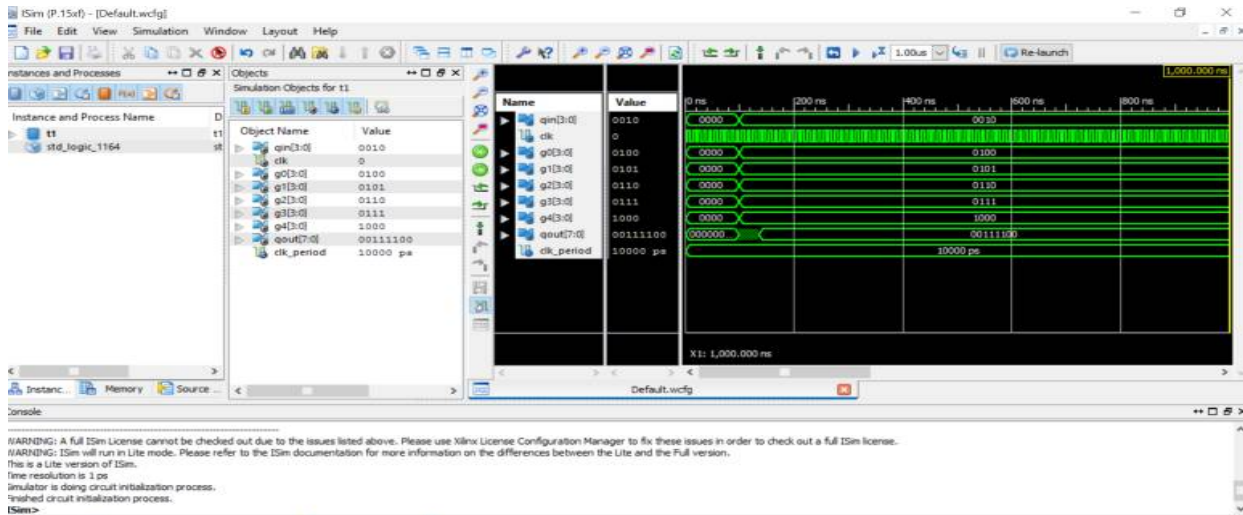


Figure 6: VHDL test waveform of multiplier less distributive arithmetic based FIR filter

Figure 5 and Figure 6 are shows the RTL view and VHDL test waveform of multiplier less distributive arithmetic based FIR filter. Proposed algorithm and previous algorithm are shows result in Table I to Table III. The proposed algorithm is efficient delay and slice in previous algorithm. Table I shows the result of the advance HDL synthesis report and Table II shows the result of the synthesis device family.

Table I: Advance HDL Synthesis Report

Architecture	Register	Xor
Multiplier based FIR	32	432
Multiplier less FIR Filter	12	356

Table II: Synthesis Device Report

Architecture	Slice Registers	LUTs	FF Pairs
Multiplier based FIR	37	186	34
Multiplier less FIR Filter	27	141	19

Table III: Timing Summary

Architecture	Minimum Period	Maximum Frequency
Multiplier based FIR	4.654 nsec	419.643 MHz
Multiplier less FIR Filter	1.598 nsec	625.821 MHz

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VII. CONCLUSION

In this paper, a FIR filter using reversible multiplier less distributive arithmetic technique for area efficient design is implemented. . The above designs are modeled using VHDL. Xilinx Project Navigator 14.2 is used as a synthesis tool and ISE simulator is used for simulation. The proposed architecture achieves better advantages in terms of area, LUTs and delay when compared to other architectures.

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