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# Review Paper on Flash Memory for High-Performance Storage Devices

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**ABSTRACT:** In this paper, a comparison of existing pulse triggers flip flop system with various techniques is presented. Flash memory is a non-volatile memory chip used for storage and for transferring data between a personal computer (PC) and digital devices. It has the ability to be electronically reprogrammed and erased. It is often found in USB flash drives, MP3 players, digital cameras and solid-state drives. Flash memory is a type of electronically erasable programmable read only memory (EEPROM), but may also be a standalone memory storage device such as a USB drives. EEPROM is a type of data memory device using an electronic device to erase or write digital data. Flash memory is a distinct type of EEPROM, which is programmed and erased in large blocks.

**KEYWORDS:** Flip Flop, Pulse Trigger, Flash Memory

### I. INTRODUCTION

The reverie of modern smart electronic devices is curtailed without memory element. Basically memory element used in electronic devices like microprocessor is flip-flop. In the present era the biggest challenge in front of VLSI engineers is to design electronic chip's whose power consumption should be less and efficiency should be high with small in size. For achieving such goal the memory element used in chip (flip-flop) should also fulfill the desired requirement. Flip-flop is basically latch with clock, which means it can be divide into to part's one is clock which provide it speed and other is latch which act as a storage element. The power consumed in a flip-flop can be divide approximately equal between clock and latch.

There are various schemes like transmission gate, master-slave, and pulse triggered are used for designing memory element (FF). Among all other pulse triggered approach has its own benefits. Some of the features associated with pulse triggered scheme are its single latch structure, simplified circuit, lower power consumption. The single latch structure of pulse triggered flip-flop gives it advantage of high speed over conventional master-slave flip flop.

In the United States, computer equipment accounts for about 2-3% of national electricity consumption. This figure is expected to increase as there is tremendous increase in household computer applications, Web phones, handheld computers, and internal terminals. These economic and environmental reasons have compelled the requirement for energy efficient computers. In order to meet the demand in high computational applications, the clock rate is steadily increasing and clock skew being an increasingly significant part of the clock cycle. The energy consumed by low-skew clock distribution networks is perpetually growing. Clock related power consumption can reach more than 30-40% of the total power of microprocessor and is becoming a larger fraction of the chip power. In addition, the number of logic gate delays in a clock period is reduced by 25% per generation. As a result, latency of flip flops or latches is becoming a larger portion of the cycle time.

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## II. LITERATURE SURVEY

Lopamudra Samal, Sauvagya Ranjan Sahoo, "A Novel Modified Low Power Pulse Triggered Flip-Flop", 2017 IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT) [1], reducing power consumption is a crucial task for any circuits. Increased demand for portable devices with reduced power dissipation has put necessary traction to design low power circuits. Both explicit and implicit pulse triggered flip flops are designed. Multiple Threshold CMOS (MTCMOS) technique and Self-controllable voltage level (SVL) circuit are employed to reduce power consumption. All the circuits are designed in 45nm technology for 1 GHz frequency.

Dennis land Larsen, Pere Llimos Muntal, Ivan H. H. Jørgensen and Erik Bruun, "High-voltage Pulse-triggered SR Latch Level-Shifter Design Considerations", 978-1-4799-5442-1/14/\$31.00 ©2014 IEEE [2], this paper compares pulse-triggered level shifters with a traditional level-triggered topology for high-voltage applications with supply voltages in the 50 V to 100 V range. It is found that the pulse-triggered SR (Set/Reset) latch level shifter has a superior power consumption of 1800  $\mu\text{W}/\text{MHz}$  translating a signal from 0-3.3 V to 87.5-100 V. The operation of this level-shifter is verified with measurements on a fabricated chip. The shortcomings of the implemented level-shifter in terms of power dissipation, transition delay, area, and startup behavior are then considered and an improved circuit is suggested which has been designed in three variants being able to translate the low-voltage 0-3.3 V signal to 45-50 V, 85-90 V, and 95-100 V respectively. The improved 95-100 V level shifter achieves a considerably lower power consumption of 438  $\mu\text{W}/\text{MHz}$  along with a significantly lower transition delay. The 45-50 V version achieves 47.5  $\mu\text{W}/\text{MHz}$  and a transition delay of only 2.03 ns resulting in an impressive FOM of  $2.03 \text{ ns} / (0.35 \mu\text{m} \cdot 50 \text{ V}) = 0.12 \text{ ns}/\mu\text{m V}$ .

Guang-Ping Xiang, Ji-Zhong Shen, Xue-Xiang Wu and Liang Geng, "Design of a Low-Power Pulse Triggered Flip-Flop with Conditional Clock Technique", 978-1-4673-5762-3/13/\$31.00 ©2013 IEEE [3], flip-flops are basic sequential elements in digital circuits and they have a deep impact on the performance of the circuits. In order to reduce the redundant transitions at internal nodes of the flip-flop, a conditional clock technique is proposed, and then a conditional clock pulse-triggered flip-flop (CCFF) based on this technique is designed. In CCFF, the clock is blocked when the input remains unchanged so that the internal nodes will not switch with the clock, which reduces the power consumption effectively. Based on the TSMC 0.18  $\mu\text{m}$  technology, the post-layout simulation results show that the proposed CCFF has an obvious advantage in power consumption when the data switching activity factor is below 50% as compared with other state-of-the-art pulse-triggered flip-flops, and the power saving is more than 50% when the activity factor is 10%.

Sebastien Bernard, Alexandre Valentian, Marc Belleville, David Bol and Jean-Didier Legat, "Design of a Robust and Ultra-Low-Voltage Pulse-Triggered Flip-Flop in 28nm UTBB-FDSOI Technology", 978-1-4799-1361-9/13/\$31.00 ©2013 IEEE [4], so far, pulse-triggered flip-flops (pulsed-FFs) are mainly used in high-performance digital circuits, thanks to their small data-to-output delay. However, they suffer from a poor robustness to local variations occurring at ultra-low voltage (ULV). Thanks to an innovative pulse generator, the operability of an energy-efficient pulsed-FF was validated at ultra-low operating supply voltage. Measurements of delays and correct functionality are performed in 28nm FDSOI technology. Then, the effect of back bias voltage, a key point in FDSOI technology, is studied and it is shown that our pulsed-FF reaches a minimum operating supply voltage of 170mV.

Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme", IEEE Transactions on Very Large Scale Integration (VLSI) Systems 1063-8210/\$31.00 © 2013 IEEE [5], in this brief, a low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using TSMC CMOS 90-nm technology, the proposed design outperforms the conventional P FF design data-close-to-output (ep-DCO) by 8.2% in data-to-Q delay. In the meantime, the performance edges on power and power-delay-product metrics are 22.7% and 29.7%, respectively.

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Yin-Tsung Hwang, Jin-Fa Lin, and Ming-Hwa Sheu, "Low-Power Pulse-Triggered Flip-Flop Design with Conditional Pulse-Enhancement Scheme", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, VOL. 20, NO. 2, FEBRUARY 2012 [6], in this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. First, the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the proposed design features the best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%. Compared with the conventional transmission gate-based FF design; the average leakage power consumption is also reduced by a factor of 3.52.

Xue-Xiang Wu and Ji-Zhong Shen, "Low-power explicit-pulsed triggered flip-flop with robust output", ELECTRONICS LETTERS 22nd November 2012 Vol. 48 No. 24 [7], a novel power-efficient explicit-pulsed dual-edge triggered flip-flop (SEDNIFF) is proposed. The proposed SEDNIFF puts the latch node inside its structure, which not only simplifies the latch structure but also strengthens the robustness of the output signal. Based on the TSMC0.18 mm technology, the post-layout simulation results show that the proposed flip-flop gains an improvement of up to 17.9 and 23.5% in terms of total average power and power-delay product, respectively, as compared with its counterparts.

### III. LOW POWER AND LOW VOLTAGE CMOS DESIGN

The design of portable devices requires consideration for peak power consumption to ensure reliability and proper operation. However, the time averaged power is often more critical as it is linearly related to the battery life. There are four sources of power dissipation in digital CMOS circuits: switching power, short-circuit power, leakage power and static power. The following equation describes these four components of power:

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} + P_{static} \quad (1)$$

$P_{switching}$  is the switching power. For a properly designed CMOS circuit, this power component usually dominates, and may account for more than 90% of the total power. Hence the energy provide by the supply source is

$$E = \int_0^{\infty} V_{dd} I(t) dt \quad (2)$$

Where

$$I(t) = \frac{V}{R} e^{-t/RC_L} \quad (3)$$

$I(t)$  is the current drawn from the supply Here,  $R$  is the resistance of the path between the  $V_{dd}$  and the output node.

### IV. PULSE TRIGGERED FLIP FLOP

In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In figure 1, shows the DSCH diagram of classic explicit P-FF design named date-close-to-output (ep-DCO). It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this design used 9 inverters, 2PMOS and 4 NMOS. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node is discharged on every rising edge of the clock in spite of the presence of a static input "1."

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Flash memory was first introduced in 1980 and developed by Dr. Fujio Masuoka, an inventor and mid level factory manager at Toshiba Corporation (TOSBF). Flash memory was named after its capability to erase a block of data “in a flash.” Dr. Masuoka’s objective was to create a memory chip preserving data when the power was turned off. Dr. Masuoka also invented a type of memory known as SAMOS and developed a 1Mb dynamic random access memory (DRAM). In 1988, Intel Corporation produced the first commercial NOR-type flash chip, which replaced the permanent read-only memory (ROM) chip on PC motherboards containing the basic input/output operating system (BIOS).

A flash memory chip is composed of NOR or NAND gates. NOR is a type of memory cell created by Intel in 1988. The NOR gate interface supports full addresses, data buses and random access to any memory location. The shelf life of NOR flash is 10,000 to 1,000,000 write/erase cycles.

NAND was not developed by Toshiba a year after NOR was produced. It is faster, has a lower cost per bit, requires less chip area per cell and has added resilience. The shelf life of a NAND gate is approximately 100,000 write/erase cycles. In NOR gate flash every cell has an end connected to a bit line and the other end connected to a ground. If a word line is “high” then the transistor proceeds to lower the output bit line.

Flash memory has many features. It is a lot less expensive than EEPROM and does not require batteries for solid-state storage such as static RAM (SRAM). It is non-volatile, has a very fast access time and has a higher resistance to kinetic shock compared to a hard disc drive. Flash memory is extremely durable and can withstand intense pressure or extreme temperatures. It can be used for a wide array of applications such as digital cameras, mobile phones, laptop computers, PDAs (personal digital assistants), digital audio players and solid-state drives (SSDs).

## V. DESIGN IMPLEMENTATION

MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification providing an innovative education initiative to help individuals to develop the skills needed for design positions in virtually every domain of IC industry.

The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH. It has some important points are,

- User-friendly environment for rapid design of logic circuits Supports hierarchical logic design
- Handles both conventional pattern-based logic simulation and intuitive on screen mouse-driven simulation
- Improved built-in extractor which generates a SPICE netlist from the schematic diagram (Compatible with PSPICETM and WinSpiceTM)
- Generates a VERILOG description of the schematic for layout conversion
- Immediate access to symbol properties (Delay, fanout) Model and assembly support for 8051 and PIC 16F84 microcontrollers Sub-micron, deep-submicron, nano scale technology support
- Supported by huge symbol library.

## VI. SIMULATION RESULT

The ep-DCO, CD and single feed-through techniques are used to design pulse triggered flip flop circuits. All design have be drawn by using the DSCH tool and verified by the level of the section in the designed circuit. The layout and the compilation could be verified using MICROWIND. DSCH and MICROWIND tools are used to carry out the work for different technologies like 25nm, 65nm and 90nm.

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## VII. CONCLUSION

This paper simulated ep-DCO, CD and single feed-through techniques designed with different transistor is having different power dissipation. The pulse triggered flip flops are simulated for 90nm, 65nm and 25nm nodes using the DSCH and MICROWIND tools. Hence from results, as the technologies is scaled down power dissipation increases.

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