

Design and Implementation of Partition Multiplier based on Brent Kung Adder

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ABSTRACT: In this paper a partition multiplier based on Brent Kung adder is presented. Partition multiplier is used in various applications i.e. digital systems, different types of filters and digital signal processing. We have design area efficient and less time consuming partition multiplier with the help of Brent Kung adder. All design is implemented VHDL platform and Xilinx 14.5 software. The Brent–Kung adder is a parallel prefix adder (PPA) and it is types of the carry-look ahead adder (CLA). It has higher normality with the structure of the adder and minimized the wiring issues, reduced complexities, provides better execution, faster and less area which is not the case with the ripple carry adder.

KEYWORDS: - Brent Kung Adder, Partition Multiplier, Delay, Carry Look Ahead Adder.

I. INTRODUCTION

Multiplier is the important function in arithmetic operations and CPU processing performance depends on it. Currently multiplier is used in many digital signal processing applications such as filtering, microprocessors in its arithmetic and logic units and Fast Fourier Transform (FFT). Since execution time of most DSP algorithms depends on the multiplication, so there is need of high speed multiplier. Currently determining the instruction cycle of a DSP chip totally depends on multiplication time. The high speed processing demand has been increasing day by day due to expending computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the higher performance in real time applications and image processing applications, one of the important key is high speed multiplications to achieve this performance and development of high speed multiplier has been subject of interests over decades. In this paper simple 16 bit partition multiplier is proposed which is based on Brent-kung adder. The main concept of this paper is decrease the delay and area of the conventional architecture.

II. PARTITION MULTIPLIER

In partition multipliers to determine the performance of the multiplier that given a number of partial products to be added is the main parameter. To reduce the number of partial products to be added, the Brent Kung adder (BKA) is one of the most popular adders in multiplication modules. The multiplication of two unsigned n-bit numbers, where $A = A_{n-1}, A_{n-2}, A_{n-3}, \dots, A_0$ is the multiplicand and $B = B_{n-1}, B_{n-2}, B_{n-3}, \dots, B_0$ is the multiplier.

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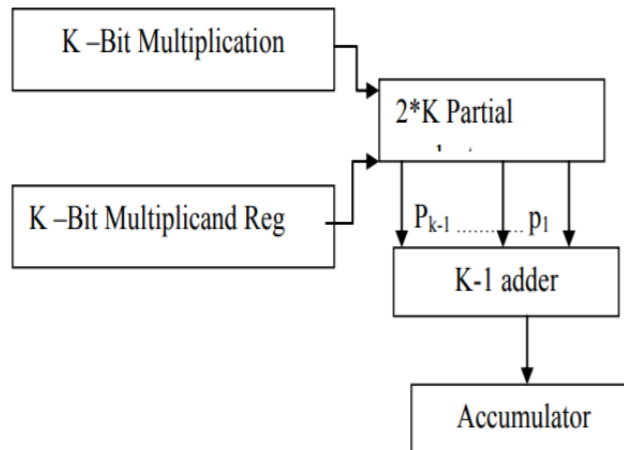


Figure 1: Partition multiplier multiplication

III. METHODOLOGY

Brent Kung Adder

The Brent–Kung adder is a carry look ahead adder and it is parallel prefix adder (PPA). In 1982, it is proposed by Richard Peirce Brent and Hsiang Te Kung. It has higher normality with the structure of the adder and has minimize the wiring issues, reduces complexities and provides better execution and less chip region which is not the case with the ripple carry adder (RCA) and also it is very faster than ripple-carry adders (RCA).

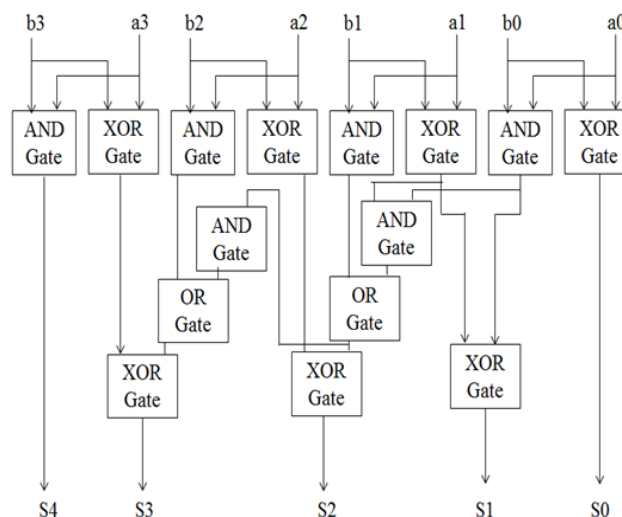


Figure 2: Block Diagram of Brent Kung Adder

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IV. IMPLEMENTATION METHODOLOGY

We consider two K-bit operands $a_{K-1}, a_{K-2}, \dots, a_2, a_1, a_0$ and $b_{K-1}, b_{K-2}, \dots, b_2, b_1, b_0$ for K by K multiplier, the partial products of two K-bit numbers are $a_i b_j$ where i, j go from $0, 1, \dots, K-1$. The longest two columns in the middle of the partial products contribute to the maximum delay. We then proceed to sum up each column of the two parts in parallel.

Partition Multiplier Method: - Let X and Y be numbers of p-bits such that multiplication of the inputs X and Y gives the 2p bits product. Here X and Y are split into q numbers as $X_0, X_1, X_2, \dots, X_{q-1}$ and

$Y_0, Y_1, Y_2, \dots, Y_{q-1}$ each consisting of r bits

Where

$$q = \frac{p}{r} \tag{1}$$

Consider the value of $p = 8, r = 2$

Then

$$q = 4 \tag{2}$$

X and Y can therefore be expressed as

$$X_0 = X \left(\frac{k}{2} - 1 \text{ to } 0 \right) \tag{3}$$

$$X_1 = X \left(k - 1 \text{ to } \frac{k}{2} \right) \tag{4}$$

$$Y_0 = Y \left(\frac{k}{2} - 1 \text{ to } 0 \right) \tag{5}$$

$$Y_1 = Y \left(k - 1 \text{ to } \frac{k}{2} \right) \tag{6}$$

Therefore X_0 contains the even partitions of X and X_1 contains the odd partitions of X, similarly Y_0 contains the even partitions of Y and Y_1 contains the odd partitions of Y. X_0 Contains multiplier all the partition of Y. X_0 is multiplier of Y_0 , the lower significant bit (LSB) of the X_0 add with LSB of the Y_0 bit position and most significant bit (MSB) of the X_0 add with MSB of the Y_0 bit position.

$$Z = X \times Y = X_0 \times Y_0 + X_0 \times Y_1 + X_1 \times Y_0 + X_1 \times Y_1$$

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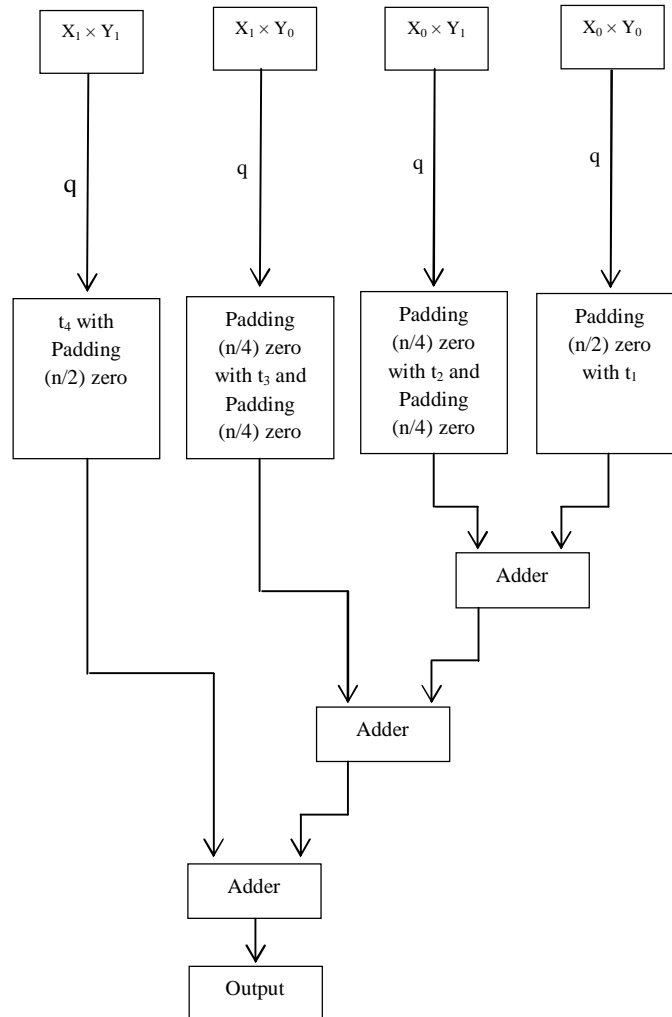


Figure 3: Flow chart of proposed partition multiplier method

V. SIMULATION RESULT AND DISCUSSION

VHDL Descriptions comprise of essential outline units and auxiliary configuration units. The essential outline units are the Entity and the Package. The optional configuration units are the Architecture and the Package Body. Optional configuration units are constantly identified with an essential outline unit. Libraries are accumulations of essential and optional configuration units.

A regular plan as a rule contains one or more libraries of configuration units. VHDL representation can be seen as content record portraying a computerized framework. The advanced framework can be spoken to in distinctive structures, for example, a behavioral model or a basic model. Most usually known as levels of deliberation, these levels help the planner to create complex frameworks effectively.

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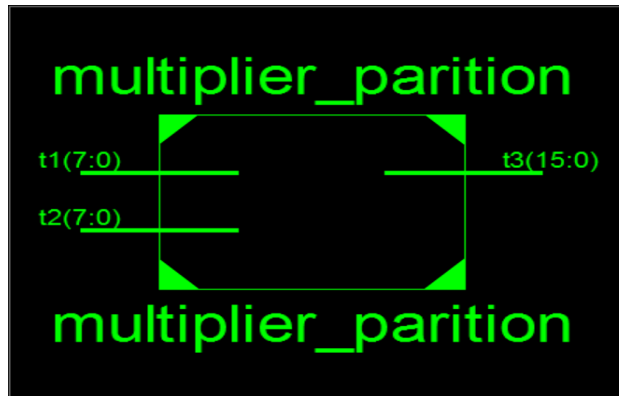


Figure 4: View Technology Schematic of Partition Multiplier

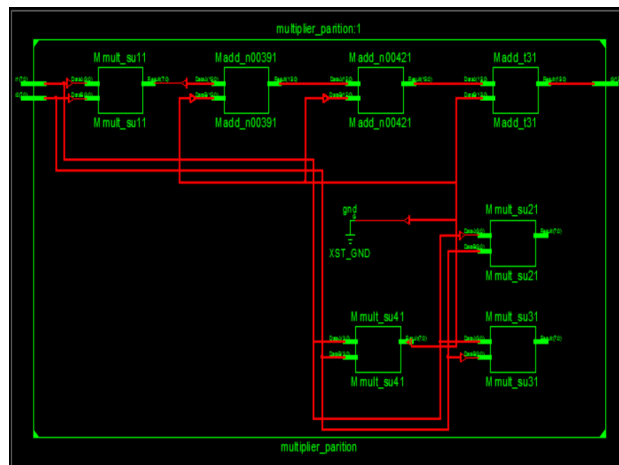


Figure 5: RTL View of Partition Multiplier

Device utilization summary:

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Selected Device : 4vfx12sf363-12

Number of Slices:           40 out of  5472    0%
Number of 4 input LUTs:    69 out of 10944    0%
Number of IOs:             32
Number of bonded IOBs:     32 out of   240   13%
Number of DSP48s:          3 out of    32    9%
Timing Summary:
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Speed Grade: -12

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 15.081ns

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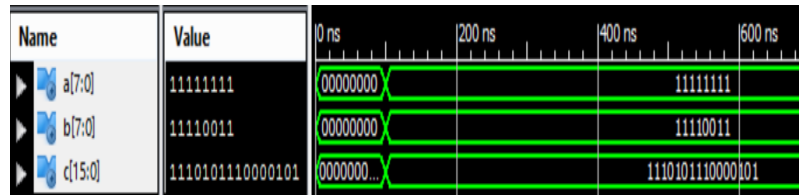


Figure 6: VHDL Test Bench of Partition Multiplier

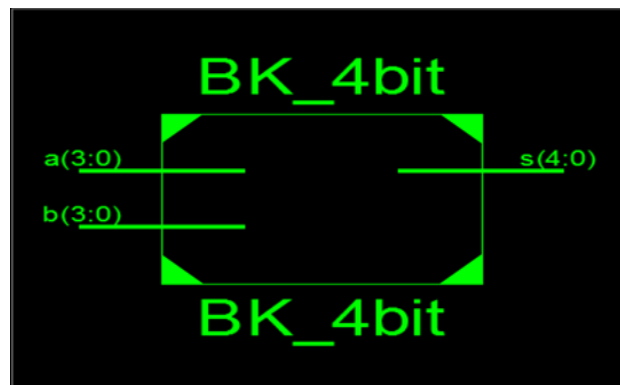


Figure 7: VTS for 4-bit BK Adder

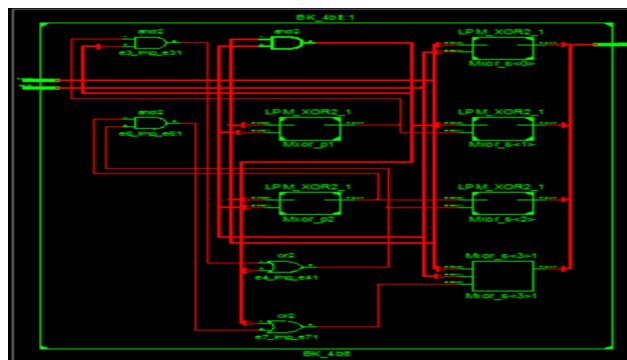


Figure 8: RTL View of 4-bit BK Adder

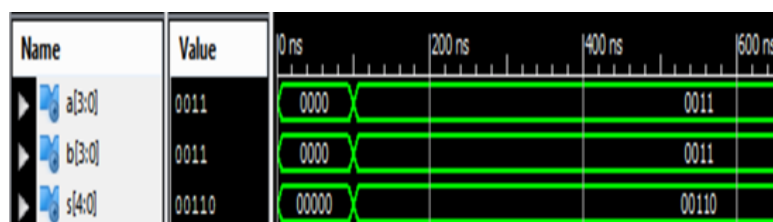


Figure 9: VHDL Test Bench of 4-bit BK Adder

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Table I: Comparisons result for implemented design and existing algorithm

Design	Width	Area Gate court
Ripple Carry Adder	4	52
	8	104
	16	208
	32	416
CSLA Adder	4	64
	8	128
	16	256
	32	512
Compressor based Adder	4	45
	8	90
	16	180
	32	360
Implemented Brent Kung Adder	4	43
	8	86
	16	172
	32	344

Table II: Comparison Result of Previous Multiplier and Proposed Multiplier

Bit	Previous Vedic Method	Proposed Partition Method
4-bit	10.43 ns	9.134 ns
8-bit	15.22 ns	11.631 ns
16-bit	19.58 ns	13.816 ns
32-bit	22.32 ns	16.234 ns

VI. CONCLUSION

In previous design, carry look ahead adder was used for designing parallel FIR filter but it was having the drawback that it was consuming more delay and large circuit complexity. So to remove this drawback, we have used Brent Kung adder which is an advanced binary adder. Its advantage is that it reduces the cost and the complexities of the circuit and is much faster than Ripple Carry adder and carry look ahead adder. So it provides better performance and less area to implement in comparison to Kogge Stone adder. The main advantage of Brent Kung adder is that it works on every bit and consumes less space.

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