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## Design and Implementation of Arithmetic and Logical Block Using QCA Technology

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**ABSTRACT:** In this paper an eight bit arithmetic and logical block is designed using QCA technology. QCA cells does not conducts the information as current as used in conventional logic circuits. It operates based on the concept of Columbic Interaction of the states of electrons in QCA cells. Quantum dot cellular automata (QCA) is one of the emerging technologies that shows features to overcome the limitations like high computation throughput and power consumption faced in CMOS technologies. A lot of research has been done in designing universal logic gates, combinational circuits, sequential circuits and ALU using QCA and has shown its efficiency due to its small size and high computational speed. Apart from these advantages of QCA, it also has a great potential for low power consumption. So far, the research in QCA circuit design was mainly based on irreversible circuits and as proved by Landauer in, that any circuits designed using traditional logic gates will inevitably loss information in the form of energy dissipation in a circuit. So, designing of eight bit ALU block at low power can be achieved by using QCA technology.

### I. INTRODUCTION

Quantum dot cellular automata (QCA) is one of the emerging technologies that shows features to overcome the limitations like high computation throughput and power consumption faced in CMOS technologies. A lot of research has been done in designing universal logic gates, combinational circuits, sequential circuits and ALU using QCA and has shown its efficiency due to its small size and high computational speed. Apart from these advantages of QCA, it also has a great potential for low power consumption. So far, the research in QCA circuit design was mainly based on irreversible circuits and as proved by Landauer in, that any circuits designed using traditional logic gates will inevitably loss information in the form of energy dissipation in a circuit.

Traditional logic functions such as AND, OR etc., are not reversible in nature as more than one input are mapped into one output state. But in reversible logic the logic functions have one to one correspondence between inputs and output, i.e., there is a distinct output assignment for each distinct input. Therefore, input can be distinctly determined from its output in reversible logic and hence no loss of information occurs in circuits designed using reversible logic.

Like all other emerging nanotechnologies such as quantum computing, optical computing, Spintronic, DNA computing, molecular computing etc., QCA also has applications of reversible logic. Reversible logic is proposed to maintain the trend according to Moore's Law and to minimize the energy dissipation occurring during computation. It is shown that information loss occurring in terms of energy dissipation while computing in traditional logic circuits would not occur if it is carried out in a reversible way.

Due to the rapid development of technology, the scenario of digital industry has changed in the past few years. Intel cofounder Gordon Moore in 1960 predicted that the number of transistors on a single chip will double in every eighteen months. According to his prediction, the conventional CMOS based devices advanced from micron to submicron,

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submicron to deep submicron and to manometer regime over last five decades. But the scaling of CMOS devices at nano scale affects the performance of several factors like heat dissipation and leakage currents. The heat generated can no longer dissipate and results in damage of the chip as more and more devices are packed into the same area. So many novel technologies and materials have been extensively researched and developed at nano scale to replace conventional transistor based VLSI technology.

Among several other alternatives, Quantum Dot Cellular Automata (QCA) is a revolutionary promising transistor less quantum paradigm that performs computation and routing information at nano domain. The unique feature of QCA is that logic states are represented by a cell. A cell is a nano scale device capable of transferring data by two state electron configurations. The advantages of QCA over conventional CMOS technology include lesser delay, high density circuits and low power consumption which permits us to perform quantum computing in near future.

QCA is an evolving nanotechnology and has capability to develop digital circuits with higher packaging density, reduced area, much lower power dissipation, and higher switching speed. QCA results in ultra-dense, high-performance digital devices as it works at nanometre scale. It is used to design new logic circuits which are basically a translation of standard logic devices. Dimensional scaling of CMOS based logic circuits is approaching its limit of feature size reduction. Further reducing the size of CMOS based circuits result in many problems and doesn't produce the necessary output required.

It is believed that the physical size and the corresponding performance of the various circuits based on CMOS technology is close to the reaching limit. Alternatives to conventional CMOS technology is QCA which provides higher density, lower dissipation of power, higher clock frequency and better output results are needed. Quantum Dot Cellular Automata (QCA) technology is explored and introduced. When a new technology is introduced, new design principles are also necessary to consider. The design nature of QCA is not very complicated, instead it is simple than the conventional technologies.

## II. LITERATURE SURVEY

This paper proposes a detailed design analysis of sequential circuits for quantum-dot cellular automata (QCA). This analysis encompasses flip-flop (FF) devices as well as circuits. Initially, a novel RS-type FF amenable to a QCA implementation is proposed. An algorithm for assigning appropriate clocking zones to a QCA sequential circuit is implemented. A technique referred to as stretching is used in the algorithm to ensure timing and delay matching. This algorithm relies on a topological sorting and enumeration step to consistently traversing only once the edges of the graph representation of the QCA sequential circuit.

QCA is a novel technology which provides implementation of digital circuits in nanoscale. QCA circuits work in higher speed, smaller size and less power consumption compared to conventional CMOS circuits. In this paper, a new design for T flip flop (T-FF), by using of special feature of QCA circuits capabilities, is proposed. This T-FF has additional inputs that can be used better in sequential circuits as memory elements. These inputs can reset and preset T-FF and no more cells needed to add them to the designed circuit. Proposed T-FF is simulated using the QCA Designer and simulation results prove its validity.

Quantum cellular automaton (QCA) is an efficient and emerging nanotechnology to create quantum computing devices. It is polarization based digital logic architecture. QCA cell is the basic unit to build logic gates and devices in quantum domain. This paper proposes an effective design of logic gates and arithmetic circuit using QCA. Here the gates and circuits are designed using minimum number of QCA cells and with no crossovers. So these designs can be used to construct complex circuits. The simulations of the present work have been carried out by means of QCA designer tools. The simulation results help to implement the digital circuits in nano scale range.

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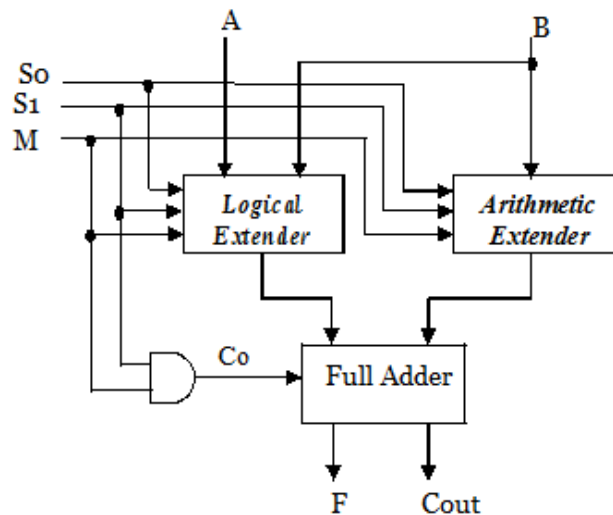
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A novel fault-tolerant full-adder for quantum dot cellular automata is presented. Quantum-dot cellular automata (QCA) are an emerging technology and a possible alternative for semiconductor transistor based technologies. A novel fault-tolerant full-adder is proposed in this paper: This component is suitable for designing fault-tolerant QCA circuits. The redundant version of full-adder is simple in structure and more robust than the standard style for this device. By considering two-dimensional arrays of QCA cells, fault tolerance properties of such block full-adder can be analyzed in terms of misalignment, missing and dislocation cells. In order to verify the functionality of the proposed device, some physical proofs are provided. The results confirm our claims and its usefulness in designing digital circuits. In modern era, Quantum-Dot Cellular Automata (QCA) is most promising and emerging technology to implement the digital logic circuit at nanoscale. Due to inherent unique characteristics of QCA, it can be possible to have device that can functions consuming high density, ultra low power and very fast clocking speeds. This work displayed an optimized design and implementation of basic flip-flops like *RS*, *JK*, *D* and *T* in QCA. The functionality and correctness of proposed flip flop circuits is verified by comparing the QCA Designer generated simulation result with truth table of proposed circuits. For general purpose nano processor, the proposed circuit can be used as basic building block.

### III. METHODS

The Arithmetic Logic Unit (ALU) performs the basic arithmetic and logical operation and consists of arithmetic extender, logical extender and one bit full adder as shown in figure 4.1. Three control signals determine the operation of the ALU. *M* is the mode control variable used to select between arithmetic and logical operations. *S1* and *S0* are used in combination with *M* to select between the eight arithmetic and logical operation the ALU supports.



**Fig 1. Architecture of ALU**

#### Arithmetic Extender

The Arithmetic extender modifies the second operand and passes it to the Full adder to the arithmetic.

According to truth table we write Boolean equation of arithmetic extender shown in equation (1) and design logic circuit of arithmetic extender shown in fig. 6.

$$Y = MS1' B + MS0' B \quad \dots (1)$$

#### Logical Extender

The logic operations are performed in the logic extender. The FAs are used simply as connection for the outputs.

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**TABLE 1.FUNCTION TABLE OF ARITHMETIC EXTENDER**

M	S <sub>1</sub>	S <sub>0</sub>	Function name	Function	X	Y	C <sub>0</sub>
1	0	0	Decrement	A-1	A	all 1's	0
1	0	1	Add	A+1	A	B	0
1	1	0	Subtract	A+B'+1	A	B'	1
1	1	1	Increment	A+1	A	all 0's	1

**TABLE 2.TRUTH TABLE OF ARITHMETIC EXTENDER**

M	S <sub>1</sub>	S <sub>0</sub>	B	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0
1	1	1	0	0
1	1	1	1	0

**TABLE 3.FUNCTION TABLE OF LOGICAL EXTENDER**

M	S <sub>1</sub>	S <sub>0</sub>	Function Name	Function	X	Y	C <sub>0</sub>
0	0	0	Complement	A'	A'	0	0
0	0	1	AND	A and B	A&B	0	0
0	1	0	Identity	A	A	0	0
0	1	1	OR	A or B	A B	0	0

**TABLE 4.FUNCTION TABLE OF LOGICAL EXTENDER**

M	S <sub>1</sub>	S <sub>0</sub>	X
0	0	0	A'
0	0	1	A & B
0	1	0	A
0	1	1	A   B
1	X	X	A

According to truth table we write Boolean equation of logical extender shown in equation (2) and design logic circuit of logical extender shown.

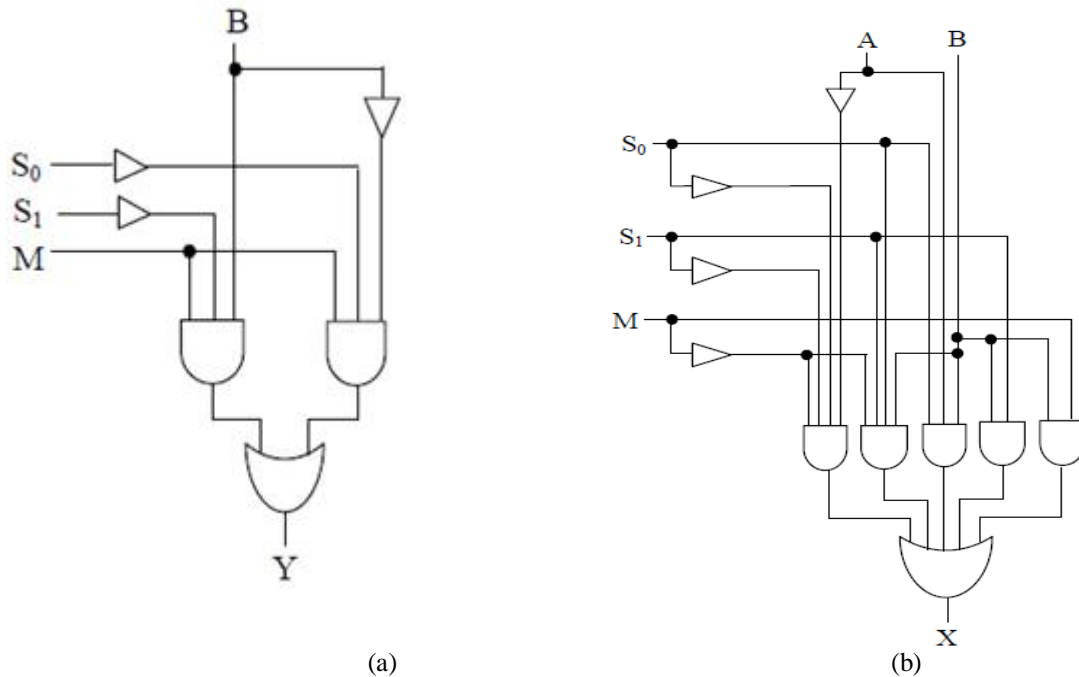
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$$X = M'S_1'S_0 + M'S_1S_0 + S_0AB + S_1A + MA \dots\dots(2)$$



(a) (b)  
**Fig 2.(a)Logic circuit of Arithmetic Extender (b) Logic circuit of Logical Extender**

### Full Adder

Full adder performs the addition of three bits. In full adder, we have given three inputs  $X$ ,  $Y$  and  $C_0$ , where  $C_0$  is carry in signals shown in equation (3).

$$C_0 = MS_1 \dots (3)$$

**TABLE 5. TRUTH TABLE OF FULL ADDER**

X	Y	$C_0$	F	$C_{out}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean equations for Full adder are shown in equations (4) & (5) and logic circuit of full adder as shown in figure 4.3.

$$F = X \oplus Y \oplus C_0 \dots (4)$$

$$C_{out} = MV X, Y, C_0 \dots (5)$$

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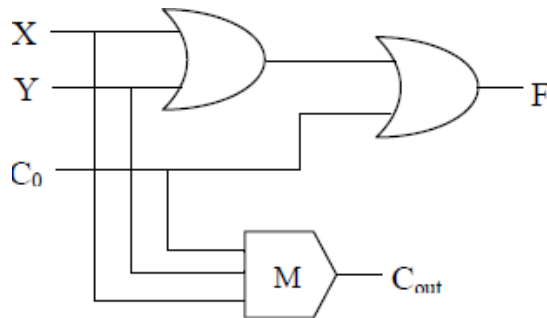


Fig .3.Logic Circuit for Full Adder

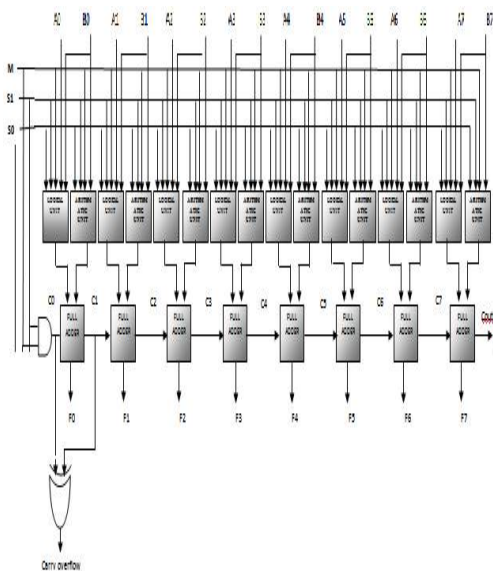


Fig. 4.Logic Circuit for 8-bit ALU

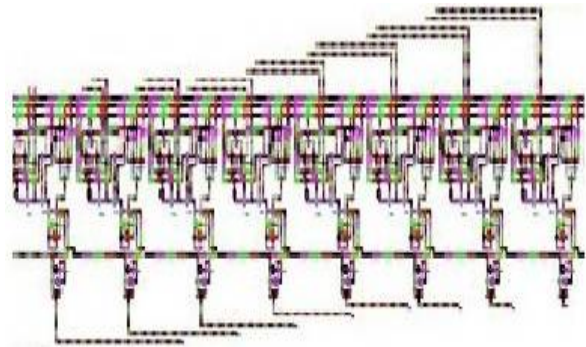


Fig. 5.Implementation of ALU Block in QCA Designer Tool

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## V. IMPLEMENTATION AND RESULTS

### 5.1 AND GATE:

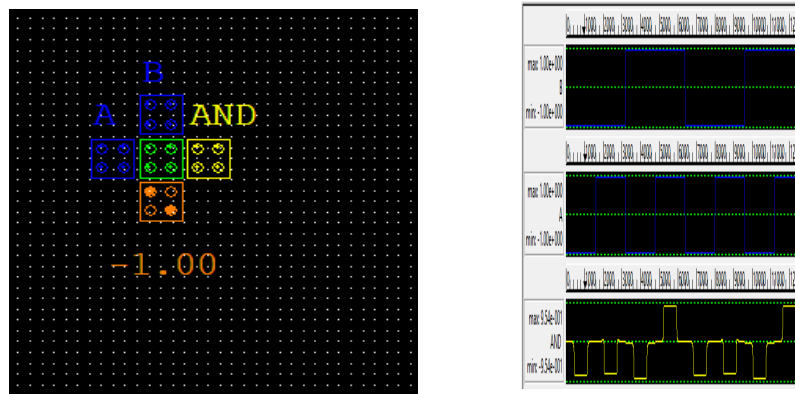


Fig.6. Implementation of QCA AND Gate, Output waveform for QCA AND Gate

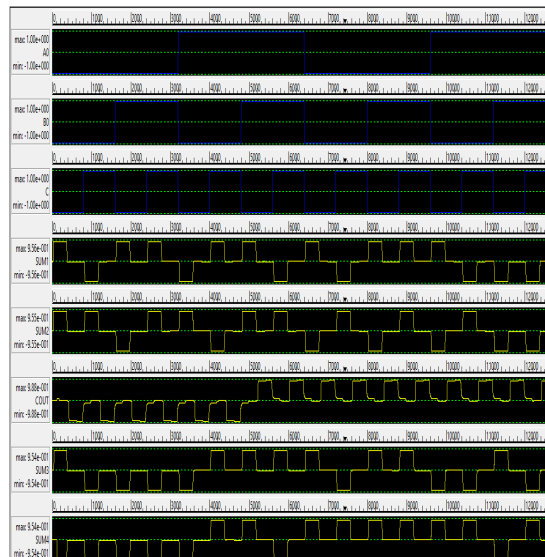


Fig 7. Output waveform for 8-bit ALU

## VI. CONCLUSION

In this paper, a standard equation from SR flip flop have designed and using that equation other flip flops like D, T and JK flip-flops are subsequently designed. The design of ALU block, which performs Arithmetic and Logical operations have designed. Any memory storage device can be built using the flip-flops designed in the above mentioned approach. The layout has been generated and simulation results are verified using QCA Designer simulation tool. The future work incorporates a two new QCA addition algorithm and the corresponding two-bit QCA adder structure that reduces the number of the majority gates and inverters required for existing designs.

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