

## International Journal of Innovative Research in Science, Engineering and Technology

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# Area Efficient VLSI Architecture for FFT using radix-2 Butterfly and Folding Technique

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**ABSTRACT:** The Discrete Fourier Transform (DFT) is an important technique in the field of Digital Signal Processing (DSP) and Telecommunications, especially for applications in Orthogonal Frequency Division Multiplexing (OFDM) systems. The Fast Fourier Transform (FFT) is an efficient algorithm to compute the DFT and its inverse. The FFT processor plays a key role in the field of communication systems such as Digital Video or Audio Broadcasting, Wireless LAN with Standards of IEEE 802.11, High Speed Digital Subscriber Lines etc. In this paper involves the implementation of a area efficient 8-point, 16-point, 32-point, 64-point and 128-point single path delay feedback (SDF) and folding technique using radix-2 DIT FFT algorithm. The proposed algorithm are used in radix-2 butterfly in all stage. The proposed algorithm is area efficient and consumed delay in previous algorithm. The all design are implementation vertex-2p device family Xilinx software.

**KEYWORDS:** FFT, Folding Technique, Single Path Delay Feedback (SDF), Serial in Serial out Shift Register

### I. INTRODUCTION

The Fourier Transform is an inevitable approach in signal processing, particularly for applications in Orthogonal Frequency Division Multiplexing (OFDM) systems [1]. The Discrete Fourier Transform decomposes a set of values into different components of frequency. The Fast Fourier transform (FFT) is an appropriate technique to do manipulation of DFT. The algorithm of FFT was devised by Cooley and Tukey in order to decrease the amount of complexity with respect to time and computations [2].

The hardware of FFT can be implemented by two types of classifications- memory architecture and pipeline architecture. The memory architecture, comprises a single processing element and various units of memory [3]. The merits of memory architecture include low power and low cost when compared to that of other styles. The specific demerits are greater latency and lower throughput. The above demerits of the memory architecture are totally eliminated by pipeline architecture at the expense of extra hardware in an acceptable way. The various types of pipeline architecture include Single delay feedback (SDF), Single delay commutator (SDC) and multiple delay commutator (MDC). The pipeline architecture is a regular structure which can be adopted by using hardware description language in an easy manner. In the recent years, the communication systems need to transmit voice and video signals of high quality in an efficient manner. In present day the efficient module is a high speed, reliable technology of communication [4].

Orthogonal Frequency Division Multiplexing (OFDM) is such a reliable option to accomplish the above requirement. The algorithms of FFT can be grouped into fixed-radix, mixed-radix and split radix algorithms in a rough manner [5]. The basic categories of algorithms of FFT include - Decimation in-frequency (DIF) and the Decimation-in-time (DIT) as shown in Figure 1. Both of these algorithms depend on disintegration of transformation of an N-point sequence into many subsequences in a successive manner. There is no major difference between them as far as complexity of

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computation is concerned. Generally DIT deals with the input and output in reverse sequence and normal sequence respectively, while DIF deals with input and output in normal sequence and reverse sequence respectively. Only Decimation-in-frequency (DIF) algorithm will be taken into consideration.

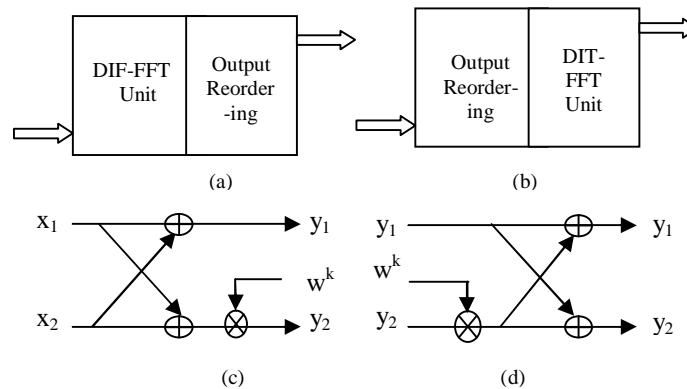


Figure 1: (a) DIF FFT processing (b) DIT FFT processing (c) DIF FFT butterfly (d) DIT FFT butterfly

## II. FAST FOURIER TRANSFORM

There are two types with respect to FFT algorithm devised by Cooley and Tukey - Decimation-in-Time algorithm (DIT) and Decimation-in-Frequency algorithm (DIF). The computation of a sequence of N-point can be obtained by means of a dual approach. The input sequence  $x(n)$  of size 'N' is decomposed into samples of odd and even and the corresponding sub-sequences  $f_1(n)$  and  $f_2(n)$  are given by:

$$f_1(n) = x(2n) \tag{1}$$

$$f_2(n) = x(2n + 1), n = 0, 1, \dots, \frac{N}{2} - 1 \tag{2}$$

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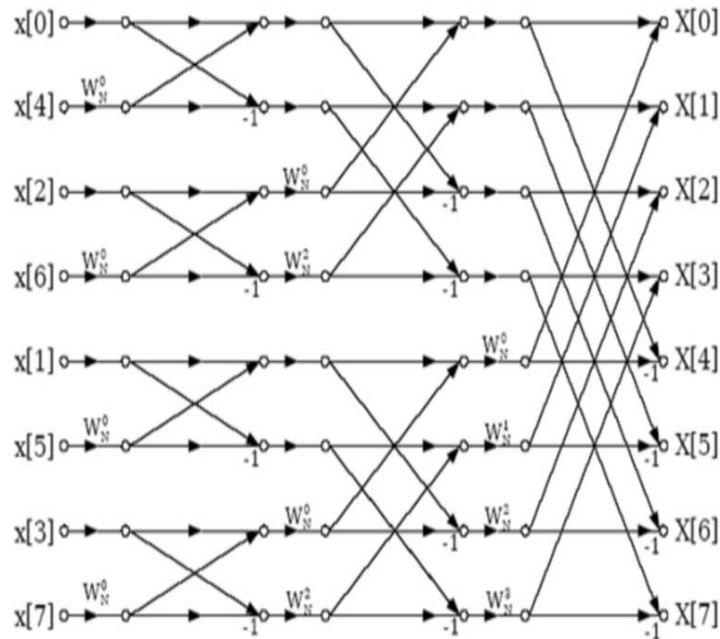


Figure 2: Butterfly of Radix-2 DIT FFT Algorithm

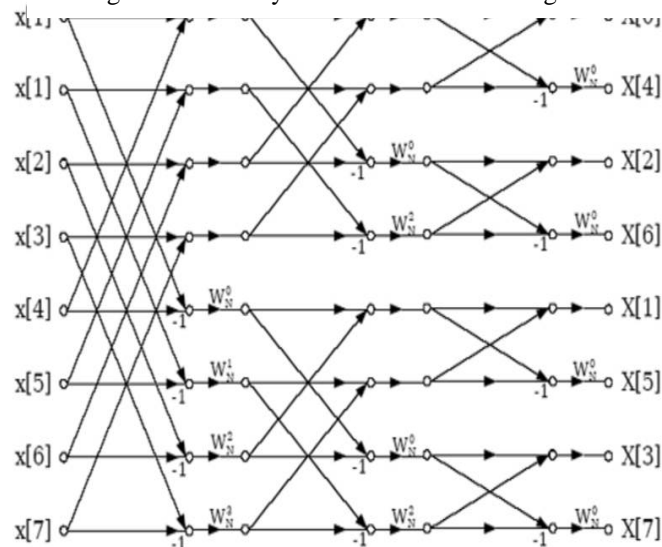


Figure 3: Butterfly of Radix-2 DIF FFT Algorithm

In figure 2, show the butterfly of radix-2 DIT FFT algorithm. In this figure we used eight inputs and eight outputs. In case of DIT the input sample is used bit reversal order while the output of DIT FFT coefficients is generated in natural order. In Figure 3, show the butterfly of radix-2 DIF FFT algorithm. In case of DIF the input sample is used in natural order while the output of DIF FFT coefficient is generated in bit reversed order.

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### III. PROPOSED METHODOLOGY

In proposed method are used in binary input is going to the serial input serial output (SISO) shift register as shown in Figure 4. In proposing algorithm consist of SISO, different types of multiplier, Kogge stone (KS) adder, subtractor, single path delay feedback (SPD) pipeline and folding architecture.

SISO: - SISO technique depends on the binary input. Suppose the binary input of the system is 8 word length, then eight delay flip flops are used in SISO register.

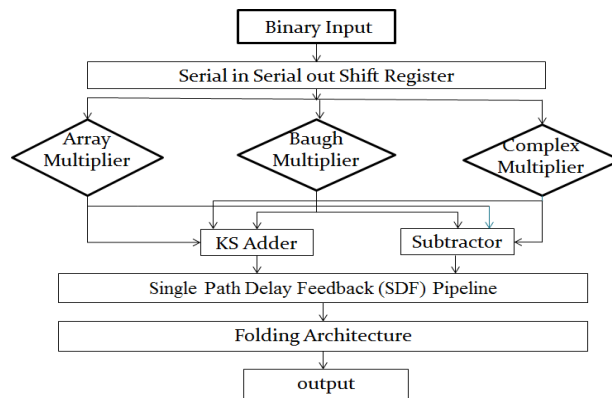


Figure 4: Flow Chart of Proposed Algorithm

Different types of Multiplier:- there are three types of multiplier are used in proposed algorithm, i.e. array multiplier, sign (Baugh) multiplier and complex multiplier. Another name of array multiplier is binary unsigned multiplied.

The Baugh - Wooley algorithm for the signed binary multiplication is based on the concept shown in figure 5. The algorithm specifies that all possible AND terms are created white cell and all possible NAND terms are created gray cell. The white cell consists of full adder and AND gate, but the gray cell consists of full adder and NAND gate.

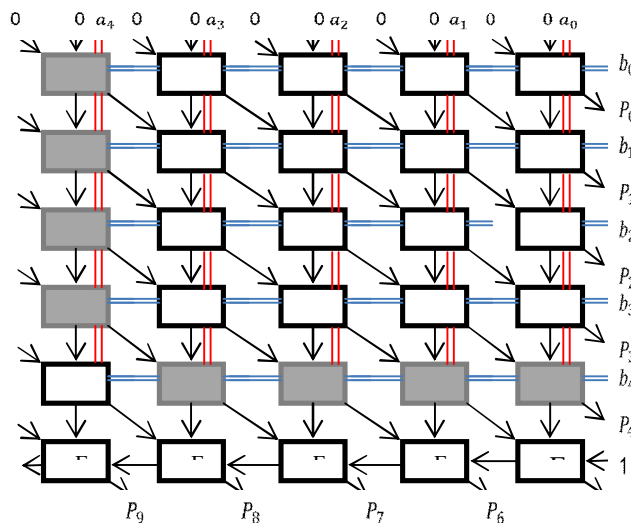


Figure 5: Block Diagram of Sign Multiplier

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Complex multiplication is consisting of 4 multiplications, 2 adders and 1 subtraction. But in the proposed complex multiplication is consisting of 3 multiplications, 1 adder and 1 subtraction in shown in figure 6.

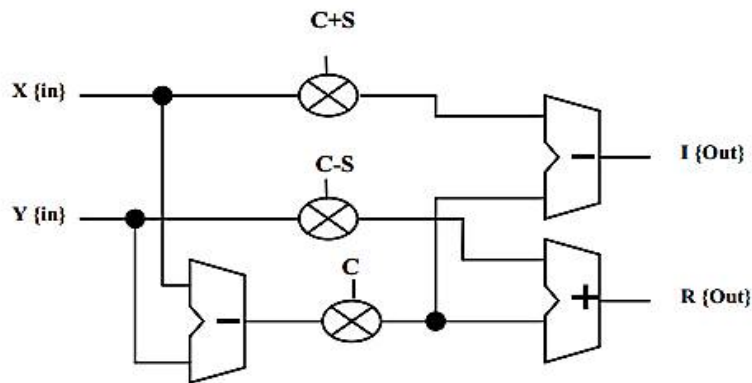


Figure 6: Block Diagram of Complex Multiplication

Subtractor:- Subtractor is consist of half subtractor and full subtractor depends on word length in proposed algorithm.

KS adder:- Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay. Area and propagation delay can be reduced by the aid of proposed kogge stone (KS) adder. This adder will be designed like as ripple carry adder. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay.

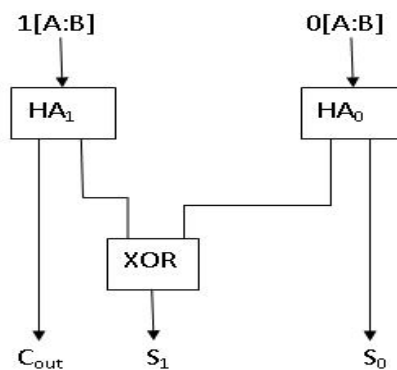


Figure 7: A Proposed 2 bit KS Adder

Single-path Delay Feedback Pipeline Architecture:- Herbert L. Groginsky and George A. Works introduced a feedback mechanism in order to minimize the number of delay elements. In the proposed architecture one half of outputs from each stage are fed back to the input data buffer when the input data are directly sent to the butterfly.

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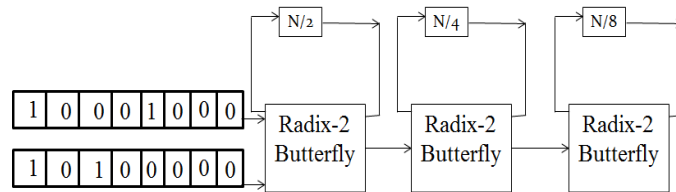


Figure 8: Flow Graph of the Radix-2 SDF Pipeline Architecture

Folding Architecture:- Folding is a transformation technique using in DSP architecture, implementation for minimizing the number of functional blocks in synthesizing DSP architecture. Folding was first developed by Keshab K. Parhi and his students in 1992.

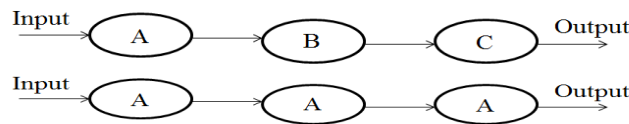


Figure 9: (a) Without folding technique (b) With folding technique

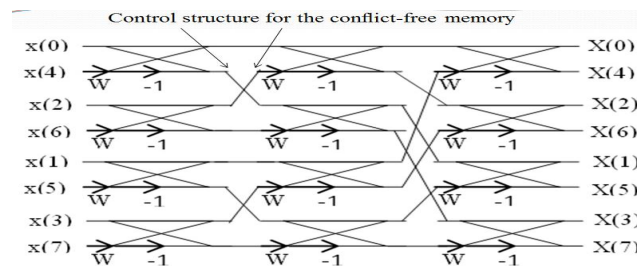


Figure 10: Proposed DIT Radix-2 FFT algorithm using Radix-2 Butterfly

The simulation results for various FFT algorithms have been tested practically by implementing in the Vertex-2p Xilinx software. Also these software outputs can be verified with simulation results obtained using MODELSIM. Some of the snapshots of results in the Xilinx software and simulation are as follows

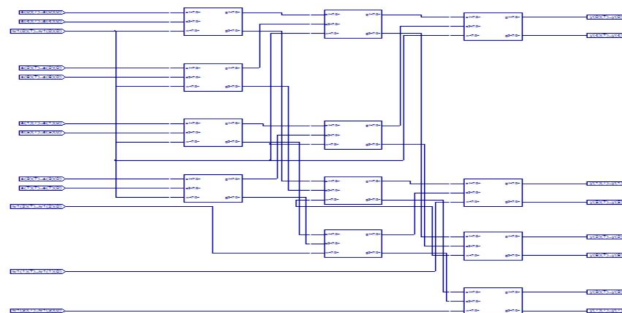


Figure 11: RTL view of proposed DIT Radix-2 FFT algorithm

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Table I: Show the result for proposed algorithm in array multiplier with Vertex-2p device family

Design	N	Number of slices	Number of 4 input LUTs	MCPD (nsec)
Proposed structure	8	97	192	15.598
	16	260	512	19.260
	32	656	1280	22.806
	64	1564	3072	26.319
	128	3141	6152	31.453

Table II: Result for complex number

Radix-2 DIT Algorithm for N=8 and N=16			
Parameter	Number of Slice	Number of LUTs	MCPD (nsec)
N=8	438	864	24.948
N=16	1168	2304	30.687

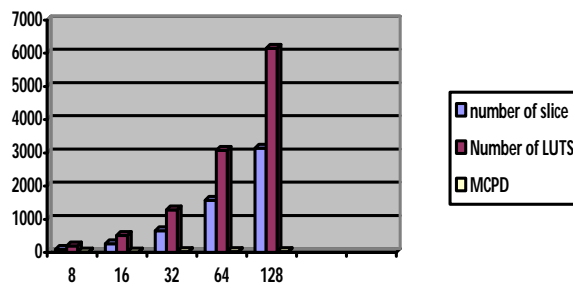


Figure 12: Bar graph of the array multiplier

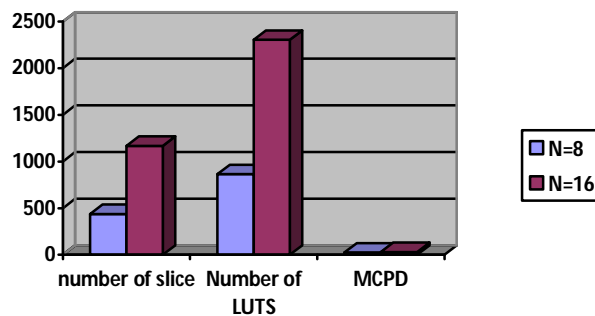


Figure 13: Bar graph of the complex multiplier

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## V. CONCLUSION

The Fast Fourier transformation (FFT) is a frequently used Digital signal processing (DSP) algorithms for the applications of Orthogonal Frequency Division multiplexing (OFDM). The combination of Orthogonal Frequency Division Multiplexing (OFDM) with Multiple Input Multiple Output (MIMO) signal processing is a definite approach of enhancing the data rates of various communication systems such as Wireless LAN, e Mobile, 4G etc. Since FFT processor is a complex module in OFDM, it is highly inevitable to design the processor in an efficient way. This research work involved the implementation of a low delay and area efficient 128-point pipelined FFT processor using radix-2 algorithm. The proposed algorithm is about 14- 15% consumed de in existing algorithm.

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