

18<sup>th</sup> September 2020

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# A Novel SRAM Array Design with Improved Delay

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**ABSTRACT:** The present semiconductor industry is developing quite quickly. Mobile and portable devices are becoming small for each day and moreover there is a rising demand for extended battery power. With these requirements, the leakage power in stand-by mode becomes a critical concern for researchers. In most of these devices, memory is an integral part and its size also scales down as the device size is reduced. Static random access memory power and speed dissipation are the significant factor in most of the electronic applications, which prompts numerous plans with the power utilization of limiting the power during the hold, write, and read processes. In this work, A novel SRAM array design with improved delay is presented. An array of 16x16 SRAM array structure is designed using SRAM, sense amplifier, row and column decoder will be designed. This design is able to diminish the leakage power dissipation. To determine schematic solutions and to analyze power dissipation, delay and PDP (power delay product) Tanner EDA (Electronic Design Automation) tool is used. The design models and the results can be analyzed with the use of industrial standard library files. Presented SRAM array performance can be compared with other earlier SRAM arrays in terms of dissipation of power, PDP and delay.

**KEYWORDS:** Static Random Access Memory (SRAM), Tanner EDA, Power Delay Product (PDP)

## I. INTRODUCTION

The present mechanically associated world creates various measure of information and the innovation engaged with regular application is essential to process and preserve this colossal measure of information. Memory happens to be a necessary piece of every electronic gadget for putting away guidelines or information created by calculation. SRAM cell is one of the mostly used memories.

Static random-access memory is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.

SRAM cell is a high-speed memory cell that is used for high speed applications like buffers and caches. The reason SRAM is used in this application is that it is faster than DRAM which is also used as a memory cell but it is constituted of capacitors while the other hand SRAM is constituted of transistors. The low power and high throughput issues are becoming increasingly important in Very large-scale integration (VLSI) system, microprocessor, and Static Random Access Memory (SRAM) designs for Artificial Intelligent (AI) application, such as in autonomous vehicles and Internet of Things.

The SRAM is utilized as reserve memory in super PCs and workstations due to low power and fast activity. The leakage current involves a rate which is more than 40 % of vitality utilization in the superior IC's. SRAM cluster in SOC (System On Chip) adds to a large portion of spillage and also subsequently planning a low leakage and low power expending memory square is attractive. Moreover, the solidness of the memory cell for composing and perusing the bit put away is of convey and with diminished inventory voltage supply, the defer increments. Consequently, a fair strategy should be utilized to diminish leakage power, power utilization and increment stability of the cell.

The need for low power/energy consumption of the integrated ICs, is increasing rigidly through the success of wearable and portable electronic components as well as the omnipresent implementation of sensor networks in wireless

18<sup>th</sup> September 2020

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communication. The supply voltage of the integrated circuits has been reduced in the near/sub-threshold values if the frequency is not a major issue in order to decrease the energy/ power consumption of these circuits. The embedded chips include essential elements which make a major contribution to overall power/energy use in the static random access memory devices.

Nonetheless, owing to the severe damage in the noise margin with static read and the capacity with write enable, in addition to the rigorous impacts of the leakage current with read bitline, a regular six transistor. The most normally utilized 6T SRAM cell has the detriment of keeping up essential Read Noise Margin (RNM) and Write Noise Margin (WNM) as the innovation is downsized. To conquer this, SRAM cells with 7T, 8T and 9T were built to cast and accomplish preferable outcomes over the regular 6T cell.

In general, charge-based memories suffer from performance degradation with the down scaling reaching deep nanoscale (10-nm node and beyond). This problem affects the reliability, endurance, and the noise margin of SRAM memory. With the use of lower technology nodes, the size of a memory cell is also reduced. This leads to increases in the leakage current component of memory cells. Various components that contribute to leakage in SRAM cells are the junction leakage current, gate leakage current and sub-threshold leakage current. However, in lower technologies, sub-threshold leakage is dominant. Various techniques for leakage power reduction and improvement in cell stability have been proposed by various researchers. Multi-threshold CMOS (MTCMOS) is one of the prominent techniques to minimize leakage power.

Shorten in static current causes the lessening in leakage power dispersal. To shun the information maintenance exhaustingness, most extreme voltage is provided to the circuit during the dynamic mode and limited voltage is supplied during the backup mode. There are many techniques for originating memory cell with low power and delay. The SRAM cell uses self-controllable voltage level-upper (SVL-U) method and transmission gate logic with the condensation in dynamic power.

In this work a novel SRAM array design with improved delay is presented. The rest of the paper is organized as follows: section II describes the related work. The section III demonstrates presented SRAM design. The section IV demonstrates the result analysis of presented design and finally the work is concluded in section V.

## II. LITERATURE SURVEY

Pulla Reddy A, G Sreenivasulu, R Veerabhadra Chary et. al., [1] presents Write and Read Assist Techniques for SRAM Memories in Nanometer Technology. Along with improving the write-ability of the SRAM cell the write assist techniques will impact the performance, power and area of the chip. At lower voltages the noise margin is very crucial for the SRAM cell stability. Read assist techniques help in improving the cell stability and these techniques analyzed across the process, voltage and temperature range. These read assist techniques not only helps the readability and stability of SRAM bit cells but they also will impact the performance, power and area of the chip.

Amit Namdev, Paresh Rawat et. al., [2] presents A Comparison of n-T SRAM Cell in Nanometre Regime. In this paper we have simulated and analyzed the performance of various topologies of SRAM cells at 65nm and 45nm technology for parameters like cell power consumption, delay and SNM. In this paper authors have compared 4T, 6T, 7T, 8T and 9T SRAM cell at 65nm and 45nm technology by using HSPICE simulator and analyse in terms Power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.

Kowsalya.M, Dr.H.Mangalam et. al., [3] presents Performance Evaluation and Stability Analysis of SRAM Cells. This paper compares the performance of various SRAM cell topologies, which include the conventional 6T-cell, 7T-cell, 8T-cell, 9T-cell and the 10T-cell implementations. Even though 9T and 10T cell implementation result in a reported 13% and 30% area increase, respectively, these two topologies allow for better cell stability due to their read-disturb-free operation, which is beneficial as process technologies continue to scale down.

Dr. V. Rukkumani, Dr. M. Saravana kumar and Dr. K. Srinivasan et. al., [4] presents a Design and Analysis of SRAM Cells for Power Reduction Using Low Power Techniques In this work, instead of conventional circuit, 8 transistor (8T) and ten transistor(10T) designs are tried to improve the power efficiency under various temperature conditions. Initially



18<sup>th</sup> September 2020

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8T and 10T SRAM circuits are designed with write driver logic and the power is calculated for both static and dynamic conditions. Then, charge recycling logic is tried along with precharge logic with various temperature ranges.

J. Ramesh, P. Brundavani et. al., [5] presents a Design of Power Efficient High Performance SRAM Cell using Transmission Gates (TG). A TG primarily based 10T SRAM exploitation voltage swing cell at 0.09 um feature size in CMOS is planned to accomplish low power memory operation. This project compares proposed TG-VS SRAM cell with existing SRAM cells in terms of power and delay with different temperature. To implement proposed TG-SRAM cell in Tanner EDA (Electronic Design Automation) tool with 90nm CMOS environment is used.

Vema Vishnu Priya, G. Ramesh et. al., [6] presents a Design of 7T SRAM Cell Using Self-Controllable Voltage Level Circuit to Achieve Low Power In this project first, a low power 7T SRAM Cell is designed and later it is build with "Self-controllable Voltage level" circuit for maintaining low power consumption and high performance. A Self-Controllable Voltage Level (SVL) Circuit can supply a maximum dc voltage when the load circuits are in active mode or it can also decrease the dc voltage supplied to a load circuit which is said to be in standby mode. This SVL circuit can reduce standby leakage power of CMOS logic circuits drastically with minimum chip size and speed by considering 7T as load circuit.

Dr. A. Senthil Kumar, I.Manju, S.Sumathi, C.Preethi et. al., [7] suggests Read/Write Stability Improvement of 8T SRAM Cell Using Schmitt Trigger. The stability of read and write operations can be increased using Schmitt trigger based SRAM bit cells. In this paper the Schmitt trigger design is implemented in 8 transistor SRAM cell to increase read-stability and write-ability than the conventional 6T cell. The design is implemented in Tanner EDA tool and the results are observed.

C. Ramya Shruthi, S.Rambabu et. al., [8] implements an Efficient SRAM for Ultra-Low Voltage Application Based on ST for Better Read Stability and Write Ability. They analyze Schmitt-Trigger (ST)-based differential-sensing static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell.

Anie Jain, Shyam Akashe et. al., [9] suggests Optimization of low power 7T SRAM cell in 45nm Technology. In this paper a low power SRAM cell is proposed. In the proposed SRAM topology, additional circuitry has been added to a standard 6T-SRAM cell to improve the performance. A seven transistor (7T) cell at a 45nm feature size in CMOS is proposed to accomplish improvements in stability, power dissipation and performance compared with previous designs for low-power memory operation. The impact of process variations is investigated in detail, and the CADENCE simulation shows that the 7T SRAM cell has an excellent tolerance to process variations.

A. Islam; M. Hasan et. al., [10] presents Leakage Characterization of 10T SRAM Cell. This paper presents a technique for designing a low-power and variability-aware SRAM cell. The cell achieves low power dissipation due to its series-connected tail transistor and read buffers, which offer a stacking effect. This paper studies the impact of process, voltage, and temperature (PVT) variations on most of the design metrics of the SRAM cell and compares the results with standard 6T, 9T, and ST10T (Schmitt trigger based) SRAM cells.

### III. SRAM ARRAY DESIGN WITH IMPROVED DELAY

In this work, a novel SRAM array design with improved delay is presented. This SRAM is designed to reduce the leakage power and it has very low power dissipation and power delay product. With the help of presented SRAM, a 16 x 16 SRAM memory array will be implemented for modern cache memories.

The sense amplifier is in charge of detecting what value is stored in an SRAM cell during a read cycle and displaying that value at the output. Since only one row of data is accessed during each read cycle, each column of cells within the SRAM array requires only one sense amplifier. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly. Due to their small size, the memory cells are weak and hence cannot discharge the bit lines fast.

Address Decoder is an important digital block in SRAM which takes up to half of the total chip access time and significant part of the total SRAM power in normal read/write cycle. The memory address decoder is divided into two parts, column and row decoder. The row decoder should choose the comparing word line of the ideal memory cell. The column decoder should choose the relating bit line of the ideal memory cell design.

In the circuit design, two PMOS transistors and two NMOS transistors are announced in both pull up networks and pull down networks. The presented PMOS7 and NMOS5 transistors act like footer and header, while the NMOS6 and PMOS8 transistors are utilized to keep up rationale state during rest mode.

During sleep mode, PMOS7 and NMOS5 transistors can be switching OFF and one of the transistors in corresponding to the sleep transistors and thus holds the preceding information. In between supply and ground, the number of transistor series connection is increases means the leakage current getting decreases since the resistivity range is very high. The output of PMOS1 and PMOS2 is connected as input to NMOS1 and NMOS2 respectively and the output of NMOS1 and NMOS2 is connected as an input to PMOS1 and PMOS2 respectively.

If the leakage current is decreases then automatically static power is also decreased. In the existing techniques, the same approach is applied but those techniques based SRAM cells occupies more area than the projected one.

The SRAM array entails of SRAM cell, row and column decoder, sense amplifier. The 16 x 16 memory array is designed using presented memory cell with appropriate analysis. The presented SRAM cell memory array contains decoder and sense amplifier. The sense speaker is utilized to detect the contrast between two information signs of memory cell design.

A memory array is designed using this presented SRAM cell. The proposed 16 bit SRAM memory array output response analysis is discussed in the below section.

#### IV. RESULT ANALYSIS

This section demonstrates the result analysis of presented SRAM array. The SRAM array is implemented using Tanner EDA tool. Sense amplifiers plays a major role in the memory array where the inputs for a row decoder are In1 = 0, In2 = 0, In3 = 0, In4 = 0 and for column decoder the inputs are In5 = 0, In6 = 0 In7 = 1, In8 = 0

The static power equation is given as

$$P_{static} = I_{leakage} * V_{dd} \quad (1)$$

$$Current = \frac{q}{t} \quad (2)$$

$$Current = \frac{cv}{t} \quad (3)$$

$$t = \frac{cv}{I} \quad (4)$$

$$t = cV_{dd} / K(V_{dd} - V_T) \quad (5)$$

The dynamic power dissipation equation is given as

$$P_{dynamic} = \alpha CV_{dd} V_{swing} f \quad (6)$$

Where  $\alpha$  is activity factor,  $V_{swing}$  is voltage swiipe at output knob, c is capacitance f is frequency and Vdd is supply voltage.

The delay speaks to the propagation delay, is characterized as the normal between low-to-high progress delay ( $t_{plh}$ ) and high-to-low change delay ( $t_{phl}$ ) and it is expressed as

$$t_{pd} = \frac{t_{plh} + t_{phl}}{2} \quad (7)$$

Where,  $t_{plh}$  and  $t_{phl}$  is considered from the reproduction graph of writing activity. For instance, the  $t_{phl}$  is dictated when change between high input voltage to low yield voltage transformation and moreover  $t_{plh}$  is determined when distinction between low information voltages and high yield voltage progress. At long last, the delay is determined by the normal of  $t_{plh}$  and  $t_{phl}$ .



18<sup>th</sup> September 2020

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The table 1 represents the power dissipation of presented SRAM array and conventional 6T SRAM array.

**Table 1: POWER DISSIPATION COMPARISON**

Different SRAM arrays	Power dissipation (mW)for 1v	Power dissipation (mW) for 2v	Power dissipation (mW)for 3v
Conventional SRAM	350.8	723.4	967.4
Presented SRAM array	0.024	0.033	0.42

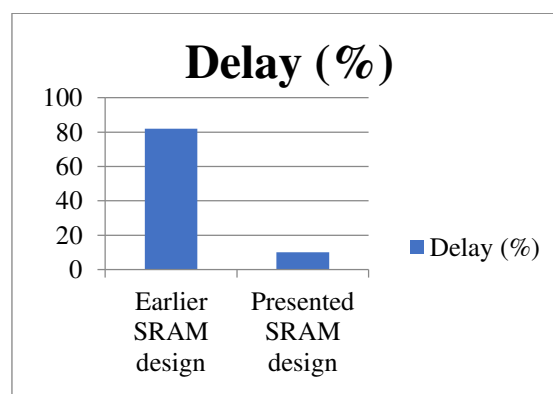
From table 1 it is clear that presented SRAM array has very less power dissipation than earlier SRAM arrays.

The table 2 represents the delay and power delay product of presented SRAM array and earlier SRAM array.

**Table 2: Delay and POWER DELAY PRODUCT COMAPRISON FOR PRESENTED AND EARLIER SRAM ARRAYS**

Different SRAM Array designs	Delay in nanoseconds(ns)	Power delay product in Joule
Earlier SRAM	0.00671	$6.74 \times 10^{-3}$
Presented SRAM array	0.0087	$3.2 \times 10^{-9}$

Therefore presented SRAM has less delay and less PDP compared to earlier SRAM designs. The Fig. 1 shows the delay comparison between presented SRAM design and earlier SRAM design.



**Fig. 1: DELAY COMAPRISON GRAPH**

Hence presented has less delay, low dissipation of power and less PDP than other earlier SRAM designs.

## V. CONCLUSION

In this work, a novel SRAM array design with improved delay is presented. This SRAM design is implemented using Tanner EDA tool. This SRAM array is available for higher read stability and less unique power usage. Firstly an SRAM cell is presented. with the help of this cell a 16x16 SRAM array memory is designed that contains sense





18<sup>th</sup> September 2020

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amplifier and a row and column decoder, During the write operation, this SRAM cell utilizes charging or releasing of bit line, thereby the dynamic power usage is reduced than earlier SRAM designs. The performance of the presented SRAM cell is measured in terms of power dissipation, delay and Power delay product. The performance of the presented SRAM design is compared with earlier SRAM designs. From the results it is clear that presented SRAM design has less delay, less power dissipation and low PDP than earlier SRAM designs.

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