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Optimization Analysis of 2-D DWT using Reversible Logic and Multiplier-less NEDA Technique

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ABSTRACT: Curtail the circuit complexity and improve the performance are proposed; Discrete Wavelet Transform is applied for the stationary and non-stationary signal, it is used to speech signal, audio and video signal etc. Distributed arithmetic (DA) is a general and effective technique to implement multiplierless filters and has been exploited in the past to implement the discrete wavelet transform as well. It's found that DA requires ROM and size of ROM increases exponentially as the increase in number of inputs, which highly increases the circuit complexity. Proposed techniques is based on high speed area efficient 2-D discrete wavelet transform (DWT) using 9/7 filter based new efficient Distributed Arithmetic (NEDA) Technique and kogge stone adder. NEDA technique is applied to low and high pass filter of the discrete wavelet transform. This technique consists of adder, shift register and free of multiplier. Design and result are implemented in Xilinx software and verified resistor transfer level (RTL) and waveform.

KEYWORDS: 2-D Discrete Wavelet Transform (DWT), MDA, Low Filter Bank, High Filter Bank, Xilinx Simulation.

I. INTRODUCTION

The Wavelet transform holds each time and frequency facts, based on a multi-resolution analysis framework while as compared to conventional transforms such as the fast Fourier Transform (FFT) and the Discrete Cosine Transform (DCT) [1]. Wavelet Transform has been used in many fields, which include photo and sign processing, sign compression, inter-stellar information evaluation, virtual fingerprints, noise reduction and so on. However, there has been an extended distance among the expectancy and the realism, due to its tough, tedious computation manner, and the computation speed.

The SRAM-based FPGA is better acceptable for mathematics, which include multiply & collect (MAC) in depth DSP capabilities and it could avoid the development charges and the lack of ability to make layout changes even after manufacturing [2].

The DWT is computationally in depth and most of its utility demand actual-time processing. One manner of reaching high pace overall performance is to apply speedy computational algorithm in a popular motive computers [3]. Another way is to make the most the parallelism inherent inside the computation for concurrent processing with the aid of a set of parallel processor.

But, it is not cost effective to use a general purpose computer for a specific application. Also, general purpose computer used for their implementation required more space, large power and more computation time. With the development of very large scale integration (VLSI) technology it facilitates to digital signal processing (DSP) system designer to design a high performance, low cost and low power system in a single chip [4]. The characteristic of VLSI system are that they offer greater potential for large amount of concurrency and offer an enormous amount of computing power within a small area. The computation is very cheap as the hardware is not an obstacle for VLSI system [5]. But, the non-



localized global communication is not only expensive but demands high power dissipation. Thus, a high degree of parallelism and a nearest neighbor communication are crucial for realization of high performance VLSI system [6]. Keeping this in view, excessive performance utility specific VLSI structures are hastily evolving in recent years. The special purpose VLSI systems maximize processing concurrency by parallel / pipeline processing and provides cost effective alternative for real- time application. Consequently, 2-D DWT is currently carried out in a VLSI system to meet the temporal requirement of real-time application. Maintaining this reality in view, numerous layout schemes have been cautioned within the final decades for efficient implementation of 2-D DWT in a VLSI system. Researchers have adopted different algorithm formulation, mapping scheme, and architectural design methods to reduce the computational time, arithmetic complexity or memory complexity of 2-D DWT structures. However, the area-delay performance of the existing structures changes marginally. The JPEG2000 preferred [4-6] defines the discrete wavelet transform (DWT) as a linear area-to-frequency remodel of the picture domain in an irreversible compression. This irreversible discrete wavelet transform is applied with the aid of a DA factorized coefficients from 9/7 Daubechies coefficients.

II. MULTILEVEL DISCRETE WAVELET TRANSFORM

Multiresolution analysis (MRA) is a characteristic feature of sub-band and it is used for better spectral representation of the signal. In MRA, the signal is decomposed for more than one DWT level known as multilevel DWT. It means the low-pass output of first DWT level is further decomposed in a similar manner in order to get the second level of DWT decomposition and the process is repeated for higher DWT levels [7]. Some algorithms have been suggested for computation of multilevel DWT. One of the most important algorithm are pyramid algorithm (PA), this algorithm are proposed Mallet for parallel computation of multilevel DWT. PA for 1-D DWT is given by

$$Y_l^j(n) = \sum_{i=0}^{k-1} h(i)Y_l^{j-1}(2n-i) \quad (1)$$

$$Y_h^j(n) = \sum_{i=0}^{k-1} g(i)Y_h^{j-1}(2n-i) \quad (2)$$

Where $Y_l^j(n)$ is the n^{th} low-pass sub band component of the j^{th} DWT level and $Y_h^j(n)$ is the n^{th} high-pass sub band component of the j^{th} DWT level. Two-dimensional signal, such as images, are analyzed using the 2-D DWT as shown in Figure 1. Currently 2-D DWT is applied in many image processing applications such as image compression and reconstruction [8]. The 2-D DWT is a mathematical technique that disintegrates an input image in the multi-resolution frequency space [9]. The 2-D DWT disintegrate an enter photo into four sub bands called low-low (LL), low-excessive (LH), high-low (HL) and high-excessive (HH) sub band.

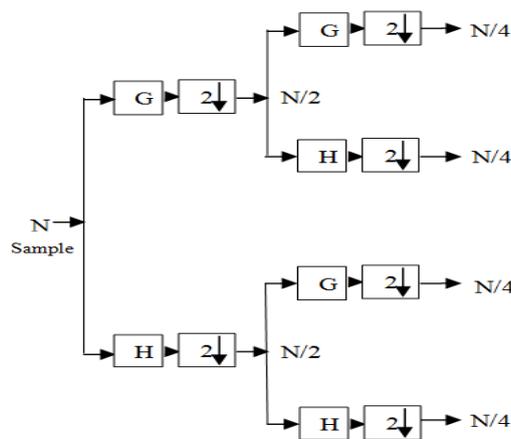


Figure 1: Two Level Diagram of Discrete Wavelet Transform



III. PROPOSED ARCHITECTURE

The block diagram of 9/7 wavelet coefficient based multilevel discrete wavelet transform using MDA structure shown in Figure 2. In this, input sample passing through 8-bit register after that all symmetrical delay input is add in the equation 3 to equation 6.

$$m(1) = X(n) + X(n - 8) \tag{3}$$

$$m(2) = X(n - 1) + X(n - 7) \tag{4}$$

$$m(3) = X(n - 2) + X(n - 6) \tag{5}$$

$$m(4) = X(n - 3) + X(n - 5) \tag{6}$$

$$m(5) = X(n - 4) \tag{7}$$

In 9/7 filter, NEDA used to remove multipliers and apply NEDA twice to get the 1-D 9/7 filter high pass output Y_{H1} and low pass output Y_{L1} .

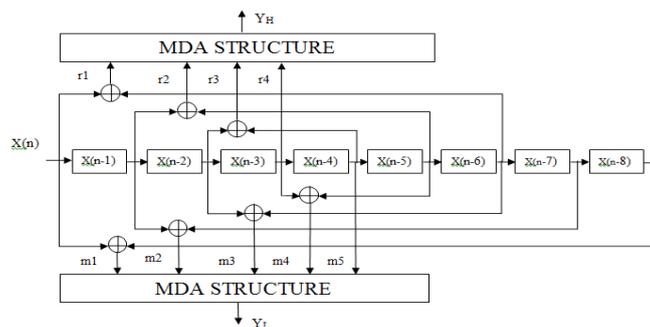


Figure 2: Block Diagram of 9/7 Wavelet Coefficient based Discrete Wavelet Transform

In above fig. h_0, h_1, h_2, h_3, h_4 are the Low pass filter coefficients and g_0, g_1, g_2 and g_3 are High pass filter coefficient. Both low pass and high pass filter bank are used to g_0, g_1, g_2 and g_3 applied NEDA technique by r_1, r_2, r_3 and r_4 to get product high pass output Y_H of the 9/7 filter after selecting the low pass coefficient h_0, h_1, h_2, h_3 , and h_4 applied NEDA technique by m_1, m_2, m_3, m_4 and m_5 then the low pass output Y_L of the 9/7 filter.

Example: low pass output step by step as-

$$Y_L = \begin{bmatrix} h_0 & h_1 & h_2 & h_3 & h_4 \end{bmatrix} \begin{bmatrix} m_1 \\ m_2 \\ m_3 \\ m_4 \\ m_5 \end{bmatrix} \tag{8}$$

Let $m_1 = 1, m_2 = 2, m_3 = 3, m_4 = 4$ and $m_5 = 5$. Then multiplier row and column and find out the low pass output 122. Where h_0, h_1, h_2, h_3 and h_4 daubechies 9/7 filter coefficients are 0.6029490, 0.2668444, -0.782232, -0.0168641 and 0.02674875 respectively. All the daubechies 9/7 filter coefficients multiplied by 128 and get the 77, 34, -10, -2 and 3 respectively.



$$Y_H = [77 \ 34 \ -10 \ -2 \ 3] \cdot \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{bmatrix} = 122$$

(9)

After selecting the low pass coefficients h_0, h_1, h_2, h_3 and h_4 applied NEDA technique by m_1, m_2, m_3, m_4 and m_5 then the low pass output Y_L of the 9/7 filter are.

Design the DA matrix by way of the filter coefficients as low pass clear out based DA matrix-

$$[Y_k] = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} m_1 \\ m_2 \\ m_3 \\ m_4 \\ m_5 \end{bmatrix} = \begin{bmatrix} m_1+m_5 \\ m_2+m_3+m_4+m_5 \\ m_1+m_3+m_4 \\ m_1+m_4 \\ m_3+m_4 \\ m_2+m_3+m_4 \\ m_1+m_3+m_4 \\ m_3+m_4 \end{bmatrix}$$

(10)

Figure 3 shows the NEDA strategies analysis as –

Step-(1)

All of the input converts' binary number

$$m_1 = 001, m_2 = 010, m_3 = 011,$$

$$m_4 = 100, m_5 = 101$$

Step-(2)

All of the binary enter carried out to sign extension so,

$$s(1) = 0001, s(2) = 0010, s(3) = 0011,$$

$$s(4) = 0100, s(5) = 0101$$

Step-(3)

All of the sign extensions enter carried out to adder array so,

$$m(1) = 0110, m(2) = 1110, m(3) = 1000,$$

$$m(4) = 0101, m(5) = 0111,$$

$$m(6) = 1001, m(7) = 1000$$

$$m(8) = \text{not}(m_3 + m_4) + 1 = 1001$$

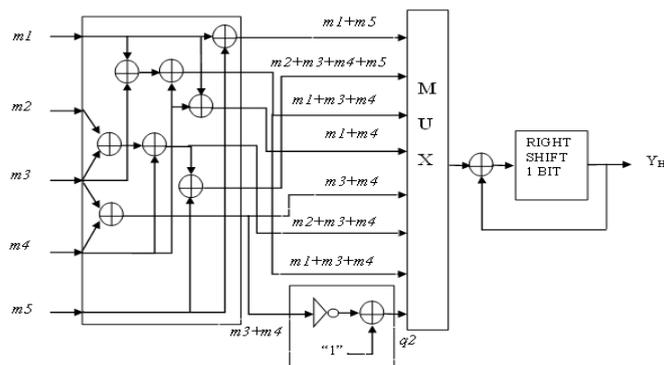


Figure 3: Proposed Architecture 1-D for Low Pass Filter Using NEDA Technique



Step-(4)

The entire adder array enter applied to MUX so, the whole adder array enter proper shift 1-bit so

$$\begin{aligned} \text{MUX}(1) &= 0^*0110 = Y_p(0) \\ \text{MUX}(1) \text{ add MUX}(2) &= Y_p(1) \\ &= 0^*0110 \\ &= 1110 \\ &+ 100010 \end{aligned}$$

Output of the $Y_p(1)$ again right shift 1-bit and adds MUX(3) so

$$\begin{aligned} &= 0^*100010 \\ &= 1000 \\ &+ 100010 \end{aligned}$$

Continuous the process one by one, after then calculate the final output

$$Y_p(7) = 00001111010 = 122$$

Carry is rejected.

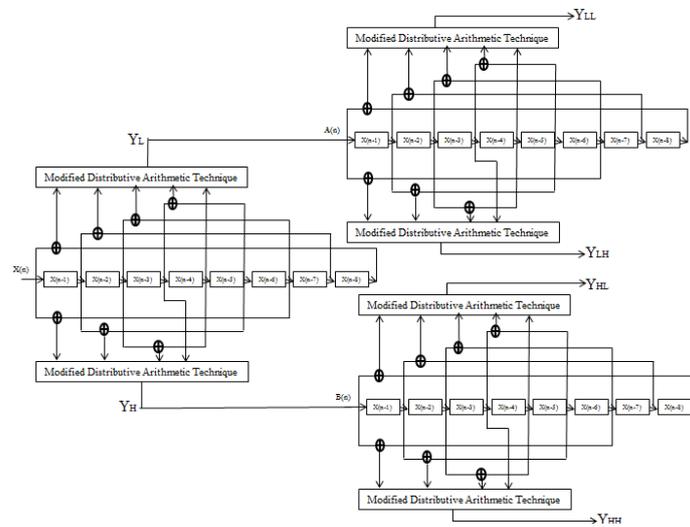


Figure 4: Proposed Architecture for 2-D DWT using NEDA Technique

Fig. 4 present the 2-D sub-band WT, the outputs of 1-D high pass and low pass filters Y_{H1} and Y_{L1} are passed through series of shift registers and then we take the samples parallel using parallel data access method. The parallel data access method is used to minimize the memory requirement in 2-D sub-band WT.

IV. SIMULATION RESULT

All of the designing and test concerning algorithm that referred to in this paper is being developed on Xilinx 14.1i up to date version. Xilinx 14.1i has couple of the striking functions inclusive of low reminiscence requirement, fast debugging, and occasional price. By means of the aid of that software program we debug the program without problems.

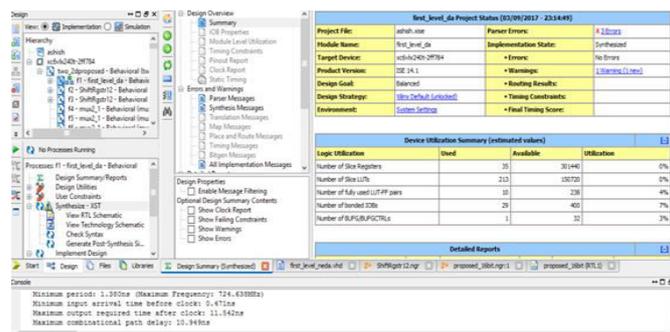


Figure 5: Synthesis Report of 1-D DWT using NEDA

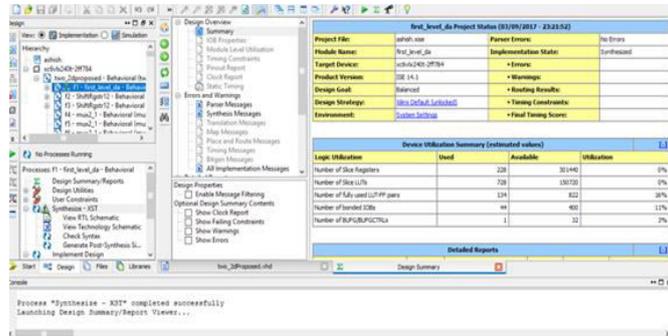


Figure 6: Synthesis Report of 2-D DWT using NEDA

Table 1: Comparison result of existing algorithm and proposed algorithm

Design	No. of Slice Registers	No. of Slice LUTs	LUT Flip Flop pair	Bonded IOBs	Maximum Frequency (MHz)
Mamatha I, Shikha [1]	139	417	71	358	633.43
Proposed Design	35	213	10	29	724.638

Comparison parameter of the past work and present work is shown in table 1, in this table some parameter are used. In previous line based and block based discrete wavelet transform are used but in proposed technology is multiplier-less i.e. modified distributive arithmetic algorithm.

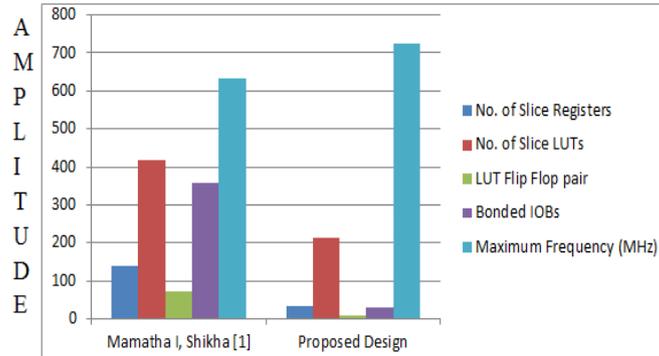


Figure 7: Shows the Bar Graph of the Previous Algorithm and Implemented Algorithm-I

V. CONCLUSION

The multilevel 2-D DWT is widely used in image compression and image coding for multimedia applications. Area-delay efficient hardware realization of the multilevel 2-D DWT has great practical interest for low-power resource constrained mobile and portable devices. In this thesis a multiplier-less VLSI architecture is proposed using new efficient distributed arithmetic algorithm named NEDA. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of ROM, multiplication, and subtraction. The proposed architecture using NEDA provides less delay and minimum number of slice compared the existing architecture. We demonstrate that NEDA is a very efficient architecture with adders as the main component and free of read only memory, multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary. So discrete wavelet transform using NEDA technique is provides the least amount of maximum combinational path delay compare to other design.

The proposed NEDA based DWT algorithm are consumed 48.92% number of slice Look up table (LUT), 32.5.0% number of full adder, 11.11% number of flip flop and 12.58% maximum combinational path delay.



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