



e-ISSN: 2319-8753 | p-ISSN: 2320-6710

# IJRSET

International Journal of Innovative Research in  
**SCIENCE | ENGINEERING | TECHNOLOGY**

# INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 11, Issue 7, July 2022

**ISSN** INTERNATIONAL  
STANDARD  
SERIAL  
NUMBER  
INDIA

Impact Factor: 8.118

# Study of Discrete Hartley Transform using Different Multiplier and Adder

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**ABSTRACT:** A discrete Hartley transform (DHT) algorithm can be efficiently implemented on a highly modular and parallel architecture having a regular structure is consisting of multiplier and adder. Discrete Hartley Transform (DHT) is one of the transform used for converting data in time domain into frequency domain using only real values. We have studied of DHT, urdhwa multiplier and Kogge stone adder (KSA). The studied of Urdhwa multiplier based on KSA as an improvement in place of simple multiplication used in conventional DHT. This paper survey of different DHT technique, describe mathematical calculation of DHT and explain the Xilinx software.

**KEYWORDS:** Discrete Hartley Transform (DHT), Urdhwa Multiplier, KSA, Xilinx Software

## I. INTRODUCTION

Discrete Hartley Transform is a Radix-2 algorithm and is especially useful in DSP applications such as image compression, signal compression, filter banks[1] signal representation and harmonic analysis, etc.[2]. The key goal behind the use of DHT is to reduce the complexity of VLSI hardware architecture [3]. While DHT computing has become an intensive hardware complexity, it is reduced. The explanation behind this is that the forward and inverse of DHT is absolutely the same except for the scaling factor. Or DHT is the opposite of its own. The same hardware will also be used for both forward and inverse measurements. In other terms, we can assume that the same numbers of adders, multipliers, etc. are used by both forward and inverse implementations. DHT is somewhat similar to the Discrete Fourier Transform (DFT) or DHT is derived from DFT. The DFT includes both actual and imaginary parts, while the DHT only has real parts.

The calculation of imaginary parts is negligible and therefore complex arithmetic is avoided. In other words, DHT is used as a replacement of DFT when the sequence is real [4] [5]. In other terms, we can assume that the same numbers of adders, multipliers, etc. are used by both forward and inverse implementations. DHT is somewhat similar to the Discrete Fourier Transform (DFT) or DHT is derived from DFT. The DFT includes both actual and imaginary parts, while the DHT only has real parts. There are also many spilt radix algorithms available for computing. These can be implemented with even low arithmetic cost [10]-[11]. The disadvantage with the classical spilt-radix algorithm is its irregular computational structure.

Delays in VLSI architecture are mainly introduced by multipliers, as they consume a large portion of the chip area. Hence, to implement multipliers, memory-based solutions are being taken into consideration. Implementation of multipliers with look-up table-based solutions, it is required that one operand should be constant [12]. It then becomes possible to store complete result in partial ROM.

## II. LITERATURE REVIEW

**Nikhil Advait Gudala et al. [1]**, one of the most significant areas of exploration in VLSI is the plan of force productive and rapid information way rationale frameworks. The speed of expansion is compelled in advanced adders when taken to engender a bring through the snake. Whenever the past piece has been added and the convey produced from this option is proliferated onto the following piece, the total for each piece in a rudimentary viper is created consecutively as such. In a few PC frameworks, the Carry Select Adder (CSLA) is utilized to relieve the issue of convey spread delay by creating various convey pieces and afterward

choosing a convey for the ideal result. The CSLA, in any case, isn't region proficient since it uses a few Ripple Carry Adders (RCA) sets to create incomplete aggregate and convey by thinking about convey information, and afterward multiplexers pick the last total and convey (mux). The center idea of this study is to utilize the Binary to Excess-1 Converter (BEC) to accomplish rapid and low-power utilization rather than the RCA in the normal CSLA. The outcomes have been examined and analyzed for execution of three adders (regular CSA, CSA with RCA, CSA with BEC). The outcomes from the presentation assessments of the adders are contrasted and one another. All the recreation is done in 45nm innovation. The postponement of CSA and CSA with RCA are same, yet the principle contrast is in decrease of region and power. Also when CSA(BEC) and CSA(RCA) are analyzed, the region has been decreased by around 18.67% and power has been diminished by 25.85%.

**Krishna Sravani Nandam et al. [2]**, the CSL (Carry Select) viper is among the best adders to perform satisfactory math activities for a long time. The design of the CSL snake is important to the point that it will in general diminish region, postponement and power use. The CSL snake structure is with the end goal that the region, deferral and power utilization will be additionally limited. It can differ between the surmised and definite methods of the activity. The CSL snake region, postponement and power are decreased with fast, fruitful entryway level changes. Multiplier is utilized as a fundamental part in computerized signal handling to perform number juggling activities. The double mode can give a multiplier a productive usage, where precision can change essentially during execution. To give a more modest region and defer involving a compelling proposed snake in the multiplier with precise mode and inexact mode. The Dynamic Accuracy Configurable Multiplier is utilized conversely, with their multiplier, surmised multiplier furnishes lower delay and higher power regarding charge of humbler precision. The boundaries with the best grade approach. Aside from precise Evaluation of the 32\_Bit multiplier can be mimicked and orchestrated with the assistance of the Square-Root (SQRT) CSL viper in XILINXISE. Utilizing 4:2 blowers, the boundary result demonstrates lower delay, higher power utilization and high velocity.

**Muteen Munawar et al. [3]**, as the computerized electronic frameworks are getting better with the progression in innovation step by step; there is a need to assemble quicker and more power-effective multipliers, which are the significant structure block in a large portion of the advanced handling frameworks. Dadda tree multiplier is one of the successful multipliers consuming low power and very quicker than different multipliers for example Vedic, Wallace and corner redix4 multiplier. In this paper, we have planned a Dadda tree multiplier with convey select snake followed by paired to abundance 1 converter which makes it a lot quicker and power productive. The outcomes for this multiplier are similarly better thinking about other existing multipliers.

**Maytham Allahi et al. [4]**, another convey select viper (CSLA) engineering is proposed with a lower region and a higher speed contrasted with past CSLAs. The proposed CSLA is a low-region and rapid plan using another add-one circuit that is utilized rather than the subsequent wave convey viper (RCA) with the information convey equivalent to one ( $C = 1$ ) inside each gathering of the fundamental CSLA. Also, to facilitate the add activity, another gathering structure is proposed rather than the essential square-root (SQRT) gathering as well as using a quicker RCA in each gathering. In spite of the way that the proposed CSLA has not accomplished the least power utilization among all current plans in light of the PDK 45nm standard cell library, however it has accomplished the most reduced region and postponement contrasted with past CSLAs. Execution results show that 8 to 33% region decrease and 12 to 44% speed improvement are accomplished in the proposed CSLA contrasted with past plans.

**N. M. Hossain et al. [5]**, various sorts of processors and other computerized circuits adders are generally broadly utilized. Low power and region proficient fast circuits are most significant region in the examination of VLSI plan. The convey select snake is one of the quick adders which has less region and decreased power utilization. In this paper, a 16-cycle convey select snake has been introduced utilizing altered XOR based full viper to diminish circuit intricacy, region and deferral. The adjusted full viper configuration requires just two XOR entryways and one multiplexer. The adjusted 16-bit convey select viper gives preferred outcome over customary convey select snake as for region, power utilization and postponement.

**Deepti Gautam et al. [6]**, new VLSI calculation for a DHT that can be effectively executed on an exceptionally secluded and equal VLSI engineering having a normal construction is introduced. The simultaneous execution of the DHT calculation can be accomplished by parting on a few equal parts proficiently. What's more, the equipment intricacy can be fundamentally decreased utilizing sub articulation sharing procedure of the proposed calculation in exceptionally equal VLSI execution. With productive sharing of multipliers having similar steady and utilizing the benefits of the proposed calculation, the quantities of multipliers and



adders utilized has been essentially diminished and is kept at least contrasted and that of the current calculations. Productive execution of multipliers with a consistent is conceivable in VLSI. Computerized picture handling is the utilization of PC calculations to perform picture handling on advanced pictures. The fundamental activity performed by a straightforward advanced camera is to change the light energy over to electrical energy, then, at that point, the energy is changed over to computerized design and a pressure calculation is utilized to diminish memory prerequisite for putting away the picture. In this venture, picture pressure has been taken as an application to demonstrate the usefulness of DHT calculation in the field of advanced signal handling.

**In ref. [7]**, propose four 4:2 blowers, which have the adaptability of exchanging between the specific and rough working modes. In the rough mode, these double quality blowers give higher paces and lower power utilizations at the expense of lower exactness. Every one of these blowers has its own degree of precision in the rough mode as well as various postponements and power dispersals in the estimated and accurate modes. Involving these blowers in the designs of equal multipliers gives configurable multipliers whose exactnesses (as well as their powers and rates) may change powerfully during the runtime. The efficiencies of these blowers in a 32-cycle Dadda multiplier are assessed in a 45-nm standard CMOS innovation by contrasting their boundaries and those of the cutting edge estimated multipliers. All things considered, 46% and 68% lower postponement and power utilization in the rough mode. Likewise, the viability of these blowers is evaluated in some picture handling applications.

**Omid Akbari et al. [8]**, portrays the plan of fast Vedic multiplier that utilizes the procedures of Vedic math in view of 16 sutras (calculations) to work on the presentation. In this paper the productivity of Urdhva Tiryagbhyam (vertical and transversely) Vedic technique for augmentation which is not quite the same as the course of typical duplication is introduced. Urdhva-Tiryagbhyam is the most effective calculation that gives least deferral for duplication for a wide range of numbers independent of their size. Vedic multiplier is coded in Verilog HDL and animated and incorporated by utilizing XILINX programming 12.2 on Spartan 3E pack. Further the plan of exhibit multiplier is contrasted and the proposed multiplier as far as deferral, memory and power utilization.

### III. DISCRETE HARTLEY TRANSFORM

Discrete Hartley Transform is abbreviated for DHT and this transform was proposed by R. V. L. Hartley in 1942. DHT is the analogous to Fast Fourier transform which provides the only real value at any cost. The main difference from the DFT is that it transforms the real inputs to real outputs with no intrinsic involvement of complex value. DFT can be used to compute the DHT, and vice versa.

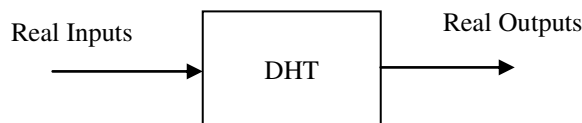


Figure 1: Block Diagram of DHT

In other words, Discrete Hartley transform is used to convert real values into real ones. It requires decomposition of data into stages using butterfly similar to FFT. But the butterfly used in DHT is quite different in terms of coefficients or multipliers. With the increase in number of DHT sequence length the number of coefficients is also increased simultaneously.

Let  $N \geq 4$  be a power of two. For any real input sequence  $\{x(i) : i = 0, 1, 2, \dots, N - 1\}$

$$X(k) = DHT(N)\{x(i)\}$$

$$= \sum_{i=0}^{N-1} x(i).cas[2ki\pi / N] \quad \text{for } k = 0, 1, \dots, N - 1$$

Where  $cas(x) = \cos(x) + \sin(x)$

#### Highly Parallel DHT for N=8

In order to clearly illustrate the features and advantages of the algorithm, the VLSI architecture for a DHT of length  $N=8$  is presented in figure 2.

It can be seen that the architecture is highly parallel and has a modular and regular structure being formed of only a few sharing block: addition, subtractor and multiplier. Each multiplier is shared by two inputs with a constant.

First two stages do not include any multiplication. Remaining terms are multiplied by the first coefficient. In the next stage again two new coefficients are introduced which is multiplied by the lower half of the third stage. In each stage multiplying of coefficients stage precedes its summing stage.

After coefficient multiplication it is preceded by its summing stage to form the common terms used in the final stage. Last stage includes only summing of terms. Finally we get the transformed data sequence in order and do not need any permutation.

Mathematical calculation for  $N=8$

$$X(0) = [(x(0) + x(4)) + (x(2) + x(6))] + [(x(1) + x(5)) + (x(3) + x(7))]$$

$$X(2) = [(x(0) + x(4)) - (x(2) + x(6))] + [(x(1) + x(5)) - (x(3) + x(7))]$$

$$X(4) = [(x(0) + x(4)) + (x(2) + x(6))] - [(x(1) + x(5)) + (x(3) + x(7))]$$

$$X(6) = [(x(0) + x(4)) - (x(2) + x(6))] - [(x(1) + x(5)) - (x(3) + x(7))]$$

$$X(1) = [(x(0) - x(4)) + (x(2) - x(6))] + c(x(1) - x(5))$$

$$X(3) = [(x(0) - x(4)) - (x(2) - x(6))] + c(x(3) - x(7))$$

$$X(5) = [(x(0) - x(4)) + (x(2) - x(6))] - c(x(1) - x(5))$$

$$X(7) = [(x(0) - x(4)) - (x(2) - x(6))] - c(x(3) - x(7))$$

$$\text{with } c = \sqrt{2}$$

Where  $c$  is the multiplier

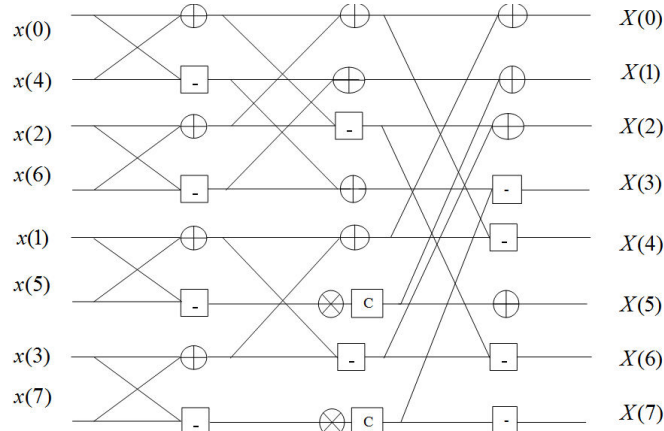


Figure 2: 8-point Discrete Hartley Transform

**Urdhwa Multiplier**

Urdhwa multiplier using KSA can compare with conventional method which is computed by vecic multiplier, full adder and half adder. Proposed technique provides less path delay and less area. Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay. Area and propagation delay can be reduced by the aid of modified KS adder. This adder will be designed like as ripple carry adder. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay.

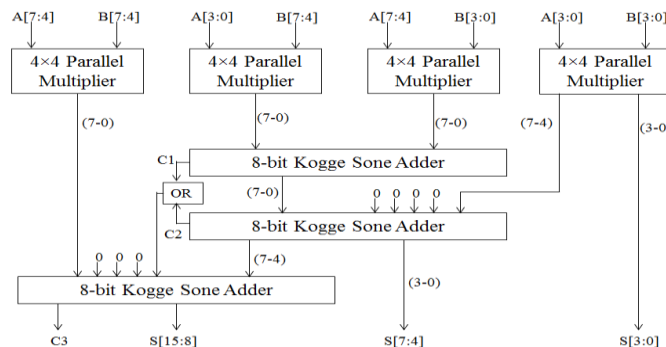


Figure 3: Logic Diagram of Urdhwa Multiplier using KSA

The sum bit of the first half adder shows the LSB bit of the output and carry output will connect to the first pin of XOR gate. The sum bit of the second half adder is connected to the second pin of the XOR gate. And the last carry output is the MSB bit of the output. Worked can be enhanced for the high bit information.

**KSA**

The Kogge–Stone adder is a parallel prefix form carry look-ahead adder. Other parallel prefix adders include the Brent-Kung adder, the Han Carlson adder, and the fastest known variation, the Lynch-Swartz lander Spanning Tree adder.

**Technique of Kogge Stone Adder**

An example of a 4-bit Kogge–Stone adder is shown in the diagram. Every vertical stage creates a "proliferate" and a "produce" bit, as appeared.

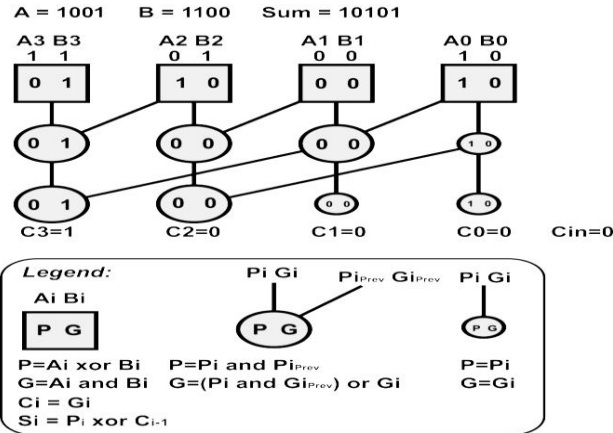


Figure 4: Logic Diagram of Urdhwa Multiplier using KSA

The coming full circle create bits (the conveys) are delivered in the last stage (vertically), and these bits are XOR with the underlying engender after the information (the red boxes) to create the aggregate bits. E.g., the main (minimum critical) total piece is figured by XORing the engender in the most distant right red box (a "1") with the convey in (a "0"), delivering a "1". The second piece is ascertained by XORing the proliferate in second box from the privilege (a "0") with C0 (a "0"), delivering a "0".

#### IV. PROPOSED TECHNOLOGY

Here, the DHT of length N=16 point requires 67 additions and 12 multiplications. We have used a different technique called Urdhwa tiryakbhyam of ancient Vedic times for multiplication. This multiplication technique reduces the delay and complexity. It converts multiplication into simple logical AND operation using associated circuits of full, half adders and AND gate. Further, the area is reduced by using various compressors for adding the partial products of multiplication.

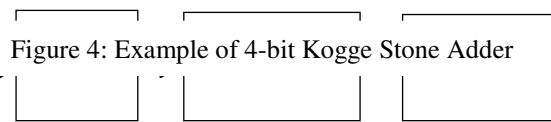


Figure 5: Proposed Architecture

#### V. CONCLUSION

DHT is a new transform used for real value to real value conversion. Urdhwa Triyambakam is an ancient technique for multiplication. DHT is used in various fields such as image processing, space science, scientific applications etc. Delay provided and area required by hardware are the two key factors which are need to be consider. Here we present DHT with 8x8 Urdhwa multiplier by using full adder, OR and XNOR gates in different types of adder. Among all adder, KSA provides the least amount of delay. Also, it takes least number of slices i.e. Occupy least area among all other adder.

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