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Survey on Reversible Arithmetic Logic Unit Based on Reversible Gate

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ABSTRACT—Reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. Reversibility plays an important role when energy efficient computations are considered. Reversible logic is used to reduce the power dissipation that occurs in classical circuits by preventing the loss of information. This paper comparative study is reversible design for 32-bit, 16-bit, 8-bit, 4-bit 2-bit and 1-bit ALU. These ALU consists of different types of operations i.e. arithmetic and logical operations. The arithmetic operations include addition, subtraction, multiplication, division and the logical operations include NAND, AND, OR, NOT, XNOR, NOR and XOR. All the modules are being designed using the basic reversible gates. Simulation and verification of the design will perform using Xilinx 14.1i with different device family.

KEYWORDS—Reversible Gates, Arithmetic Unit (ALU), Garbage Output, Quantum Cost

I. INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of $KT \cdot \log_2$ joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Bennett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. A reversible logic gate is an n -input, n -output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit.

The classical computational process which is irreversible, one bit of information is lost for each logical operation carried out by it. But in 1961, Rolf Landauer's principle states that for each bit of information.

However, this loss of energy is negligible for simple circuits and become significant for complex circuits. In 1973, Bennett showed that there would be no energy dissipation if computations are done in the reversible way [2]. Resultantly, a new paradigm in circuit design evolved with the aim of reducing the entropy increase and energy dissipation [3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed according to the above constraints is known as a reversible logic device [4].

Reversibility becomes an essential parameter for the future computer designs [4]. Reversible gates or circuits allow the reconstruction of the inputs from the observed outputs. Reversible logic is applicable to the research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology [4]. A reversible circuit should be designed using minimum number of reversible logic gates.

Parameters of Reversible Logic

There are many parameters for determining the complexity and performance of circuits in reversible logic circuit design. The following parameters should be reduced for the efficient reversible circuit design [5].

Gate count (N): This refers to the number of reversible gates used in circuit.

Constant inputs (CI): The number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function [5].

Garbage outputs (GO): The number of unused outputs present in a reversible logic circuit. Garbage outputs can't be avoided as these are essential to achieve reversibility.

Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate.

Gate levels (GL): The number of levels in the circuit which are required to realize the given logic functions[5].

II. LITERATURE SURVEY

S. Nagaraj et al. [1], semiconductor gadgets has been going through enormous improvement as far as execution, speed of the gadget on account of huge scaling of gadgets, all the while the power dispersal has been one of the central issue. As the scaling of gadget has been arrived at its limits the advancement could be the arising innovation i.e., Reversible registering in VLSI industry. As this innovation has zero power dispersal, this is a significant benefit in the reversible rationale circuits. The ALU is significant part in the framework and it is utilized in the applications like PCs, mobiles, and mini-computers. The 32 Bit number-crunching rationale unit is planned utilizing Verilog Hardware Description Language with tasks, for example, AND rationale, OR rationale, FullAdder utilizing One piece ALU. The reversible ALU can work quick as contrasted and irreversible ALU. Reversible rationale entryways diminishes power dispersal, postponement and region. So reversible entryways are utilized in VLSI plan methods. This paper presents an ALU planned of reversible rationale doors utilizing Toffoli, Fredkin, and Peres Gate which replaces the and additionally entryway for every the slightest bit ALU. Every one of the rationales are performed utilizing the virtual products Modelsim Altera 6.3g and the blend utilizing Xilinx ISE 14.7. The planned ALU utilizing reversible rationale decreases the region around 34% and delay around 48.91%.

Behrouz Safaiezadeh et al. [2], quantum dab cell automata (QCA) innovation is considered as perhaps the most appropriate substitution to decrease the CMOS-based computerized circuit plan issues at the nanoscale because of its small size, quick, inactivity and exceptionally low power utilization. One of the principle parts of chip is the math rationale unit (ALU) and as such, it goes about as the core of microchips. This paper presents a QCA innovation based reversible ALU unit utilizing essential reversible squares and an original reversible square in particular BS1 Block. The proposed block performs rationale and number-crunching tasks in the proposed plot. The recreations of the proposed plan are done by QCA Designer. As per the mimicked outcomes, the proposed structure has a 35%, 27% and 30% improvement in quantum cost, the quantity of cells and the involved region in contrast with the past led explores, separately.

Vuppala Chandralekha et al. [3], in the event that there is no deficiency of data regarding the conditions of a cycle it is named as reversibility in figuring. It is conceivable to recuperate any past states by switch processing, which is called as sensible alterability. Consistent variability is accomplished simply by utilizing actual variability. Physical variability is a technique that doesn't produce energy when applied to warm. Reversibility is a useful procedure to diminish power dissemination in low and medium power circuits. This paper presents 8-digit and 16-cycle reversible ALU plans. Correlation of the presentation boundaries region, power and LUT of the ALU plans is shown.

Hari M. et al. [4], reversibility is one of the establishments for different arising advancements like quantum, DNA and optical figuring. It could be utilized for planning ultra low power circuits, which will assist with lessening the complete energy utilization around the world. Testing of these circuits has additionally been a main pressing issue to approve their usefulness. This Paper presents an original plan of Arithmetic Logic Unit (ALU) that can be adaptable up to N number of pieces. The plan interaction uses the properties of Toffoli and Fredkin doors to make the circuit equality protecting which shows its in-assembled testability highlight. Proposed design gives full inclusion of single piece flaws in the circuit. The plan and execution is performed over reversible circuit analyzer for getting working expenses as far as number of information sources, door count, quantum cost, trash yields and ancilla inputs. As of late announced reversible ALU designs are contrasted and proposed work on a solitary stage, where we have accomplished a decrease up to 61% in the door cost.

Parth Khatter et al. [5], reversible rationale has gotten extraordinary consideration in the ongoing years because of its capacity to lessen the power dispersal which is the fundamental prerequisite in low power computerized plan. It has wide applications in cutting edge registering, low power CMOS plan, Optical data handling, DNA registering, bio data, quantum calculation and nanotechnology. Ordinary computerized circuits disperse a lot of energy since pieces of data are eradicated during the rationale activities. Accordingly, assuming rationale entryways are planned with the end goal that the data pieces are not annihilated, the power utilization can be decreased drastically. The data pieces are not lost in instance of a reversible calculation. This has prompted the turn of events of reversible doors. ALU is a principal building square of a

focal handling unit (CPU) in any registering framework; reversible number-crunching unit has a powerful enhancement on the offer. By utilizing reasonable control rationale to one of the info factors of equal snake, different number-crunching tasks can be understood.

Parth Khatter et al. [6], ALU in light of a Reversible low power control unit for number-crunching and rationale tasks is proposed. In our plan, the full Adders are acknowledged utilizing synthesizable, low quantum cost, low trash yield DPeres entryways. This paper presents a book plan of Arithmetic and Logical Unit utilizing Reversible control unit. These Reversible ALU has been displayed and confirmed utilizing Verilog and Quartus II 5.0 test system. Near outcomes are introduced as far as number of doors, number of trash yields, number of steady information sources and Quantum cost.

S. M. Swamynathan et al. [7], presents novel the slightest bit number juggling and coherent unit (ALU) plan utilizing essential reversible entryways. Two plans for both the number-crunching and the intelligent unit are proposed and one plan for the control unit is likewise advanced. These plans are coordinated together to give four complete ALU plans. Every one of the proposed plan has been carried out in Verilog HDL utilizing Xilinx ISE Suite 14.1 programming to check its usefulness. The proposed plans are thought about in view of quantum cost, trash yields and ancilla inputs with their current partners. The straightforwardness and the decreased quantum cost of the proposed ALU plans, when contrasted with the current ones, makes them ideal contender to be utilized as modules in quantum PCs. The proposed ALUs stretch out their applications to cryptography, AI and nanotechnology.

Kamaraj et al. [8], an Arithmetic rationale Unit (ALU) is utilized in number juggling, consistent capacity in all processor. It is likewise a significant subsystem in computerized framework plan. Number-crunching Logic Unit (ALU) is one of the main parts of any framework and is utilized in numerous apparatuses like adding machines, phones, and PCs. A 32-bit ALU was planned utilizing Verilog HDL with the sensible doors, for example, and additionally for every the slightest bit ALU circuit. The plan was executed in Xilinx. It can work quick than the ALU processor utilizing less power. The plan of an ALU and a Cache memory for use in an elite execution processor was inspected. Reversible rationale indispensable as of late in light of the fact that it has capacity to decrease the power dispersal which is primary prerequisite in low power plan. ALU which are planned utilizing non reversible rationale doors consume more power. So there is a requirement for lesser power utilization and the reversible rationale has been assuming indispensable part during ongoing years for low power VLSI Design methods. This method helps in lessening power utilization and power dispersal. This paper presents an execution of ALU in light of reversible rationale while contrasting it with an ALU design with the typical rationale doors. Every one of the modules are mimicked in modelsim SE 6.4c and orchestrated utilizing Xilinx ISE 14.5. ALU which is planned utilizing non reversible rationale doors consume more force of around 0.312 mw and the execution of ALU in light of reversible rationale decreases the power utilization during activities to around rates.

III. REVERSIBLE GATES

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an $m \times n$ capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

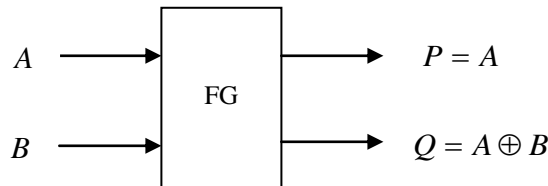


Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

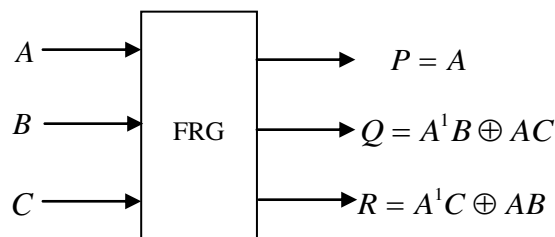


Figure 2: Fredkingate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

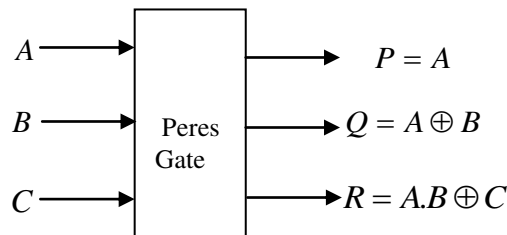


Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when $D = 0$, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

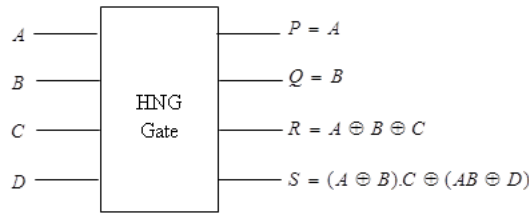


Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PFAG) gate is presented which produces outputs $P = A$ (5)

$$Q = A \oplus B \text{ (6)}$$

$$R = AB \oplus C \text{ (7)}$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \text{ (8)}$$

IV. PROPOSED METHODOLOGY

The RALU utilizes the DKGgate and BME gate to produce eight logical calculations: transfer A, addition, Sub, XOR, OR, AND, NOT and NAND. The cost and delay calculations are identical to the ALU in figure 5. The RALU has 8 inputs and 8 outputs. The inputs consist of three data inputs (A, B and C_{in}) and five (S_0, S_1, S_2, S_3, S_4) lines.

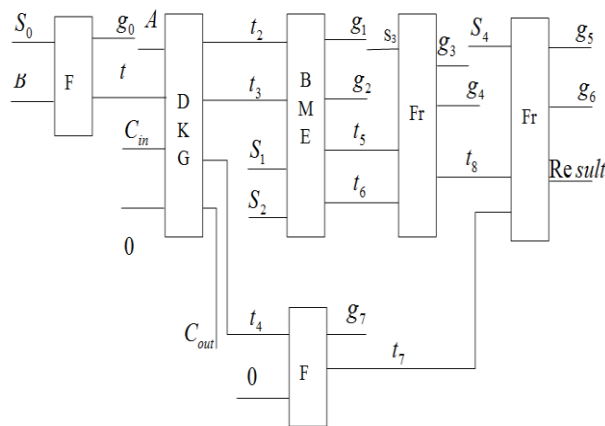


Figure 5: Block Diagram of Proposed Methodology

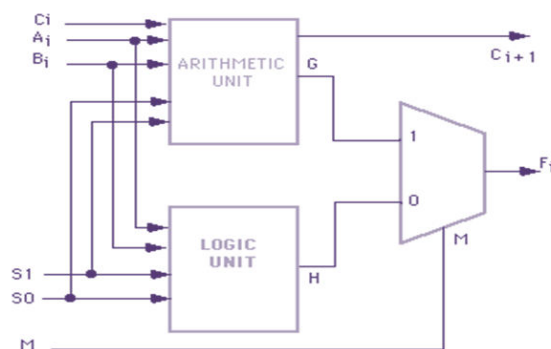


Figure 6: Flow Diagram of Arithmetic Logic Unit

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

ALU stands for "Arithmetic Logic Unit." An ALU is an integrated circuit within a CPU or GPU that performs arithmetic and logic operations. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include Boolean comparisons, such as AND, OR, XOR, and NOT operations.

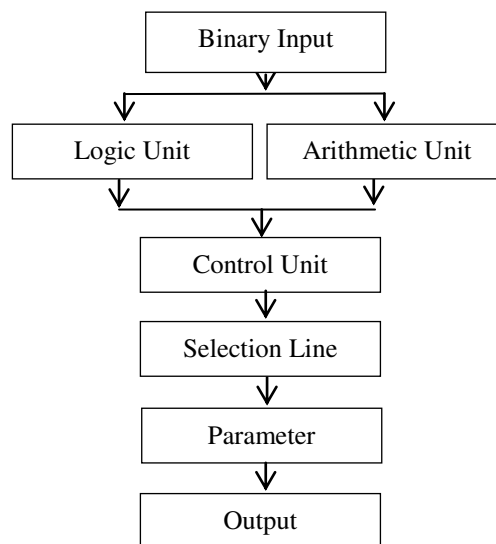


Figure 7: Flow of bit Slice ALU

V. EXPECTED RESULT

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

1. Design 64-bit, 32-bit, 16-bit, 8-bit, 4-bit, 2-bit and 1-bit using different types of reversible gate.
2. Design different types of programmable reversible gate and compared.
3. Design free garbage based architecture using different types of input and compared existing algorithm.
4. Hand calculation of delay and area in reversible arithmetic logic unit in different inputs.
5. All the modules design to different device family i.e. Spartan-3, Virtex-4 and Virtex-7.

VI. CONCLUSION

The 4bit reversible ALU is designed by integrating various sub modules that includes adder/subtract or, and logical unit. The logical unit performs AND, OR, NOR, XOR, NAND. The performance evaluation of the various sub modules are carried out using Modalism 6.5 tools and it was found that the circuits designed using reversible logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

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