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A Design of 6T- Auto Awake Mode of SRAM for Low-Power Consumption

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ABSTRACT: In the digital world, Static Random Access Memory (SRAM) is one of the efficient core component for electronics design, it consumes huge amount of power and die area. In this research, the SRAM design analysis in terms of read margin, write margin and Static Noise Margin (SNM) for low power application is considered. In SRAM memory, both read and write operation affect by noise margin. So, read and write noise margins are considered as the significant challenges in designing SRAM cell. In this research, robust 6T-SRAM cell is designed to decrease the power utilization. The Auto Awake Mode is developed to control the entire 6T-SRAM cell design. The proposed 6T-SRAM- Auto Awake Mode (6T-SRAM-AAM) was implemented to reduce power utilization of understand and write down operation inside the 22 nm FinFET library. The experimental results showed the proposed 6T-SRAM-AAM design reduced power consumption of read & write operation up to 25% to 33.33% compared to existing Static RAM cells design.

KEYWORD: SRAM, LOW-POWER CONSUMPTION, 6T - SRAM DESIGN, AUTO SENSING MODE.

I. INTRODUCTION

Nowadays, the handheld electronic Instruments such as movable telephone, handy cam, Lap top etc. are becoming more important part of personal computing and is mainly calculated to offer a matching set of compute, message and informational apparatus in a gadget about the size of standard palm. The low down power SRAM circuits contain develop into a important component of many VLSI circuit chips [1-3]. In past decades, the traditional CMOS technology has been affected by two major problems, those are less reliability and more power utilization [4]. Through a write down operation, 60% of the total dynamic power require to operate bit lines in traditional SRAM cell designs [5],[6]. The Cache built on adiabatic principles is introduced based on slowly varying supply voltages [8]. This method reduces the total power dissipation, which uses several power switches and the position produce circuit in extra area overhead. To overcome the above-mentioned problem, the 6T-SRAM-AAM cell is designed in this paper. The AAM is controlled by the SRAM cell design when the AAM condition was one, at the time SRAM cell perform otherwise it does not perform. The proposed 6T-SRAMAAM cell design efficiently reduced power consumption and impediment of the system balance to the 7T-SRAM cell design.

II. CORRELATED WORK

Many researchers have suggested a numbers of the techniques for SRAM cell design. A brief evaluation of a few significant Static RAM cell designs is existing in this part. Byung-Do Yang [5] proposed a small power Static RAM

using BL access recycle for understand writing and put in writing operations. This proposed charge recycling SRAM design was based on the hierarchical BL architecture and BL charge recycling method. The proposed method was achieved less degradation of SNM, 17% & 84% of read and write power consumption respectively achieved. other than the operation speed is inadequate to 145MHz.W. Kang et al. [9] introduced a non-volatile SRAM propose with Magnetic Tunnel Junction. They designed MAP of the MTJ device. The switching techniques provided better accumulate power, delay, and dependability disquiet. The main limitation of the system is, it consumes more switching power. A. Makosiej et al. [10] introduced TFET-based 8T SRAM cell. The 8T SRAM cell maintains full functionality in all operation modes at 1V supply voltage with no architectural limitation linked to the half-selection problem. The cell design allowed the use of long word lines with bit interleaving. The major drawback of the Static-RAM design is, whenever the supply voltage increases, at the time substantial leakage power also increases. E. Karl et al. [11] proposed a huge presentation, voltage scaling of 162 Mb Static RAM range was urbanized in 22nanometer tri-gate bulkiness equipment. The 22 nm tri-gate technology delivered a 0.092m High-Density Cell (H-DC) bit cell and 0.108 m Low Voltage Cell (LVC)bit cell. The main limitation of the 6TStatic-RAM design is, internal sensing delay is very high. These all related works have several issues like more delay and power consumption, high critical cell design. Here, the 6T-SRAM-AAM cell design is implemented to overcome these problems and to minimize dissipation of power and delay comparison of existing SRAM cells design.

III. 6T-SRAM-AAM SYSTEM

In this paper, the SRAM architecture design consists of 6Ts with a symmetrical configuration that maintains the threshold voltage of the system. The SRAM plays an important role in VLSI technology due to its low-latency and large storage. A numbers of transistors employed in the SRAM circuit, which limits the reliability of the circuit. In this work, the designing based on the AAM circuit design.

The conventional 6T SRAM circuit requires three BL (like 2-BLs (BL &BL_b) and one WL used for any read and write operations.

6T- AAM- SRAM Cell Design

A circuit diagram of the 6T-SRAM-AAM design, which balancing several factors including area, power/leakage consumption, and speed performance.

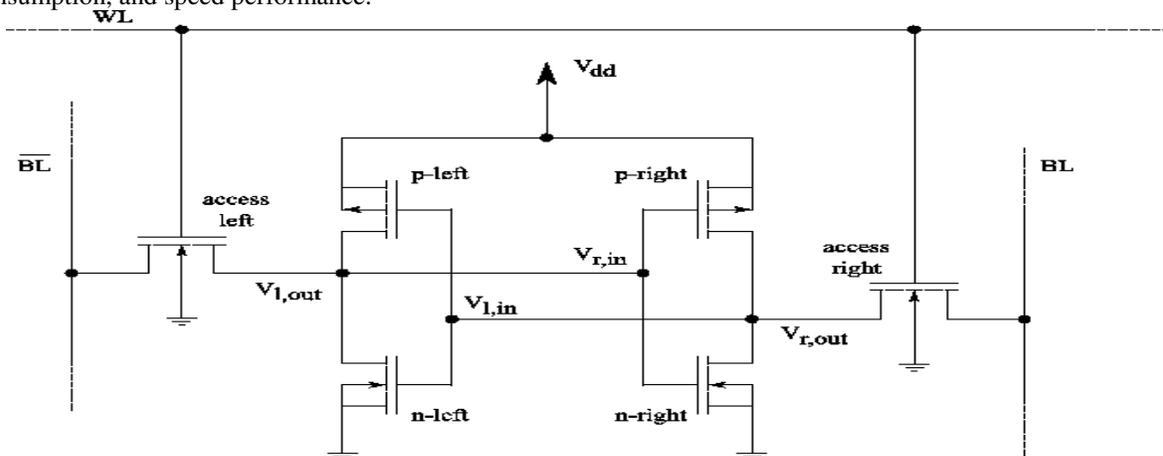


Figure 1. 6T-SRAM-AAM circuit diagram.

Static random access memory (SRAM) can retain its stored information as long as power is supplied. This is in contrast to dynamic RAM (DRAM) where periodic refreshes are necessary or non-volatile memory where no power needs to be supplied for data retention, as for example flash memory. The term "random access" means that in an array of SRAM cells each cell can be read or written in any order, no matter which cell was last accessed.

The structure of a 6 transistor SRAM cell, storing one bit of information, can be seen in Figure 1. The core of the cell is formed by two CMOS inverters, where the output potential of each inverter V_{out} is fed as input into the other V_{in} . This feedback loop stabilizes the inverters to their respective state.

The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell. In standby mode the word line is low, turning the access transistors off. In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential $V_{1,out}$ is high and the p-channel MOSFET of inverter two is turned off, $V_{r,out}$ is low.

To write information the data is imposed on the bit line and the inverse data on the inverse bit line, \overline{BL} . Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved.

For reading the word line is turned on to activate the access transistors while the information is sensed at the bit lines.

SRAM Read Operation

For a proper read operation, both the BLs such as BL and BL_b are pre-charged to V_{dd}. When the WL goes high (value 1) it enables the access transistors. Some read pulses are stored in the memory after the read operation is done. If the internal node Q value is bit 1 then the internal node Q_{bar} is bit 0. At the time value of the BL_{bar} is bit 1 and internal node Q_{bar} is bit 0. Here, the BL and BL_{bar} values are used to sense the amplifier, which act as a comparator.

SRAM Write Operation

If the content of the memory is 0 then the internal node (Q_{bar}) value becomes 1 and these values are stored in Q. The WL=1 value is required to write operation in the 6T-SRAM-AAM-. If the WL=0, it is not possible for a write operation. Here, an input operation is done by using BL and BL_{bar}. The BL_{bar} is connected to ground because of the internal node Q value is 0 at the time V_{dd} value is 1, here voltage is different so that entire system voltage is discharged.

6T- SRAM Design based on AAM Operation

The AAM design has 2-PMOS and 4-NMOS. AAW design having 3T such as 1 PMOS (MFET7) and 2NMOS (MFET8, MFET9). The 6T- SRAM output is given into the MFET 8 and MFET 9, these base stations are connected to MFET7, which act as AAM. The AAM control the overall 6T-SRAM cell based on power consumption. By using AAM circuit, the static power of the SRAM design will reduce. In the AAM- SRAM cell, data will be maintained and a voltage around SRAM memory must be greater than the minimum data retention voltage. Earlier do research perform to decrease the power consumption of Static Rams design. In that design, which is employed to increase the fundamental technology of transistor size and leakage. The existing high-performance SRAM cells use an asymmetric configuration of the 6Ts. It can minimize the leak by employing upper, but the usage of high transistor causes the performance of SRAM cell by unacceptable line margin. In this research, the asymmetric SRAM cells minimize the leakage by selecting the preferred state and this also reduces the performances of transistors when cell is in the same status. The experimental results of proposed 6TSRAM-AAM cell design is briefly explained as follows.

IV. RESULT AND DISCUSSION

A power and delay of an SRAM cell designs are the two key design circuits in the nanometer scheme. For comparison, this paper Employed the 6 Transistors-Static RAM-AAM cell design. This paper implemented 22nm technology in FinFET library for 6T-SRAM-AAM cell design. The Schematic track diagram of the 6Transistor-SRAM –AAM is given below.

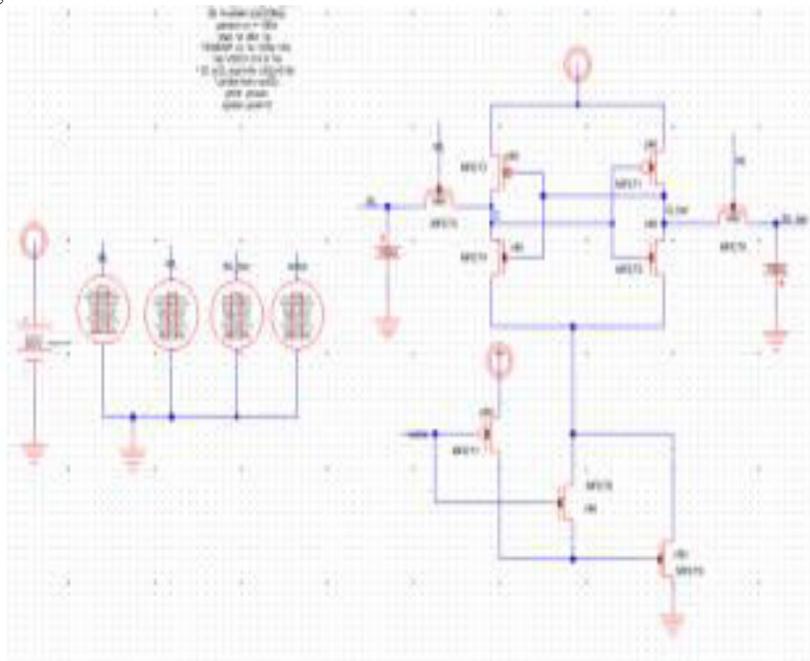


Figure 2. Schematic circuit diagram of the 6TransistorSRAM-AAM

Area computation

The area can be optimized by having a lesser number of cells and by replacing multiple cells with a single cell that includes both functionalities. In this paper, the transistor area is computed by transistor width and length (1Transistor = 15 (width)*24 (length) = 360n).

Power computation

The power consumption by the particular source is computed by multiplying the average current drawn from the source and voltage provided by the source.

Delay computation

The Static RAM delays are termed as the time required to change Static RAM cell design one sense gate to another sense gate. The wait is computed difference of time between the 0 to 0.9 voltages.

Table.1. Implemented based on 22nm technology for existing methods like 7T-SRAM, 6T-SRAM, and 6TSRAM-AAM.

Design	Operation	Area (nm)	Dynamic Power (µm)	Delay (ns)
7T-SRAM	Read	2520	900	0.5
6T-SRAM	Read	2160	540	0.1
6T-SRAM-AAM	Read	3240	360	0.01
7T-SRAM	Write	2520	1080	0.4
6T-SRAM	Write	2160	720	0.2
6T-SRAM-AAM	Write	3240	540	0.01

Table 1 shows the area, power consumption and delay performance of conventional 7T & 6T SRAM cell design and 6T-SRAM-AAM cell design. In both methods occupied more area and consume more power. In this paper, the 6TSRAM cell is designed by using AAM, which used SRAM operation control by the AAM that improved lowpowerconsumption and delay performance compared to 7TSRAM and 6T-SRAM cell design. The comparison graph of the power and delay performances are shown in Figure 3 and 4. These results are drawn by using 20nm technology for different methodologies. According to the graph, the blue and orange color represent existing technology and the gray color represent 6T-SRAM-AAM cell design. From this graph, it is clear that 6T-SRAM-AAM design consumes less power and occupied less area than the 6T-SRAM and 7TSRAM cell design.

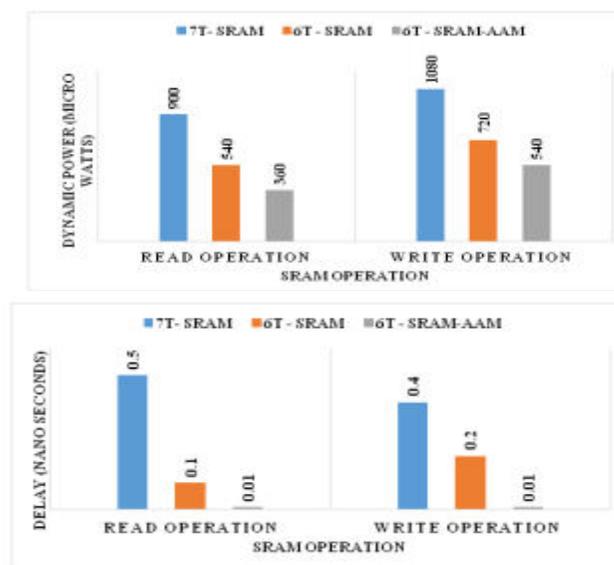


Figure 3. Performance of delay for SRAM cell designs in 22nm technology

Tab.2. Reduced performance of total dynamic, static power and total delay for existing and 6T-SRAM-AAM design.

Design	Total Dynamic power (μ W)	Total static power (μ W)	Total Delay (nS)
7T-SRAM	1980	27.9	0.9
6T-SRAM	1260	21.15	0.3
6T-SRAM-AAM	900	18.45	0.02

The total dynamic power, total static power and total delay performance of the existing and 6T-SRAM-AAM design shown in Table2. From the table, total dynamic power is computed based on read and write operation, if the condition $WL=BL=RL=1$. In Table2, it clearly shows 900 μ W of total dynamic power is reduced by using 6T-SRAM-AAM design compared to existing methods like 7T-SRAM and 6T-SRAM. Furthermore, if the condition $WL=BL=RL=0$, then the read & write operation is not possible in the SRAM circuit design. At the time the total static power is computed in SRAM cell design. The 18.45 μ W of total static power minimized by the 6T-SRAM-AAM design compared to existing SRAM cell designs. As well as the total delay also reduced 0.02 ns by using 6T-SRAM-AAM design compared to existing methods. the compression graph of total dynamic/ static power performance for SRAM cell designs in 22nm technology. comparison performance of total delay for SRAM cell design in 22 nm technology.

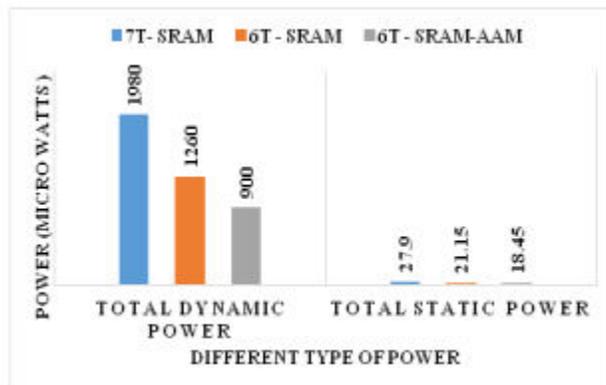


Figure 4. Comparison performance of total dynamic and static power for SRAM design in 22 nm technology

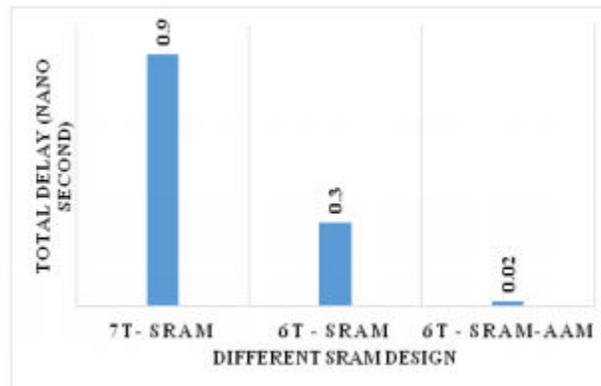


Figure 5. Comparison of total delay performance for 22 nm technology

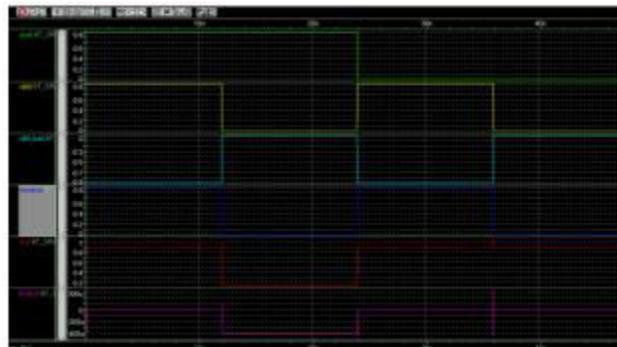


Figure 6. Performance of Read operation of the 6T-SRAM-AAM design

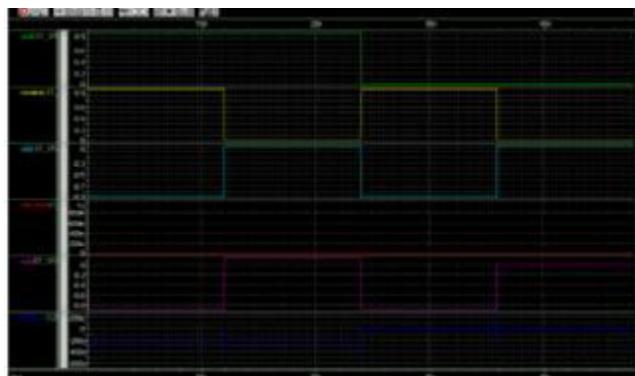


Figure 7. Performance of Write operation of the 6T-SRAM-AAM design

The Rd function of the 6TransistorStaticRAM-AAM design. The write operation of the 6T-SRAM-AAM design. The delay performance of the 6T-SRAM-AAM design is illustrated the static power performance of the

6TransitprStatic RAM-AAM design. Fig. 8 shows the conditions of BL is 0.9v, WL is 0.9v and BL_bar is -0.9v in read operation of the 6T-SRAM-AAM design. BL is -0.9v, WL is 0.9v and BL_bar is 0 in write function of the 6T-SRAM-AAM design. Delay performance computed between the 12 v to 12.1v. Static power is computed by the threshold voltage (v) and current (I). Finally, the6T-SRAM-AAM design is used to calculate the static power performance of BL, WL and BL-bar.

V. CONCLUSION

The SRAM design is used for high-speed operation with less power scheme by employing small voltage swings on the bit-line margin. In this research, the 6Transistor Static RAM cell was designed in 22 nm FinFET technology based on AAM controller to minimize the power consumption of the both Rd& WR operation for real time applications.. Hence, the proposed method achieved 33.33% of dynamic power (μm) in read operation, 25% of dynamic power (μm) in existing 6T Static RAM cell.In this research, both 7Transistor SRAM and 6T SRAM cells has been designed and compare to this cell designs the proposed 6T-SRAMAAM design obtained better power consumption. In Future work, the leakage current will play significant role to minimized power consumption. By creating a layout of the transistors SRAM cell design in Xilinx or Cadence tool, it can minimize area, respectively.

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