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# Study on VLSI Circuit with Reference to Power Estimation

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**ABSTRACT-**The performance of scatter techniques shows that the approximation outcomes of our approaches are more accurate in terms of overflow and run time than the previous congestion models. The Steiner tree breakthrough is developed to consider global scatter but the improvement on the approximation accuracy is found to be insignificant. Results show that our congestion model can approximate congestion with smaller error efficiently. With decreasing feature sizes and increasing transistor counts, power density in VLSI paths has increased dramatically. Since the heat generated by a VLSI path is proportional to its power density, the corresponding rise in on fragment temperatures adversely impacts reliability, path performance, and cooling costs. The delay of global cables subject to large temperature variations is no longer linearly proportional to cable length. To have an accurate approximation of cable delay, the temperature effect including thermal gradients has to be considered. Since the thermal profile on the die is mainly determined by the locations of macro blocks, it is, therefore, possible to perform temperature dependent delay approximation at the floor planning stage.

**KEYWORDS:** VLSI Circuit, Delay Estimation, Thermal Profile, Different Nano Technology

## I. INTRODUCTION

In VLSI technology, a single fragment contains more than billions of transistors. The overall plot process is divided into a sequence of steps: system specification, architectural plot, logic plot, path plot, physical plot or path layout, fabrication, packaging and trial (Hu et al 1985). These plot steps are demonstrated by the flow chart given in Figure 1.1. The plot cycle starts with the system specification. It is used to determine the specifications of the system, primarily functionality, performance, and physical dimensions.

It also includes the plot techniques and fabrication technology. The specifications for the size, speed, power, and functionality of the VLSI system are determined by technology, market demand, and economical perspective (Sherwani 1999). In the architectural plot step, the plot purpose and system constraints are defined.

The system is split into several sub components that interact with each other. Next, functional plot involves identifying the main functional components of the system as well as the interconnection requirements between the components. Generally, a timing pattern or other relationships between components are the end result of the functional plot.

The derivation and testing of the practical plot-conforming common sense shape is the primary focus of the common sense plot step. Typically, the smallest good judgment plot that corresponds to the practical plot is created using Boolean expressions to represent the common sense plot. Simulation and trial can also be used to determine whether the device in the good judgment plot is effective and accurate. The direction plotter then uses Boolean expressions to turn the good judgment plot into a road map while keeping in mind the unique plot's timing and power requirements. The physical plot is also known as the course layout. A path is represented geometrically in a graph. The significant test of the course design step is to change over the heading delineation of each and every viewpoint into a mathematical portrayal, which is a bunch of mathematical charts completing the alleged presence of mind normal for the relating part. Optimizing a particular objective while satisfying certain plot requirements is the process by which the geometric positions of the modules and the path of the nets are determined. Additionally, the major design issue is broken down into numerous subproblems. A discrete or nonlinear escalation problem can be used to describe any one of these subproblems. This step is covered in greater detail in the following section (Gerez, 1999). Last but not least, the

fabrication system includes a number of stages, including the transfer of the diagram data to tape, instruction of the wafer, deposition, and diffusion of various substances on the wafer. After a successful examination of the applied prototype of a fragment, it is prepared for mass production. In the end, the wafer is made and cut into person fragments in a facility for making things. After that, each fragment could be packaged and examined to make sure that all of the plot details are in place (Behjat, 2002). The VLSI plot cycle is a complex, iterative system in which representations are transformed in a number of steps. Each step affects the resulting steps and mistake occurred in any step will prompt go in the future to the first step. If mistakes or violations are found, for instance, a positive step can also be repeated and revised. As the illustration is iteratively expanded to ensure that it satisfies the course requirements, this cycle may also be repeated. The plot technique is repeated several times until all of a fragment's plot requirements are satisfied (Luo, 2008). The scatter diagram issue in the Physical plot, which plays a crucial role in the IC plot, is the primary focus of this thesis. because the effectiveness with which the course can be laid out in accordance with the formal regulations dictated by using VLSI technology is determined by the exceptional of a given scatter answer.

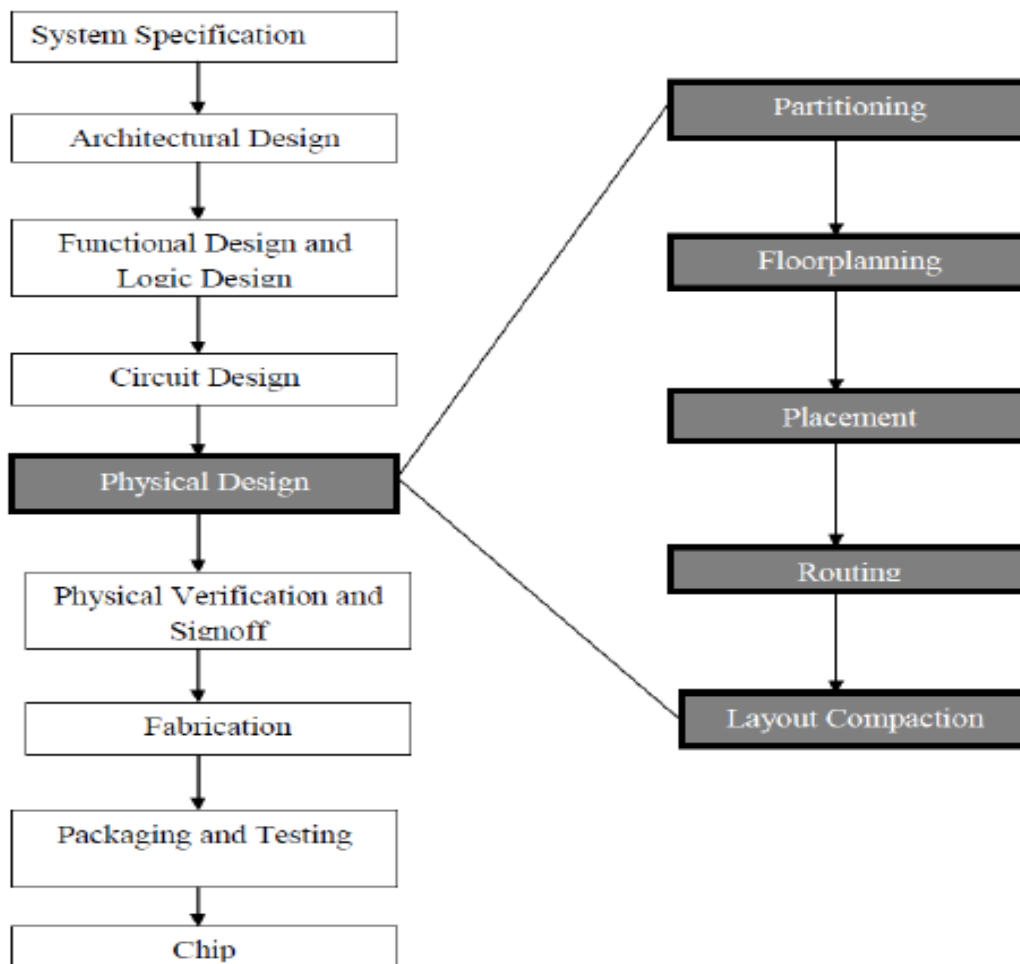


Figure 1: VLSI Design Process

## II. PROPOSED METHODOLOGY

The floorplan description file along with their connectivity information (Matrix) between the blocks should be given as input to the temperature driven Cable-planning breakthrough. The proposed flowchart will be given in Figure 5.2. The thermal map has been generated for each floorplan using hotspot tool. In Floorplan, the cable planning breakthrough invokes routine in Hotspot to calculate the temperature distribution and uses the maximum temperature as one of the metrics in the cost function.

The connectivity information among the blocks is stored in a two dimensional matrix in a Hot Floorplan and manhattan distance is used to approximate the cable length between two endpoints in a cable (Chen and Chang, 2006). In thesis, we have described a completely new model to analyze the behaviour of hot spots based on a purely geometric approach. A geometric model is proposed to evaluate the cumulative thermal power at any point of the fragment floor. The layout of each cable is determined by performing L-shape scatter between the centres of the connecting blocks. After identifying the physical layout of the cable, record the blocks over which the cable is routed.

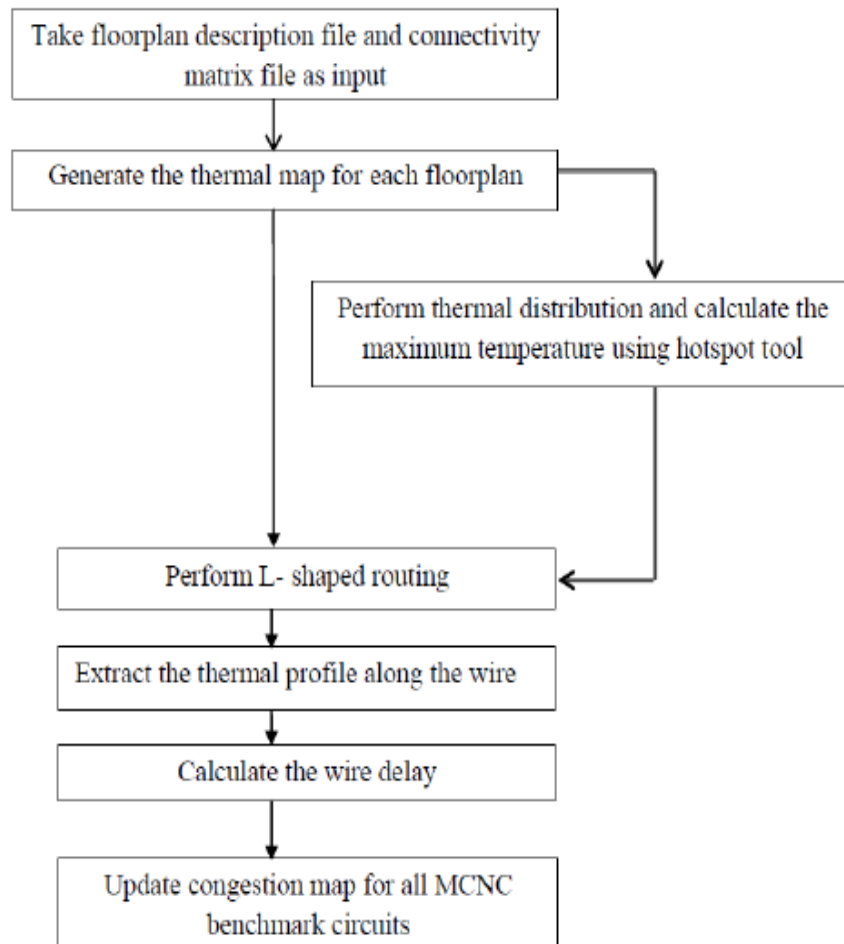


Figure 2: Proposed Flow Chart

With thermal effects taken into consideration, the two paths in the bounding box of two end points of a cable can have different delay, although their length are the same. The path which is having shorter delay has been chosen in the proposed breakthrough. In order to avoid scatter congestion, the congestion map is helpful since more cables are likely to be routed in regions with low temperature.

### III. SIMULATION RESULT

#### Delay Approximation

Using different thermal profiles, the delay increase in a global cable for 50 nm, 45nm, 40nm and 32 nm processes are plotted in Figure 3 to Figure 6. The red curve in solid line is the delay calculated with a thermal profile extracted from Hotspot tool. For comparison purpose, we also plot the delay increase with uniform temperature profiles are used namely the maximum, the average and the room temperature.



The delay at the end of the cable using the extracted thermal profile is 20 ns, while using the maximum and average temperatures can result in errors larger than 25%. This means when estimating global cable delay, we need to take the thermal gradient and not the maximum or average temperature into consideration.

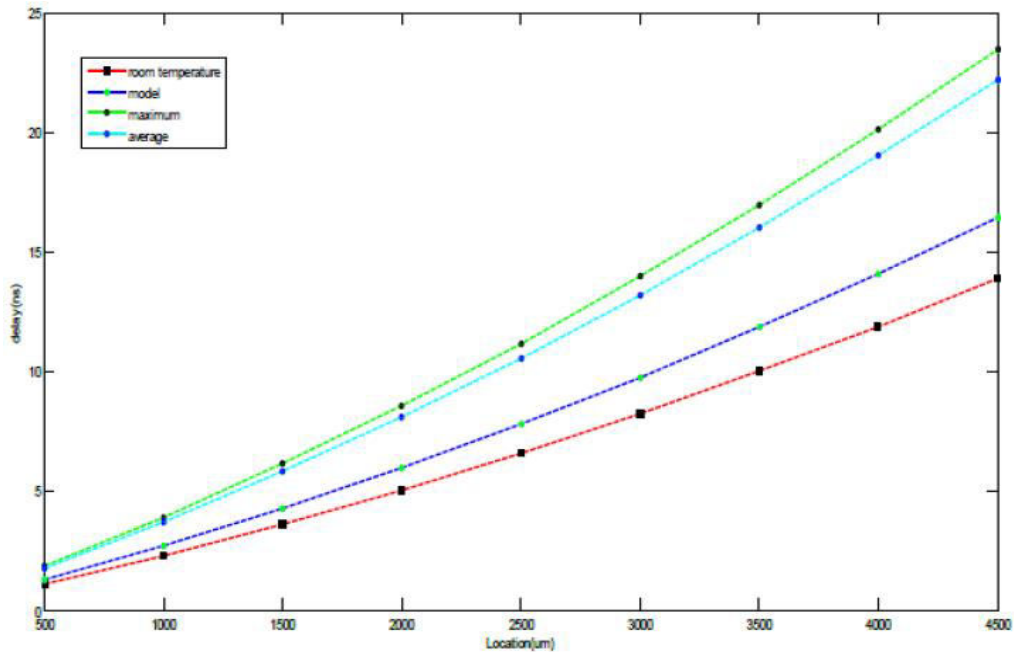


Figure 3: Delay Estimation in Thermal Profiles for 50 nm

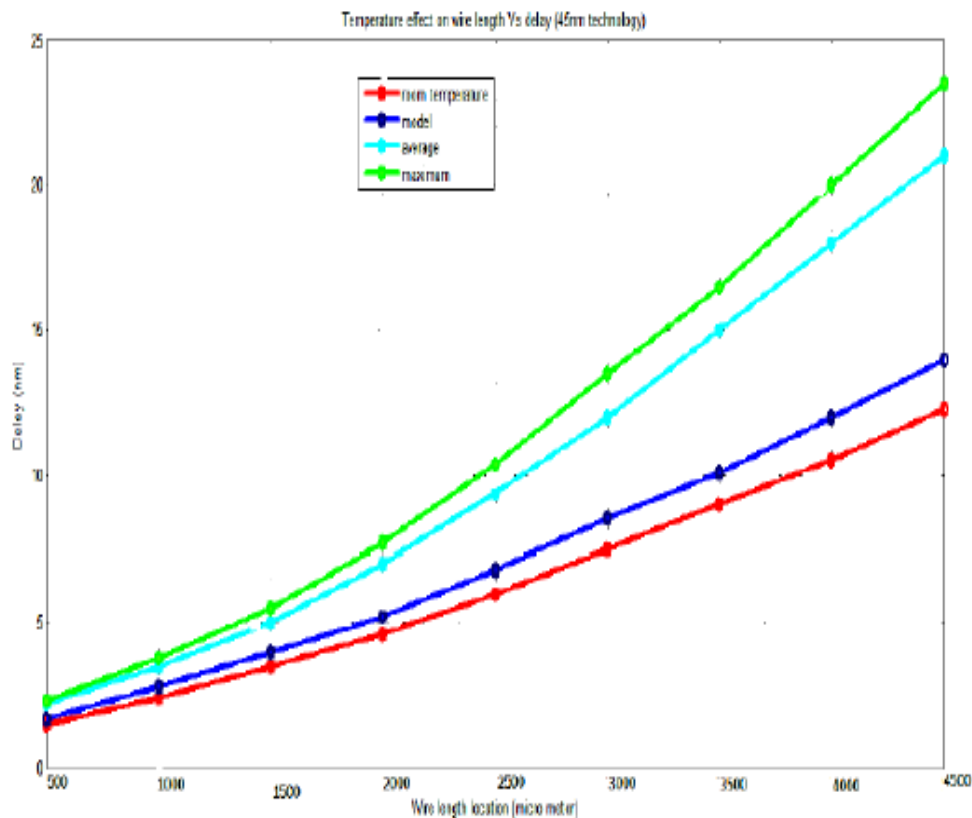


Figure 4: Delay Estimation in Thermal Profiles for 45 nm

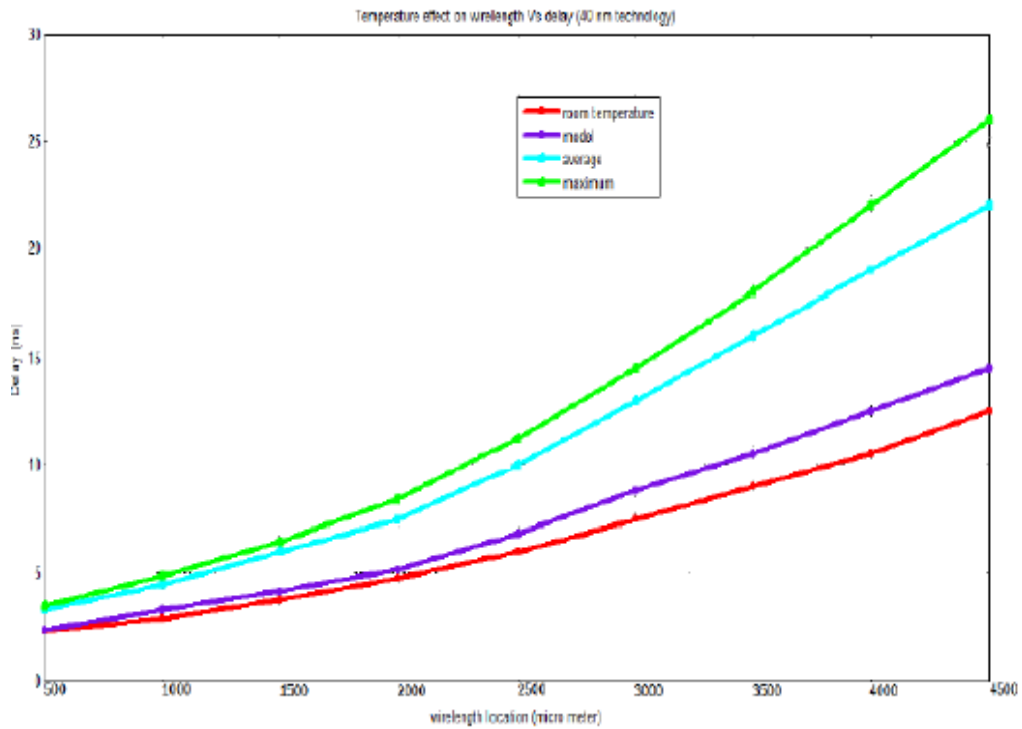


Figure 5: Delay Estimation in Thermal Profiles for 40 nm

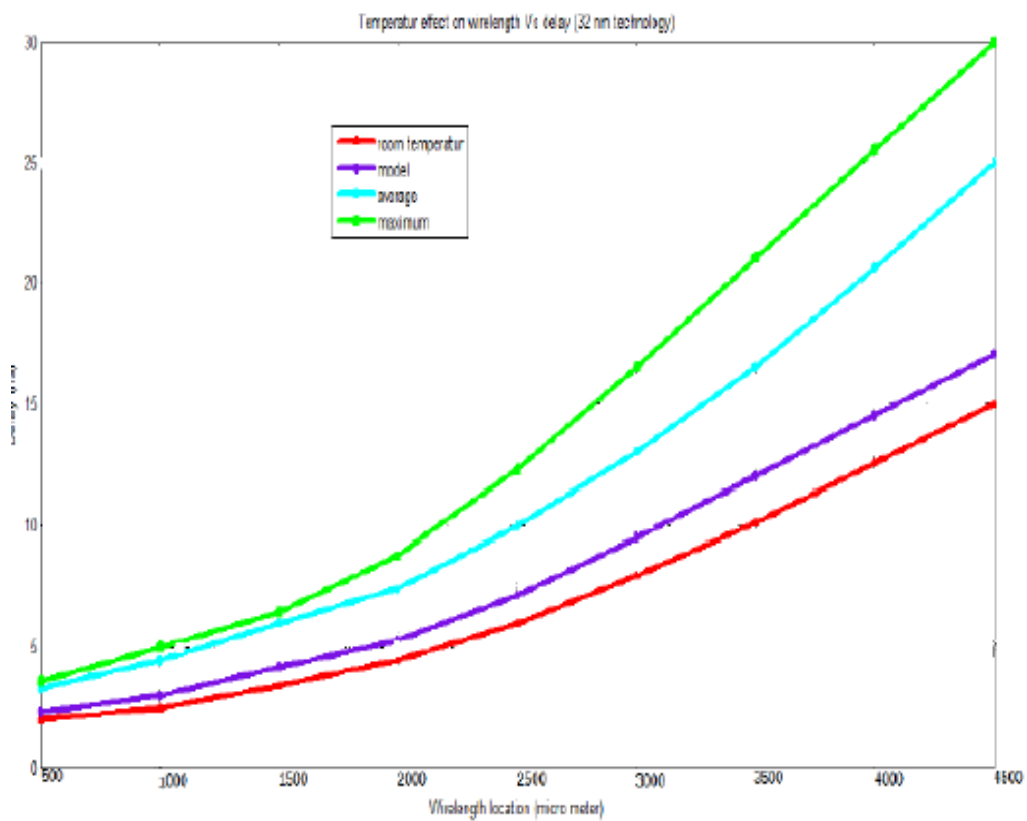


Figure 6: Delay Estimation in Thermal Profiles for 32 nm

#### IV. CONCLUSION

A significant aspect of this technique is that it can be adapted to a given place and route engine by a one-time process of characterization. Since the cable length approximation technique is based on creating a black box model of the place and route engine by characterization, it might be possible to create similar models for other place and route systems. Thus, proposed techniques have been used to provide a close interaction between the synthesis stage and the final place and route in order to achieve timing convergence. Moreover, it is shown that there is an inherent noise in place and route tools which causes variations in the cable length for the same netlist when some insignificant variables in the netlist file are changed, which makes it difficult to predict individual cable lengths, most notably for short cables, and to a lesser extent for long cables. The noise voltage for different interconnect length and width & coupling capacitance for interconnect spacing are analyzed for various nanometer technologies. Then the comparison of interconnect bandwidth and delay for various space and width of interconnect are done to approximate the prime interconnect delay.

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