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# Design and Implementation of LCVCO for PLL

Sri.P. Vali Basha<sup>1</sup>, A.V.Deepthi<sup>2</sup>, A. Bhuvana Priya<sup>3</sup>, J.Raj kumar<sup>4</sup>, D.Bavitha<sup>5</sup>

Assistant Professor, Department of Electronics and Communication Engineering, N.B.K.R Institute of Science and Technology, Vidyanagar, Tirupati, Andhra Pradesh, India<sup>1</sup>

UG Student, Department of Electronics and Communication Engineering, N.B.K.R Institute of Science and Technology, Vidyanagar, Tirupati, Andhra Pradesh, India<sup>2 3 4 5</sup>

**ABSTRACT:** The design and implementation of a low-power, high-performance LC Voltage Controlled Oscillator (LCVCO) for Phase-Locked Loop (PLL) systems. The LCVCO serves as a critical component in PLL's, which are widely used for frequency synthesis, clock generation, and synchronization in modern communication and digital systems. The proposed design leverages an LC tank topology and careful transistor sizing to achieve a broad tuning range, low phase noise, and high linearity while maintaining low power consumption. The implementation process involves optimizing circuit parameters and applying advanced design techniques to meet stringent performance criteria. Through comprehensive simulations and analysis, the effectiveness of the designed LCVCO in achieving the desired specifications is demonstrated, showcasing its potential for integration in a variety of PLL applications across different technology nodes.

**KEYWORDS:** Phase Locked Loop, Voltage Controlled Oscillator, LCVCO.

## I. INTRODUCTION

A Phase Locked Loop is a closed loop feedback control system which is capable of generating a clock signal that has a fixed relationship to the reference clock signal. It causes a particular system to track with another one [1]. The PLL technique is active around for a long time. It has various applications include keeping power generators in phase, synchronizing to the pulse in a TV set [2], clock recovery from asynchronous data, demodulating an FM modulated signal and so on. Although there are legitimate applications, the primary use is frequency synthesis. The General block diagram of the PLL is illustrated in Figure 1. The primary function of the PLL is the VCO's output using externally present reference signal and output of the frequency divider. Both signals are in phase with each other. Further, the VCO's output indicates that the phase difference between both the signals is constant with respect to time[3].

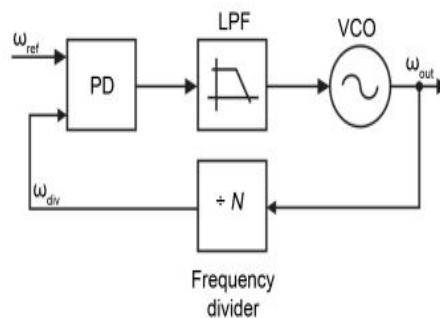


Figure 1. Block diagram of PLL

An essential module in the PLL is the Phase Detector (PD) or PFD [4]. It compares the reference frequency signal with the signal fed back from output of the VCO, and the difference signal is used as an input to both the loop filter and the VCO. In digital PLL (DPLL), the logical element is the PFD and the competence of the PFD produces a zero dead zone that leads to an attractive recording and locking performance in the PLL[5].

## II. LITERATURE REVIEW

[1] Title:Phase Frequency Detector with Minimal Blind Zone for Fast Frequency Acquisition.

Authors:Chen, W.H., Inerowicz, M.E. and Jung, B. (2010).

**Description:**Blind zone in a phase-frequency detector (PFD) reduces the input detection range and aggravates cycle slips. This brief analyzes the blind zone in latch-based PFDs and proposes a technique that removes the blind zone caused by the pre-charge time of the internal nodes. With the proposed technique, the PFD achieves a small blind zone close to the limit imposed by process-voltage-temperature variations. The comparison between the proposed design and previous works is presented. Fabricated in a 130-nm CMOS technology, the measured blind zone is 61 ps, which is smaller than that of the existing topologies by almost 100 ps.

[2] Title:Fast Frequency Acquisition Phase Frequency Detectors for Gsamples/s Phase-Locked Loops.

Authors:Mansuri, M., Liu, D., Yang, C.K. (2002).

**Description:**Phase-locked loops (PLLs) have been widely used in high-performance microprocessors and high-speed digital communication systems as clock generators. As the speed of these systems is increasing, PLLs with higher operating frequency and lower jitter are in demand. A common architecture for clock generation uses a phase-frequency detector (PFD) for simultaneous phase and frequency acquisition. Generating a high-frequency clock increases the difficulty of the design of the PFDs, particularly for systems with a high input clock frequency and minimum frequency multiplication.

[3] Title:Design of a CMOS PFD-CP Module for a PLL. Sadhana.

Authors:Anushkannan, N.K. and Mangalam, H. (2015).

**Description:**Modified design of Phase frequency detector (PFD) with reduced dead zone and improved charge pump (CP) with reduced current mismatch for a Phase Locked Loop (PLL). Three modified PFD circuits are proposed, designed, simulated, and the results are analyzed considering dead zone as a constraint. Design of pass transistor logic network plays a part in the diminution of the dead zone. Further, an improved design of CP is proposed to reduce current mismatch. It is achieved by placing the single ended differential amplifier in current– voltage feedback configuration which offers high output impedance. Simulations are performed using T-SPICE, implemented in IBM 0.13  $\mu\text{m}$  technology under 1.3 V power supply. Results show that the modified PFD design has a dead zone of 0.3 ns and the current mismatch decrements to 0.1  $\mu\text{A}$  in an improved CP design.

## III. EXISTING METHOD

In PLL, The CP is nothing but the switching circuit used to generate dc voltages that are higher than the standard power supply. It is used to sink and source current into a loop filter based on the output of the phase frequency detector. The CP converts the up and down signal pulses from PFD into current pulses as there are capacitors in the loop filter. These current pulses change voltage drop on the loop filter impedance that is also the VCO control voltage. The CP design is mainly used to avoid the charge sharing effect. A Loop-filter is nothing but the Low Pass Filter (LPF) integrates error current to generate VCO control voltage and suppresses the noise and unwanted phase detector outputs. The filter shown in Figure 5 alters the ability of the loop to change frequencies instantly. If the filter has low cut off frequency, then the changes in tune voltage take place slowly. The VCO is unable to vary its frequency as soon, and this is due to the slow changes in the voltage level.

Another important module in designing PLL is the VCO. A type of VCO called Ring Oscillator (RO) consists of some delay stages with a feedback system and to achieve the oscillation, the phase shift of  $2\pi$  and unity voltage gain is required at the oscillating frequency. Design of the Current starved VCO is similar to that of RO. From the schematic circuit of the VCO in Figure 3, the MOSFET M2 and M3 acts as an inverter, where M1 and M4 promote as current sources. The current sources M1 and M4 limit the current availability of the inverter M2 and M3. The MOSFET M5 and M6 illustrate each inverter/current source stage. The upper PMOS transistors are attached to the gate M6, and the source voltage is applied to the gates of all the lower NMOS transistors. In PLL, the reference signal and the signal from the VCO are connected into the PFD circuit. The result of the PFD circuit is connected to the CP.

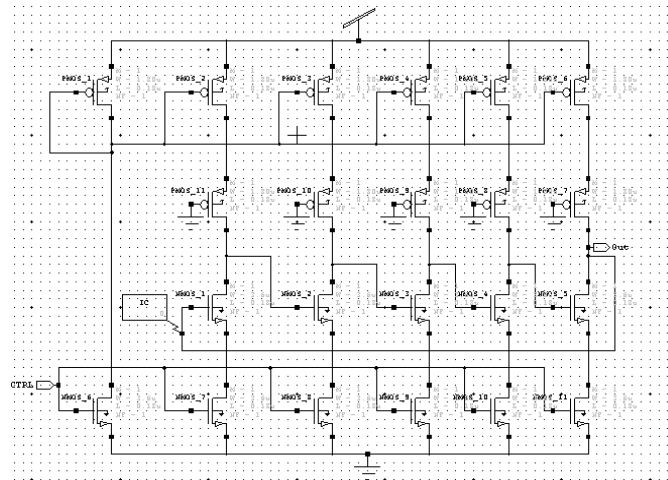


Figure 2. Current starved VCO

PLL operation is repeated with every external input pulse so that the feedback VCO and the external input clock are matched, the circuit then locks onto itself within a narrow frequency band. If the clock of entry varies slightly, the PLL frequency does not change. This narrow frequency band is the dead zone of the PPFD. Within this zone, the VCO signal and reference signal are so close in-phase that there are no correction pulses out of the PPFD circuit. Once the phase shifts out of this frequency band, the PPFD is correcting again. As the PLL design is functioning properly, it is extended further by connecting with Frequency divider (FD) blocks. The FD performs the frequency division by a factor of 2 which is illustrated in Figure 4 where it will divide the phase of the input signal by 2 as well.

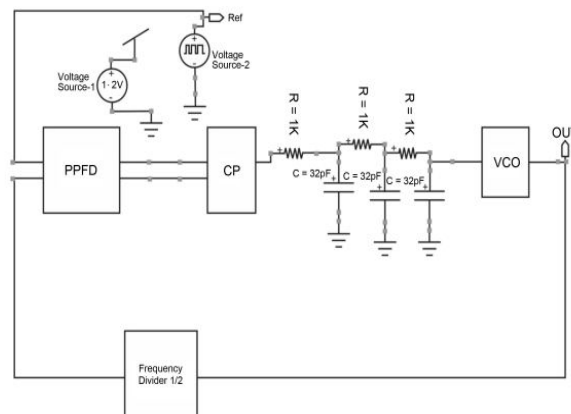


Figure 3. A PLL Design with FD/2.

The overall PLL design is presented with every external input pulse so that the feedback VCO and the external input clock are matched, the circuit then locks onto itself within a narrow frequency band. If the clock of entry varies slightly, the PLL frequency does not change. This narrow frequency band is the dead zone of the PPFD. Within this zone, the VCO signal and reference signal are so close in-phase that there are no correction pulses out of the PPFD circuit. Once the phase shifts out of this frequency band, the PPFD is correcting again. As the PLL design is functioning properly, it is extended further by connecting with Frequency divider (FD) blocks. Here, the transistors in DFF helps to eliminate the short-circuit power during the FD by-2 operation.

**Disadvantages:**

- Due to Multi-stage VCO, the number of MOSFET's are increasing.
- Higher power consumption.
- Higher delay.



#### IV. PROPOSED METHOD

The design and implementation of an LC Voltage Controlled Oscillator (LCVCO) play a crucial role in achieving stable and efficient performance in PLLs, which are essential for a wide range of modern communication and digital applications. LCVCOs offer advantages such as low phase noise, broad tuning range, and high linearity, making them ideal for frequency synthesis and clock generation tasks. By optimizing the design and implementation of LCVCOs, engineers can improve the overall efficiency and performance of PLL-based systems across various technology nodes.

#### LCVCO:

In this, we confine ourselves to designing and implementing the CMOS cross coupled oscillator as shown in figure 5. The purpose of this paper is to get a clear understanding of the important analysis and parameters that are needed to be measured before actually implementing the entire VCO core. The circuit schematic of the proposed LC VCO is shown in Figure 5. The topology of proposed VCO is based on complementary NMOS and PMOS cross-coupled differential LC structure (NP-pair) with NMOS tail current source. This structure, once optimized, performs better than other common VCO topologies, in terms of the phase noise value and the overall power consumption under low power levels.

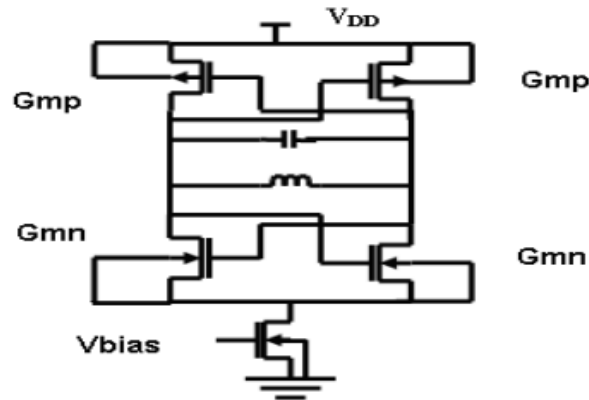


Figure.4 Simple CMOS complementary -Gm oscillator.

The tank amplitude of an NP-pair topology is twice that of an N-pair or a P-pair only topology for a given current. The circuit can be optimized to have more symmetry in the output waveform, which leads further phase noise reduction. The transconductances of the NMOS and PMOS switching devices have been set approximately equal to obtain symmetry in the output waveforms. Asymmetry of the output waveforms is the cause of the additional up-conversion noise. However, with increasing tail-current from a low power supply voltage the NP-pair goes into the voltage-limited region quickly due to reduced voltage headroom. So, if power dissipation is not a concern, N-pair or P-pair only topology can be used for better phase noise performance.

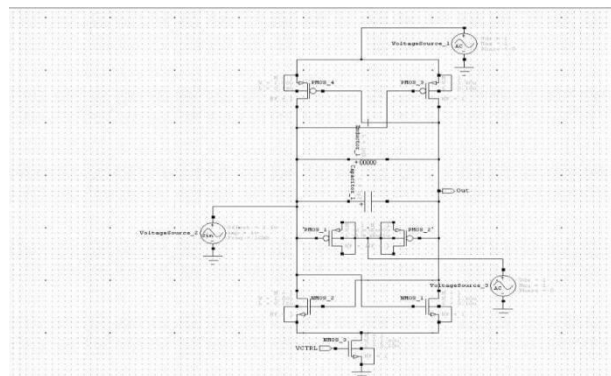


Figure.5 LCVCO Design

The values of the on-chip inductors, varactors and the sizes of cross-coupled NMOS and PMOS FET pairs are chosen in accordance to the oscillation condition and frequency tuning range. In particular, the inductance was increased as large as possible for low power consumption while maintaining a suitable frequency tuning range.

In the sub threshold regime, also known as weak inversion, the drain current depends exponentially on the gate source voltage  $V_{gs}$ . This latter is slightly below the transistor’s threshold voltage  $V_{th}$  and the concentration of carriers is very low but not negligible. In this work, an NMOS cross-coupled topology using the adaptive body biasing technique has been selected. Figure 6 presents the detailed schematic of the VCO topology. It is composed by an LC resonator, also referred as LC-tank, an adaptive body biasing circuit (M3 and M4) and an NMOS cross-coupled pair (M1 and M2) biased in the sub threshold region. This pair is used to provide the negative conductance and to overcome the tank loss.

**Advantages:**

- Lower Power Consumption
- Lower Delay
- Lesser MOSFET utilization

**V.SIMULATION RESULTS**

There are many phases or progressions of a design. A common term you will hear when working with a Designer is “Schematic Design”. This phase is early in the design process. Schematic Design establishes the general scope, conceptual ideas, the scale and relationship of the various program elements. The primary objective of schematic design is to arrive at a clearly defined feasible concept based on the most promising design solutions. First step is to double click on the icon of s-edit on the desktop. A new window will open.

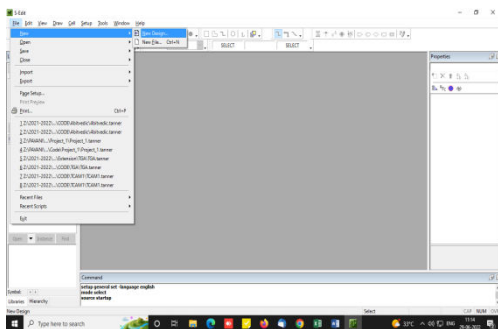


Figure 6. Creating new Design.

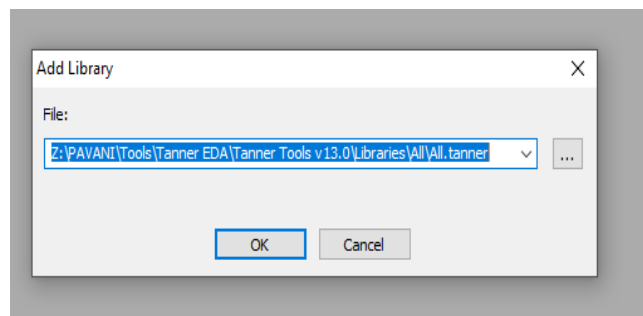


Figure 7. Add libraries.

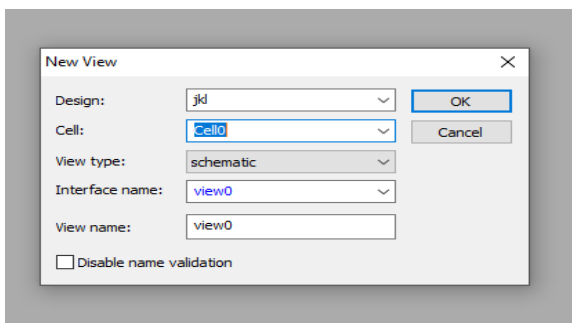


Figure 8. Create cell.

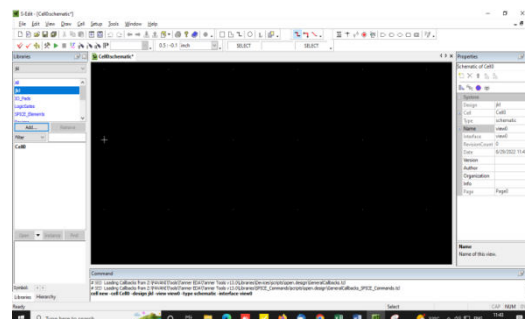


Figure 9. Cell Schematic.

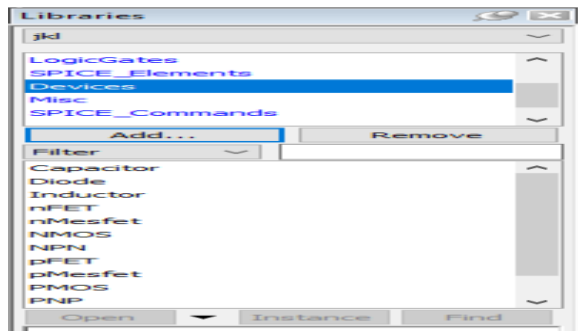


Figure 10. Select Devices.

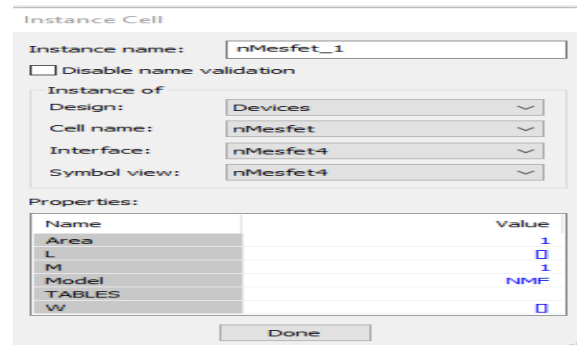


Figure 11. Instances cell.

Now, after completed these steps, you should give the supply (VDD) & ground (GND).

For that Go to libraries >> MISC >>Select VDD and GND.

Now create a source of VDD. For that go to libraries >> spice\_element >> and then select voltage source of type DC . we can give any value in vdd .lets take vdd =5v.

**Pre layout simulation:**

After schematic design check the design, it is match with the specification required or not . Then we need to simulate the design which is called Pre layout simulation.

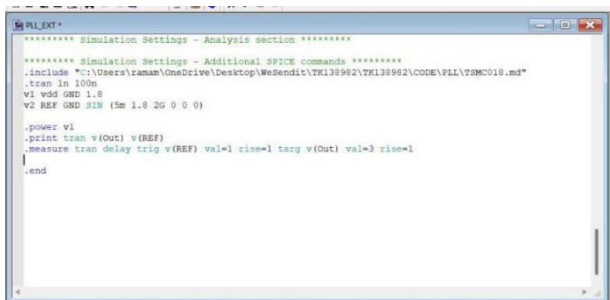


Figure 12. Reference Input.

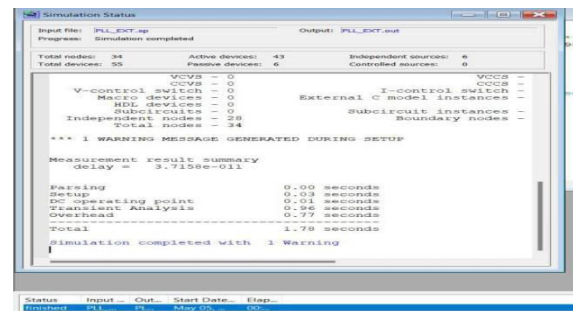


Figure 13. Simulation Status

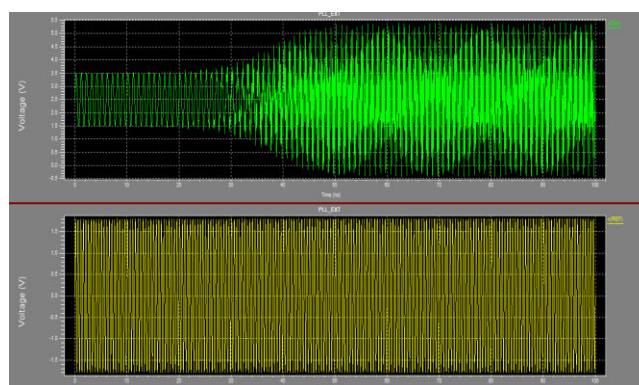


Figure 14. PLL Waveform



**Performance Table:**

	<i>Power</i>	<i>Area</i>	<i>Delay</i>
<b>PLL_CSVCO</b>	3.056282e-003	58	1.1833e-010
<b>PLL_LCVCO</b>	9.179639e-004	43	3.7158e-011

**VI.CONCLUSION**

In conclusion, the design and implementation of an LC Voltage Controlled Oscillator (LCVCO) for Phase-Locked Loop (PLL) systems offer a promising approach to enhancing performance and efficiency. The LCVCO provides critical capabilities such as low phase noise, broad tuning range, and high linearity, which are essential for reliable frequency synthesis and clock generation. Through meticulous design and optimization, the proposed LCVCO has demonstrated efficiency in terms of power and delay, which are crucial metrics for modern PLL applications. The results indicate that the LCVCO effectively contributes to the overall improvement of PLL-based systems, supporting their application in a wide range of communication and digital technologies. This work paves the way for further advancements in PLL design, promoting the development of energy-efficient and high-performance digital systems.

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