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# A Novel Methodology Based On Matrix Converter for Voltage and Current Source Inverters

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Abstract— A new Pulse Width Modulation algorithm is presented which derives from ac-ac matrix converter theory. It can be used to implement either a Voltage Source or a Current Source Inverter, using only conventional bridge topologies. The resultant modulation strategy produces minimum low order ac harmonics, yet it is readily capable of being computed on-line in a single switching cycle by a low-cost microprocessor at switching frequencies of up to several kHz. The new algorithm also allows independent control of the output waveform magnitude and frequency, and provides for a wide range of operation without changing the switching frequency. Furthermore, the strategy guarantees dc source current continuity for the Current Source Inverter topology, which still allowing the ac output current to step change to a new value within one switching cycle. The paper presents theory, simulation results and experimental results showing the new algorithm in operation.

Keywords— Matrix Converter, Voltage Source Inverter, Current Source Inverter, PWM, Low order Harmonic.

## I. INTRODUCTION

In the last decade, considerable research effort has gone into the development of Pulse Width Modulation (PWM) strategies for Voltage Source Inverters (VSI) and Current Source Inverters (CSI) to achieve the maximum possible range of output voltage or current whilst satisfying the conflicting requirements of minimum low order harmonics (achieved by increased switching times) and minimum switching losses (achieved by reducing the number of switch transitions per second). The algorithms that have resulted can be broadly grouped into one of two categories, viz. - Variations and developments of the standard "sinetriangle" PWM algorithm. This category includes regular symmetric and regular asymmetric PWM, which were developed for implementation using digital microprocessors.

- Various harmonic elimination and optimization strategies, which implement a PWM strategy optimized for a specific goal. The elimination of low order harmonics is a common objective. Many of the PWM algorithms that have been proposed are quite computationally intensive (especially the harmonic elimination techniques), and cannot be computed on-line within one switching cycle. This is an increasing limitation as switching frequencies increase with new power electronic devices. A common solution to resolve the conflicting requirements of increased PWM switching speeds and more sophisticated control requirements is to store a number of pre-calculated optimal switching tables in computer memory. This approach generally has resolution limitations, and requires techniques such as sub-optimal interpolation and "gear ratio" changing to provide an extended or more accurate range of inverter operation. Irrespective of the PWM algorithm that is used, inverters used in variable speed drive applications are required to produce a sinusoidal variable frequency output voltage or current with adjustable output magnitude, preferably whilst generating a minimum of low order harmonics. In many applications, the output waveform frequency and magnitude are linked by a fixed relationship. For example, Voltage Source Inverters usually are arranged to produce an output voltage with a constant voltage/frequency ratio, to maintain constant magnetizing current in the driven induction motor. However, additional output voltage magnitude control may be sometimes needed to compensate for varying dc voltage, non-linear machine magnetizing input characteristics, etc. As a further example, Current Source Inverters have the additional requirement to maintain



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current continuity from the dc current source, which places constraints on the PWM algorithm that can be implemented. Modulation strategies which are computed off-line and interpolated on-line from stored tables generally cannot accommodate these additional control requirements. In a recent research it is showed how ac-ac matrix converter theory could be adapted to implement an PWM controlled rectifier bridge with minimum low order harmonics, controllable input power factor, direct on-line computation of the required switching intervals, and no increase in the number of switches in the bridge. This paper extends this work to use ac-ac matrix converter theory to achieve substantially improved control of standard Voltage and Current Source Inverter bridge topologies, without requiring additional switching devices. The result is a VSI/CSI modulation strategy which produces minimum low order ac harmonics and is readily capable of being computed online in a single switching cycle by a low-cost microprocessor. The algorithms derive the required switching intervals directly from cosine tables, which can be stored to any desired level of angular resolution, and they can independently adjust the magnitude and frequency of the output waveform. Furthermore, since the modulation functions are defined directly in terms of the output voltage/current phasor magnitude and angle, the modulation strategy can be readily adapted to fieldorientated control drive applications. Finally, the CSI algorithm guarantees that dc source current continuity is always maintained, whilst allowing the ac output current to step change within one switching cycle. Any current shoot-through that is required is implicitly generated by the computation algorithm

#### II. SUMMARY OF MATRIX CONVERTER THEORY

Matrix converters were first proposed in 1976, and were then investigated as a generalized high frequency ac-ac switching matrix in 1981. A more recent investigation showed how the addition of third harmonic voltage components can extend the transfer ratio of a matrix converter to 0.866, the theoretical maximum that can be achieved.. The general topology of a three phase ac-ac matrix converter is shown in Figure 1, and consists of nine bi-directional switches arranged in a matrix so that any input phase can be connected to any output phase. In principle, for a given set of input phase voltages, any desired set of output voltages can be synthesized by suitably toggling the matrix.



Figure 1 Topology of general AC-AC Matrix Converter

Mathematically, the fundamental requirement of the bridge is given a set of 3 phase input voltages

$$\mathbf{V}_{i(t)} = \begin{pmatrix} \mathbf{V}_{i1}(t) \\ \mathbf{V}_{i2}(t) \\ \mathbf{V}_{i3}(t) \end{pmatrix} = \begin{pmatrix} \mathbf{V}_{i} \cos(\omega_{i}t + \theta_{i}) \\ \mathbf{V}_{i} \cos(\omega_{i}t + \theta_{i} - \frac{2\pi}{3}) \\ \mathbf{V}_{i} \cos(\omega_{i}t + \theta_{i} + \frac{2\pi}{3}) \end{pmatrix}$$
(1)

determine the switching function M(t) which will produce the set of three phase output voltages:

$$V_{o}(t) = M(t) \cdot [v_{i}(t)] = \begin{pmatrix} V_{o} \cos(\omega_{o}t + \phi_{o}) \\ V_{o} \cos(\omega_{o}t - \frac{2\pi}{3} + \phi_{o}) \\ V_{o} \cos(\omega_{o}t + \frac{2\pi}{3} + \phi_{o}) \end{pmatrix}$$
(2)

Considering the initial output phase equal to zero then venturini shows that in order to have max gain.  $(q_{max}=.86)$  following equation (3) should be considered :

$$v_{o}(t) = \begin{pmatrix} v_{a}(t) \\ v_{b}(t) \\ v_{c}(t) \end{pmatrix}$$
  
= 
$$\begin{pmatrix} V_{o} \cos (\omega_{o}t) + V_{i}/4 \cos(3\alpha\omega_{i}t) - V_{o}/6 \cos (3\omega_{o}t) \\ V_{o} \cos (\omega_{o}t + \frac{2\pi}{3}) + V_{i}/4 \cos(3\alpha\omega_{i}t) - V_{o}/6 \cos (3\omega_{o}t) \\ V_{o} \cos (\omega_{o}t + \frac{4\pi}{3}) + V_{i}/4 \cos(3\alpha\omega_{i}t) - V_{o}/6 \cos (3\omega_{o}t) \end{pmatrix}$$
  
(3)

 $q = q_r q_{max} = V_o / V_i$ 

Where  $q_r$  is the relative voltage gain. It is computed in such a way that the output voltage is always constant. In the same way, the input currents are also shown by expression (4):



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$$\begin{split} I_i(t) &= M^T(t) . [I_o(t)] = q \cos\theta_o / \cos\theta_i \quad I_o(K) \quad (4) \\ \text{Where K is a matrix defined as :} \end{split}$$

$$\begin{pmatrix} \cos (\alpha \omega_i t + \varphi_i) \\ \cos (\alpha \omega_i t + 2\pi/3 + \varphi_i) \\ \cos (\alpha \omega_i t + 4\pi/3 + \varphi_i) \end{pmatrix}$$

In order to obtain matrix [M] which is known as modulation matrix the following equations (4) must be solved and that the following active power balance equation must be satisfied with,

$$q[\cos(\omega_{o} t)] = [M_{11} M_{12} M_{13}] \begin{pmatrix} \cos(\beta\omega_{i} t) \\ \cos(\beta\omega_{i} t + 120) \\ \cos(\beta\omega_{i} t + 240) \end{pmatrix}$$
(5)

where  $\beta = V_0/V_i \{1 - \frac{\tan(input \ pf \ angle)}{\tan(output \ pf \ angle)}\}$ with  $\omega_m = (\omega_0 + \alpha \omega_i)$  will results in :

 $q[\cos(\omega_{o}t)] = \frac{1}{2} \{\cos(\omega_{o})t + \cos(2\alpha\omega_{i} + \omega_{o}) t + \cos(\omega_{o})t + \cos[(2\alpha\omega_{i} + \omega_{o}) t + 240] + \cos(\omega_{o})t + \cos[(2\alpha\omega_{i} + \omega_{o}) t + 120] \}$ 

 $= 3/2 \cos(\omega_0 t)$  (6)

which simplifies to:

$$\begin{split} M_{11}^{+} &= \frac{2q}{3} \cos(\omega_{o} + \alpha \omega_{i}), \\ M_{12}^{+} &= \frac{2q}{3} \cos(\omega_{o} + \alpha \omega_{i} + 120), \text{ and} \\ M_{13}^{+} &= \frac{2q}{3} \cos(\omega_{o} + \alpha \omega_{i} + 240) \end{split}$$

But with  $\omega_m = (\omega_o - \alpha \omega_i)$  results simplifies to :

$$M_{11}^{-} = \frac{2q}{3} \cos(\omega_{o} - \alpha \omega_{i}),$$
  

$$M_{12}^{-} = \frac{2q}{3} \cos(\omega_{o} - \alpha \omega_{i} + 120), \text{ and}$$
  

$$M_{13}^{-} = 2q/3 \cos(\omega_{o} - \alpha \omega_{i} + 240)$$

Since the element (  $0 \le m_q \le 1$ ), if the constraint below applied:

 $\sum_{i=1}^{3} mij = 1$ , i = 1, 2, and 3. (7)

For unity power factor :  $m_{ij} = \frac{1}{2} [m_{ij}^{+} + m_{ij}^{-}]$ i = 1,2 and 3

The same procedure is applied for the second row of matrix (2) and has to satisfy (4), matrix M can be represent by:

$$\begin{split} m_{Kj} &= 1/3 \, \left[ 1 + q \left[ \begin{array}{c} \cos(\omega_o + \alpha \omega_i) \, t + \cos(\omega_o - \alpha \omega_i) \, t + \\ \left( \begin{array}{c} \omega_o - \alpha \omega_i \end{array} \right) t + \cos(\omega_o - \alpha \omega_i) \, t \end{array} \right] \end{split}$$

 $m_{Kj}\!=1/3\;[1\!+2q[\;\cos(\;\omega_{o}\;)\;t_{j}\;\;x\;\cos\left(\alpha\omega_{i}\right)t_{k}\;]].$ 

Since  $q = V_{oj (Max)} / V_{inK(Max)}$  then,

$$m_{Kj} = \frac{1}{3} \{1 + 2V_{oj(Max)} / V_{inK(Max)} [\cos(\omega_o)t] \times \cos(\alpha \omega_i) t] \}$$
(8)

Which is:  $m_{Kj} = t_{Kj}/Ts = \frac{1}{3} \{1+2 \ (V_{oj} \ x \ V_{inK} \ ) \ /V_{inK \ (Max)\}}^2 \}$ Where :  $V_{oj} = V_{oj(Max)} \ [ \ \cos(\omega_o) \ t \ (i-1) \ x \ 2\pi/3 \ ],$ i=1,2,3 and j=a,b,c.

$$\begin{array}{l} V_{inK} = V_{inK(Max)} \ x \ cos \ (\alpha \omega_i \ ) \ t \ , \\ m_{i \ j} = \ t_{ij} \ / \ T = [1 + (2 \ V_{inK} \ V_{oj} \ ) / \ V_i^2] \\ i = A,B,C \ and \ j = \ a,b,c \end{array} \tag{(*)}$$

# III. REDUCTION OF MATRIX CONVERTER TO VOLTAGE SOURCE INVERTER.

To operate a matrix converter as a Voltage Source Inverter, the input frequency  $\omega_i$  is set to zero, and the input offset angle  $\theta_i$  is set to zero. The three phase input voltages (1) then become:

$$\begin{array}{l} \begin{pmatrix} V_{i1}(t) \\ V_{i2}(t) \\ V_{i3}(t) \\ \end{pmatrix} &= \begin{pmatrix} V_i \\ -V_i/2 \\ \end{pmatrix} \\ -V_i/2 \\ \end{pmatrix}$$

Furthermore, current continuity restrictions **on** the output side of the converter mean that one switch of the pairs (S1,S2), (S4, S5), (S7,S8) must be on at any time. Consequently the reverse conduction section of each of these six "bi-directional" switches can be deleted. This reduction can be illustrated by considering the conditions of a forward current flowing out through output terminal  $V_{o1}$ . If switch S1 is off, the reverse diode across switch S2 will conduct the output current. When switch S1turns on, it will immediately take over from the S2 reverse diode, and conduct the output current. Thus there is no need for the reverse conduction capability of S1 to be controlled and the reverse conduction active section of this switch can be deleted.

Similar considerations apply to all six switches, and hence the reduction to the conventional VSI bridge topology as shown in Figure 2 is achieved. The converter output voltage magnitude can now be expressed in terms of the actual dc input voltage  $V_{dc}$ . rather than the original ac input waveform magnitude Vi, as follows:

For 
$$\theta_i = 0$$
,  $V_{dc} = V_{i1} - V_{i2} = 1.5$  Vi. (10)

Since the maximum output voltage that can be achieved from a matrix converter is 0.866Vi, the VSI maximum output voltage magnitude becomes:



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switches S2,S5 and S8 to conduct for the remainder of

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 $V_o (max) = 0.866 V_{dc} / 1.5 = 1.15 V_{dc} / 2.$ 

This compares very favorably with conventional high performance PWM algorithms



Figure 2: Reduction of general AC-AC Matrix Converter Bridge to conventional Voltage Source Inverter Topology.

The matrix converter voltage transfer relationship (4) now reduces to:

$$\begin{pmatrix} V_{01}(t) \\ V_{02}(t) \\ V_{03}(t) \\ (11) \end{pmatrix} = \begin{pmatrix} m_{11}(t) & \{1 - m_{11}(t)\} \\ m_{21}(t) & \{1 - m_{21}(t)\} \\ m_{31}(t) & \{1\} \end{pmatrix} \cdot \begin{pmatrix} V_i \\ m_{31}(t) \end{pmatrix} V_i/2$$

And the low frequency modulation functions (5) reduce to:

$$m_{11}(t) = m\{\frac{1}{\sqrt{3}}\cos(2\omega o t) - \frac{1}{6\sqrt{3}}\cos(3\omega o t) + \frac{1}{6}\} + \frac{1}{3}$$

$$m_{21}(t) = m\{\frac{1}{\sqrt{3}}\cos(2\omega o t - \frac{2\pi}{3}) - \frac{1}{6\sqrt{3}}\cos(3\omega o t) + \frac{1}{6}\} + \frac{1}{3}$$

$$m_{31}(t) = m\{\frac{1}{\sqrt{3}}\cos(2\omega o t + \frac{2\pi}{3}) - \frac{1}{6\sqrt{3}}\cos(3\omega o t) + \frac{1}{6}\} + \frac{1}{3}$$

Where m= modulation ratio (0<m<1) (12)

Under the significance of :

-  $\omega_{o}$ ,  $\theta_{i}$ ,  $\theta_{o}$  equal to zero.

- unity power factor irrespective to output power factor.

- calculate only  $m_{11}(t)$ ,  $m_{21}(t)$  and  $m_{31}(t)$  because of current continuity consideration.

The three expressions in (12) above define the fractional on-time of the three upper switches S1, S4 and S7 in the VSI bridge shown in Figure 2, leaving the lower leg each switching time period  $\Delta t$ . These expressions require three table lookups, three multiplications and three additions for their computation and this can be readily achieved within one switching cycle using a microprocessor with hardware multiply facility. The cosine lookup tables can be stored to any desired degree of accuracy, say to  $0.5^{\circ}$  for normal applications, and even only an 8 bit multiply allows for 0.5% modulation depth step changes. Hence the new algorithm allows for very fine control of output frequency (i.e. the angular step moved at each  $\Delta t$  period) and voltage magnitude, without requiring multiple lookup tables or variable switching periods.

The algorithm offers additional benefits since the modulation functions are defined directly in terms of output voltage magnitude and cosine angle. For example, it is straightforward to adjust the modulation ratio at each switching period to compensate for a changing dc input voltage, so that constant ac output voltage is achieved. Alternatively, the bridge can switch to any arbitrary output voltage magnitude and phasor angle within one switching period, and this has application for field orientated drive applications. Many other novel applications are also feasible.

# IV. REDUCTION OF MATRIX CONVERTER TO CURRENT SOURCE INVERTER.

To operate a matrix converter as a Current Source Inverter, the converter is operated in reverse; with the output frequency  $\omega_o$  set to zero and the output offset angle  $\theta$ , set to  $30^\circ$ . However, to maintain consistency with the earlier equations, the term "output" will be used to refer to the dc source current side, and the term "input" will be used to refer to the resultant ac current side. Under these conditions, with a current source connected to the "output" as shown in Figure3, the "output" currents become:

Since  $I_{02}(t)$  is zero, (instantaneously and on average, from current continuity considerations), switches S4,S5,S6 from Figure 1 are not required. Furthermore, the remaining switches are constrained by current continuity considerations so as to never short circuit the "input" terminals. Consequently they can only conduct current from the current source in the forward direction, so the reverse conduction switch sections and reverse diodes are not required. Hence the reduction to the conventional



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Current Source Inverter topology as shown in Figure 3 is achieved.

The converter "input" current magnitude can now be expressed in terms of the actual dc source current  $I_{dc}$ , as follows:

For 
$$\theta_{o} = 30^{\circ}$$
,  $I_{dc} = I_{o} \cos (30^{\circ})$   
(14)

From power balance considerations, at unity "input" and "output" power factor, the maximum current transfer ratio that can be achieved is  $I_i = 0.866 I_o$ , and the CSI maximum "input" current magnitude becomes:

 $I_i(max) = 0.866 \quad I_{dc}/\cos(30^0) = I_{dc}$ (15)

i.e. the peak value of the ac "input" current equals the dc source current.



Figure 3: Reduction of general AC-AC Matrix Converter Bridge to conventional Current Source Inverter Topology.

This is the maximum value that can ever be achieved under any CSI modulation strategy. The matrix converter current transfer relationship (8) now reduces to:

$$\begin{pmatrix} I_{11}(t) \\ I_{12}(t) \\ I_{13}(t) \\ (16) \end{pmatrix} = \begin{pmatrix} m_{11}(t) & m_{31}(t) \\ m_{12}(t) & m_{32}(t) \\ (1 - m_{11}(t) - m_{12}(t)) & (1 - m_{31}(t) - m_{32}(t)) \end{pmatrix} \begin{pmatrix} I_{dc} \\ -I_{dc} \\ -I_{dc} \end{pmatrix}$$

and the low frequency modulation expressions (16) reduce to:

$$m_{11}(t) = m\{\frac{1}{2}\cos(\omega t) + \frac{7}{36}\cos(2\omega t) - \frac{1}{36}\cos(4\omega t)\} + \frac{1}{3}$$

$$m_{21}(t) = m\{\frac{1}{2}\cos(\omega t - \frac{2\pi}{3}) + \frac{7}{36}\cos(2\omega t + 2\pi 3)\} + 13$$

$$m_{31}(t) = m\{-\frac{1}{2}\cos(\omega t) + \frac{7}{36}\cos(2\omega t) - \frac{1}{36}\cos(4\omega t)\} + \frac{1}{3}$$

$$m_{32}(t) = m\{-\frac{1}{2}\cos(\omega t - \frac{2\pi}{3}) + \frac{7}{36}\cos(2\omega t + \frac{2\pi}{3})\frac{1}{36}\cos(4\omega t - \frac{2\pi}{3}) + \frac{7}{36}\cos(2\omega t + \frac{2\pi}{3})\frac{1}{36}\cos(4\omega t - \frac{2\pi}{3}) + \frac{1}{3}$$
(17)

Under the significance of :

-  $\omega_0$ ,  $\theta_i$ , equal to zero and  $\theta_0$  equal to 360°

- unity power factor
- -output power factor.

- calculate only  $m_{11}(t)$  ,  $m_{21}(t),\,m_{31}(t)$  and  $m_{32}(t)$  because of current continuity consideration.

Similar to the VSI implementation in section III above, the four expressions in (17) define the fractional on-time of the four switches S1, S2, S7 and S8 in the CSI bridge shown in Figure 3, leaving switches S3 and S9 to conduct for the remainder of each switching period  $\Delta t$ . These expressions require four table lookups, four multiplications and four additions for their computation. The application comments made with regard to the VSI implementation earlier also apply to the implementation of the CSI algorithm using the above modulation expressions. The above development requires that the "input" power factor is set to unity, but this will not occur in a practical situation where the converter is used for a variable speed drive application. The following argument shows that this does not affect the validity of the algorithm.

Assume that the "input" voltages are sinusoidal of the form shown in (l), where  $\theta$ i is the phase angle between the target "input" currents and the "input" voltages, but is NOT used to vary the  $\beta$  terms in (5) ( $\theta$ i will usually be somewhat greater than 180° for normal CSI operation to maintain reverse power flow through the converter).

From(4)  $Vo_1(t) = m_{11}(t)*V_{11}(t) + m_{12}(t).V_{12}(t) + m_{13}(t).V_{13}(t)$  (18)  $Vo_3(t) = m_{31}(t)*V_{11}(t) + m_{32}(t)*V_{12}(t) + m_{33}(t).V_{13}(t)$  (19)

and Vm(t) is not required since switches S4, S5 and S6 have been deleted. Substituting for  $V_{ix}(t)$  from(1) m  $_{yy}(t)$  from (17) and invoking current continuity considerations gives, after some manipulation:

$$V_{01}(t) = m\{\frac{3}{4}\cos\theta i + \frac{7}{24}\cos(3\omega t + \theta i) - \frac{1}{24}\cos(3\omega t - \theta i)\}$$



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 $V_{01}(t) = m\{\frac{3}{4}\cos\theta i + \frac{7}{24}\cos(3\omega t + \theta i) - \frac{1}{24}\cos(3\omega t - \theta i)\}$ (20)
(20)

and the dc source voltage  $V_d$ , becomes:

 $V_{dc}(t) = V_{01}(t) - V_{03}(t) = 1.5m .cos\theta_i .V_i$  (21)

Power balance through the converter is therefore satisfied because:

 $P_{in} = 3/2 V_i I_i \cos\theta_i = 1.5 V_i m I_i \cos\theta_i = V_{dc} I_{dc} = P_{out} (22)$ and the CSI algorithm is valid even if the input power factor is not unity. The modulation expressions developed in (17) above are not as intuitively obvious as those developed for the VSI implementation (12), since they include "input" third harmonic voltage terms which have appear to have no direct relevance to the generation of the required "input" currents. Mathematically, these terms are required to satisfy the existence constraint (7) of the modulation terms. Physically, they can be explained by considering the duality of voltages and currents on either side of the converter. While the CSI has the prime objective of converting a dc source current into ac load currents, it also converts the associated dc source voltage into an ac load voltage. Hence the additional terms in (17) are explained. This new CSI algorithm offers the particular benefit that the "input" current magnitude can be varied within one switching period, without changing the dc source current. Any "excess" dc source current shoots-through the bridge implicitly without affecting the ac current. This is a major advantage over conventional Current Source Inverters, particularly for field orientated drive applications. Essentially, the algorithm can produce an output current phasor of arbitrary magnitude and phase angle within one switching period, provided the maximum phasor magnitude does not exceed the dc source current.

### V. SIMULATION RESULTS

The new algorithms have been extensively tested using simulated physical models of the converter topologies under consideration. These models represent the VSI and the CSI bridges as a set of ideal switches, which are coupled into differential equations representing the load impedances, source impedances and any input or output filters as a network of resistances, inductances and capacitors. The converter switching algorithm to be investigated is then implemented as discrete switch transitions at the required time intervals which cause discontinuities to the voltages or currents applied to this network. The response of the network is calculated by numerical integration of the differential equations, and produces a simulated output which is very close to that which would be produced by a physical bridge (since a real converter operates its switches in exactly the same

way). The only differences arise from non-linearity in the real load/source impedances and filter networks, and the non ideal switching characteristics of the switching devices themselves.

In the simulation results that follow, all switched waveforms (i.e. output voltages and input currents) have been passed through a low pass RC filter with a time constant of 500 µsec, to emphasize their low frequency performance. Harmonic analysis has been done after passing the raw switched waveform through **a** low pass RC filter with a time constant of 50 µsec, to minimize aliasing effects. All simulations have been computed at **a** fixed switching frequency of 2 kHz. All voltages and currents are in per unit representation.

#### A. VSI SIMULATION RESULTS

Figure 4(a) presents the output line-to-line voltage produced by the converter operating under the new VSI algorithm at a modulation depth of 0.8 and an output frequency of 30 Hz. Figure 4(b) presents the spectrum of this output voltage. As predicted, there are no significant low order harmonic components present.



Figure 4: Voltage Source Inverter. Line-Line Output Voltage: -30 Hz Output Frequency, 0.8 Modulation Depth, 2 kHz Switching Frequency.

Figure 5(a) illustrates the inverter response if an output voltage step frequency change from 20 Hz to 40 Hz is suddenly demanded. Figure 5(b) illustrates the inverter response to a step change in modulation depth from 0.5 to 1. In both cases the response is immediate, and, in the case of the frequency change, smooth.



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(a) 20 Hz to 40 Hz change in  $f_{\rm o}$  (b) 0.5 to 1.0 modulation change

Figure 5: Voltage Source Inverter .Line-Line Output Voltage:-Step Output Frequency and Modulation Changes, 2 kHz Switching Frequency

Figure 6 illustrates one of the ways in which improved inverter performance can be achieved with the new algorithm. Figure 6(a) shows the effect on the ac output voltage with a substantial 300 Hz ripple imposed on the dc input voltage. Figure 6(b) shows the improvement in ac output voltage that can be achieved if the modulation ratio is adjusted at each switching interval to maintain constant output voltage magnitude despite the changing input voltage.



(a) dc ripple uncompensated compensated

(b) dc ripple

Figure 6: Voltage Source Inverter . Line-Line Output Voltage: -Uncompensated and Compensated response with dc input ripple, 2 kHz Switching Frequency.

#### **B. CSI SIMULATION RESULTS**

Figure 7(a) presents the "output" current produced by the converter operating under the new CSI algorithm at a modulation depth of 0.8 and an "input" frequency of 30 Hz. Figure 7(b) presents the spectrum of this current. Once more, there are no significant low order harmonic components present.



(a) Time Domain Analysis (b) Harmonic

Figure 7: Current Source Inverter."Input" Line Current:-30 Hz Output Frequency, 0.8 Modulation Depth, 2 kHz Switching Frequency

Figure 8(a) illustrates the inverter response to a step change in modulation depth from 0.8 to 0.3. Figure 8(b) illustrates the response if a step change in the ac current phasor angle of  $60^{\circ}$  is demanded. The ac current response is immediate: - any necessary shoot-through of the dc source current through the bridge is implicitly controlled by the switching timing.



(a) 0.8 to 0.3 modulation change (b)  $60^\circ$  angle step change

Figure 8:Current Source Inverter."Input" Line Current:-Step Modulation and Phase Angle changes, 2 kHz Switching Frequency.

#### VI. EXPERIMENTAL VERIFICATION

An experimental controller has been constructed to verify the feasibility of computing the new PWM algorithms in real-time. This controller is based on a HD64180 microprocessor, which programs upto six 16 bit hardware timers at every switching cycle. The HD64180 is an 8 bit



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microprocessor, which is essentially a 9 MHz Z80 equivalent microprocessor with an additional hardware multiply instruction. The PWM algorithm is programmed in the C language. The 16 bit timers are Intel 82C54 Programmable Timers, with a minimum timing resolution of 0.25  $\mu$ sec.

#### A.VSI Experimental Implementation

For the VSI implementation, a 16 bit timer **is** used to generate a master interrupt at 500  $\mu$  sec intervals. This interrupt triggers three one-shot slave timers, whose outputs enable the upper half of the three VSI bridge legs for the one-shot periods (switches S1, S4 and S7). At the end of each one-shot period, the bridge legs fall back to their lower half switch elements (switches S2, S5 and S8 respectively).

Simultaneously, the master interrupt causes the microprocessor to compute the three modulation functions that axe required to achieve the current values of the output voltage phasor magnitude and angle, and preloads the three one-shot slave timers with these results. These values become active at the next master interrupt.

To complete the implementation, the outputs from the slave timers are fed through interface electronics which inserts a cross-over delay between the upper and lower switch pairs of each leg of the bridge as they change state. The output of this interface electronics directly drives the power transistor base drive circuitry.

#### **B.** CSI Experimental Implementation

For the CSI implementation, the controlling 16 bit timer generates a master interrupt at 500 µsec intervals, which triggers two one-shot slave timers. The output of these timers control switches S1and S7. At the end of their respective one-shot periods, the slave timers trigger another set of one-shot timers, whose outputs control switches S2 and S8 respectively. Switches S3 and S9 are turned on at the end of these second one-shot periods to complete the switching period. Similar to the VSI implementation, the master interrupt also causes the microprocessor to compute the four modulation functions that are required to achieve the instantaneous value of current magnitude and phase angle that is required. These values are then preloaded to the slave one-shot timers as the timers commence counting down the last interval that was preloaded. At present, the CSI implementation has only been developed to the stage of generating the drive transistor base signals.

## VI. CONCLUSION

A new Pulse Width Modulation algorithm for both Voltage Source and Current Source Inverters has been presented, derived from ac-ac matrix converter theory. The new algorithm has been shown to have the benefits of

- Minimum low order harmonics.

- High maximum transfer ratio.

- Independent control of output waveform magnitude and phase angle.

- Able to be computed on-line in real-time within one switching cycle.

- fixed switching frequency.

- Instantaneous control of output current magnitude for CSI operation.

The algorithm uses conventional VSI or CSI topologies without requiring additional switch elements. Furthermore, since the modulation strategy is defined directly in terms of the output waveform magnitude and phase angle, it is readily adapted to high performance motor drive applications such as field orientated control.

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