

Multi Level Invertors for Renewable Energy System

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Abstract—The flying capacitor multilevel inverter (FCMLI) is a multiple voltage level Inverter topology intended for high-power and high-voltage operations at low distortion. It uses capacitor, called flying capacitors, to clamp the voltage across the power semiconductor devices. A method for controlling the FCMLI is proposed which ensures that the flying capacitor voltages remain nearly constant using the preferential charging and discharging of these capacitors. A static synchronous compensator (STATCOM) based on seven-level flying capacitor inverters has been proposed. Control scheme for STATOM controllers had been developed and verified in terms of voltage control, power flow control, and power oscillation damping when installed in a renewable energy system. Simulation studies are performed in MATLAB/simulink to validate the efficacy of the control scheme and the FCMLI-based flexible alternating current transmission system (FACTS) controller. The modified PWM technique is used to reduce switching losses. Also the proposed topology can reduce the number of required power switches. The proposed circuit produces high output voltage and lower electromagnetic interference.

Index Terms—FCMLI, multilevel inverter, power oscillation damping, STATCOM

I. INTRODUCTION

THE multilevel inverters have gained considerable interests over the past decade in industries as well as in academia over the multistep inverters and the conventional two-level inverters for high voltage and power applications [1]–[7]. In the multilevel inverters, all the devices are individually controlled and hence can provide better control over voltage magnitude and harmonic suppression. Further, switching each device from a voltage that is a fraction of the total dc-link

voltage avoids the problem of designing the costly and bulky snubber circuits. The term multilevel starts with the three-level inverter. With the increase in levels the synthesized output waveform approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems. Unfortunately, the number of achievable voltage levels is limited due to voltage unbalance problems, voltage clamping requirements, circuit layout, cost and packaging constraints [3].

At present, there are three benchmark multilevel inverter topologies: i) diode-clamped multilevel inverter (DCMLI), ii) cascade H-bridge inverter, and iii) flying capacitor multilevel inverter (FCMLI). DCMLI suffers from the limitations of dc-link voltage unbalance, indirect clamping of the inner devices and multiple blocking voltages of the clamping diodes [3]–[5]. H-bridge cascade inverter has limitations such as, the requirement of large number of inverters to decrease the harmonics and complex dc-voltage regulation loop. It needs separate dc sources for real power conversion and thus has somewhat limited applications. Connecting separate dc sources between two converters in a back-to-back arrangement (e.g., in UPFC) is not possible because a short-circuit will be introduced when two back-to-back converters are not switching synchronously [4]. In this inverter, the switching modulation needs to be optimized for high-performance applications due to a limited combination of switching patterns. Moreover, for reactive power exchange, the power pulsation at twice the output frequency occurring with the dc-link of each H-bridge inverter necessitates over-sizing of the link capacitors [2]–[5].

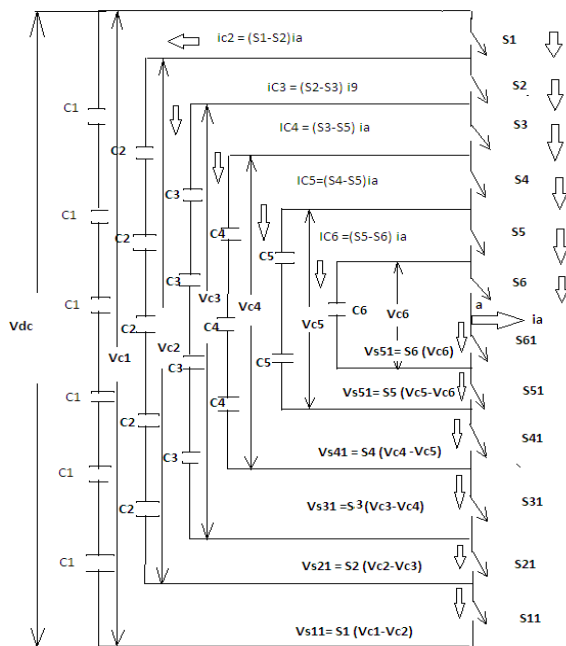


Fig.1. One phase leg of a Seven-level Flying capacitor inverter.

For any initial state of clamping voltages the inverter output voltage is given by

$$V_{an} = S1 (V_{c1} - V_{c2}) + S2 (V_{c2} - V_{c3}) + S3 (V_{c3} - V_{c4}) + S4 (V_{c4} - V_{c5}) + S5 (V_{c5} - V_{c6}) + S6 (V_{c5} - V_{dc}/2). \quad (1)$$

In Fig 1. and in (1), the switching states S1 to S4 take the value 1 if the corresponding switch is conducting and 0 otherwise. Based on (1), the switch combination given in Table 3.1 are used to synthesize the output voltage V_{an} of phase-a with respect to the neutral point n. table I also indicates the states of the flying capacitors corresponding to the switching combinations chosen. The state NC indicates that the capacitor neither charges nor discharges in this mode. The states +and – denote the charging and discharging respectively of the corresponding capacitors. The switching states given are for the positive half cycle of the current waveform (indicated as outgoing current in fig 3.3). the capacitor states (+and -) will reverse for the negative half cycle of the current the output voltage for an n-level inverter can

similarly be defined. In general an n-level FCMLI requires (n-1) pairs of power semiconductor devices and (n-1)*(n-2)/2 clamping capacitors per phase leg in addition to (n-1) main dc bus capacitors provided all the capacitors are of equal value. The number of capacitors can be reduced by sizing the capacitors in a single leg as an equivalent one. The size of the voltage increment between two consecutive clamping legs defines the size of the voltage increment between two consecutive clamping legs defines the size of voltage steps in the output waveform.

The voltage of the innermost clamping leg (e.g., C6 in fig. 3.3) clamping the innermost two devices is $V_{dc}/(n-1)$. The voltage of the next innermost clamping leg will be $V_{dc}/(n-1) + V_{dc}/(n-1) = 2V_{dc}/(n-1)$ and so on. Thus, each extra clamping leg will have the voltage increment of $V_{dc}/(n-1)$ from its immediate inner one. The voltage stress across each capacitor is $V_{dc}/(n-1)$. The voltage levels and the arrangement of the flying capacitors in the FCMOLI structure assure that the voltage stress across each main device is same and is equal to $V_{dc}/(n-1)$.

The line-to-line output voltage of the inverter varies from $+V_{dc}$ to $-V_{dc}$ and has $(2n-1)$ levels in the output, while the phase voltage varies from $+V_{dc}$ to $-V_{dc}$ with n-levels. It can be seen from table 3.1 that the structure offers multiple switching combinations for $V_{ac} = V_{dc}/4, 0$ and $-V_{dc}/4$. Since such

TABLE 1

SWITCH SCHEME FOR ONE PHASE – SEVEN LEVEL FCMLI

Switches	6	5	4	3	2	1	0
S1	1	0	0	0	0	0	0
S2	1	1	0	0	0	0	0
S3	1	1	1	0	0	0	0
S4	1	1	1	1	0	0	0
S5	1	1	1	1	1	0	0
S6	1	1	1	1	1	1	0
S61	0	1	1	1	1	1	1
S51	0	0	1	1	1	1	1
S41	0	0	0	1	1	1	1
S31	0	0	0	0	1	1	1
S21	0	0	0	0	0	1	1
S11	0	0	0	0	0	0	1
vtg	+3v dc	+2v dc	+vdc	0	- vdc	-2v dc	-3v dc

redundancies are available one can choose a preferential switching state that will help in maintaining the capacitor voltages constant. However, the switching combination chosen affects the current rations of the capacitors.

In the other two combinations more than one capacitor are required to be charged or discharged. Therefore, the rms current ratings of the capacitors will necessarily be higher for the single capacitor case than that in the two-capacitor case. Thus optimization of the switching sequence is required, i.e., one that minimizes the capacitor cost and the system losses.

B. Modulation Scheme

Of the various strategies developed to improve the output voltage and reduce the harmonics, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method for an -level inverter, carrier waves are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by their intersections. The output signal of the comparator resembles with the output voltage waveform of the inverter and decides the voltage level that must be generated at a particular instant. For a five-level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter as shown in Fig. 2. The modulating signals of each phase are displaced from each other by 120°. The phase shift angle of the modulating signal, i.e., depends on the application requirements, as discussed Sections III and IV. The modulation index is given by

$$M_a = A_m / 2A_c \quad (2)$$

where A_m is the amplitude of the modulating signal and is that of one carrier wave (peak to peak). Some researches have been reported about the relations between the phases and frequencies of the carrier waves and the shape of the modulating signal to reduce the output voltage harmonics of the multilevel inverters [3], [4], [8], [9].

Here, the carrier waves are taken to have phase displacement of 120° for smallest distortion in the output [3] and their frequency is taken as times to that of the modulating signal, where is a multiple of three so that triplen harmonic cancellation takes place across the three-phase inverter load [9].

The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from +0.98 to -0.98. The amplitudes of the four carrier waves are from 0 to 0.5, 0.5 to 1, in the positive half cycle of the modulating signal, and from 0 to to in the negative half cycle. The modulating signal and four carrier waves are compared in four comparators, on instantaneous basis. The comparator output is when the modulating signal exceeds the carrier wave and zero otherwise. The binary outputs of these comparators are combined arithmetically to produce the levels. The so-generated SPWM output reference signal is shown in Fig. 2(b). This signal resembles the output voltage waveform of the inverter and decides the voltage level, which is to be generated at a particular instant.

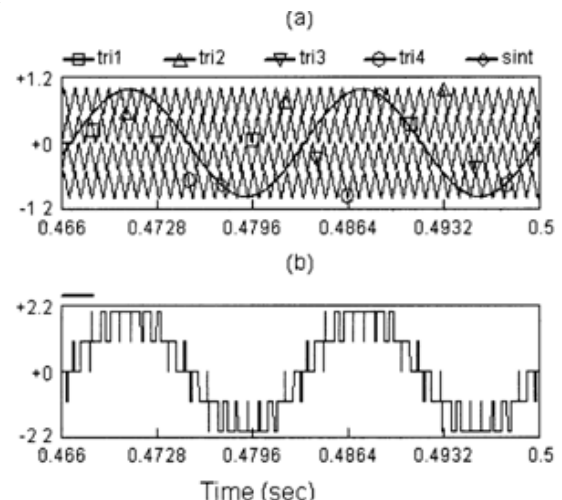


Fig. 2. Modulation scheme. (a) SPWM. (b) Output waveform

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C. Control Strategy for FCMLI In an

In an n -level inverter, there are $(n+1)$ possible switching states that supply the zero voltage level, $n-1$ possible switching states for the next higher level, and so on (excepting the levels $\pm V_{dc}$, which have only one switching combination each). The control scheme proposed here utilizes this feature to readily control the flying capacitor voltages around their reference values while at the same time generating the desired voltage level at the output. The control system block diagram is shown in Fig. 3. The main dc bus voltage is assumed here to be regulated externally as discussed. For a Seven-level inverter with the dc bus voltage of V_{dc} , the reference values of the capacitor voltages VC_6 , VC_5 , and VC_2 (Fig. 1) are $V_{dc}/6$, $V_{dc}/4$, and $3V_{dc}/6$, respectively. The modulation scheme discussed defines the voltage level to be generated at a particular instant (Fig. 2). In addition, the control

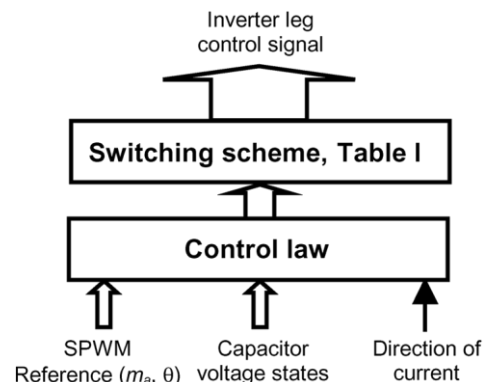
scheme requires the information about the direction of the output current of the inverter and about the capacitor voltage states, which are obtained from suitable sensors and circuits.

Suppose the desired output voltage level $V_{dc/6}$ is and the direction of current is positive, i.e., outgoing (Fig. 1). Referring to Table I, out of the four possible combinations of the switches for $V_{dc/6}$, a particular combination is chosen comparing the capacitor voltage states with respect to their reference values. Thus, the capacitor voltage level will be characterized by a logic signal, which is either high or low. The signal is high if the capacitor voltage is greater than its reference (e.g., $V_{dc/6}$ for the innermost clamping leg) and is low if it is lower. Based on this information a switching combination will be chosen, which will cause the flying capacitor voltage to increase or decrease toward its reference value. Therefore, depending upon the time interval for a particular voltage level output, the control scheme may choose more than one combination (one after another) for the same voltage level output, if the difference between the reference and the actual capacitor voltage changes its sign. If for a particular desired

voltage level, all the flying capacitors are at their reference values, the control scheme will choose the combination of switches, which will have most "NC" capacitor states (Table I).

Fig. 4. shows the inverter output phase voltage V_{an} , corresponding current (i_a) (amplified by 10 times in the plot) and the error (error) (amplified by 50 times) between the reference voltage of the innermost leg (V_{dc}) and its actual value VC_4 .

It can be seen that the capacitor C_6 either charges or discharges or remains unaffected depending on the output voltage level and the direction of current. In a similar manner all the other flying capacitor leg voltages are regulated and hence are managed to remain balance. The reference values for the



external control changes VC_1 and the dc battery is absent, the flying capacitor voltages accordingly follow their new reference values in a time that depends on the current and on the capacitors.

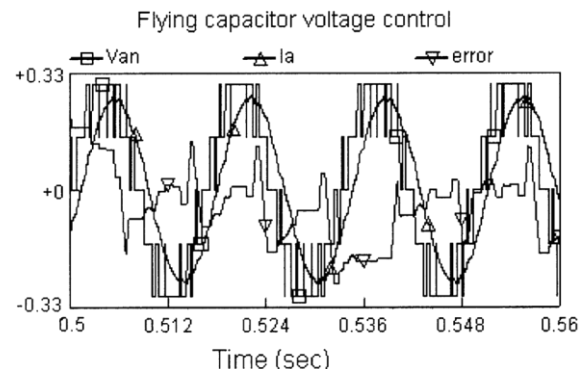


Fig. 4. Control scheme response.

flying capacitor voltages are taken with respect to the main dc-link voltage $VC_1 = V_{dc}$. Therefore, in a certain application if the

D. Block diagram for Renewable Energy System and FCMLI

This section describes the use of the STATCOM based on the Seven-level flying capacitor inverter for power oscillation damping and voltage control of power system. The study is based on renewable energy system with the STATCOM connected in shunt at the midpoint of the transmission line.

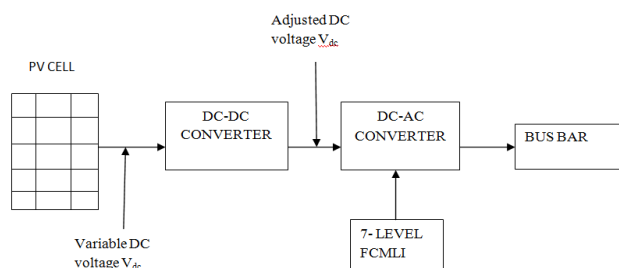


Fig.5 Block diagram of seven-level FCMLI based STATCOM

A STATCOM is a device that can provide reactive power support to bus. It is useful in improving the transient stability, power oscillation damping, voltage stability, and increase in power transfer limit of the connected power system. It consists of a voltage source inverter connected to an energy storage device on one side and to the power system on the other side. A STATCOM can be viewed as a controllable ac voltage source.

The active and reactive power transfer is caused by the voltage difference across this reactance. Usually, the inverter output voltage is almost in phase with the voltage of the ac system. Therefore, only reactive power transfer occurs, whose quantity and

sign depend on the magnitude of the inverter output voltage that

of midpoint ac voltage. If it is higher than ac voltage the reactive power is supplied to the system and if it is lower the converter circuit absorbs the reactive power. The magnitude of the inverter output voltage depends on the modulation index and dc-link voltage.

F. Block diagram of the STATCOM control scheme

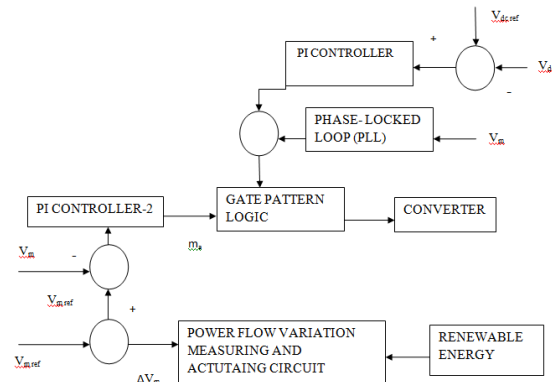


Fig 6. Block diagram of the STATCOM control scheme

There are many strategies to control the operation of STATCOM such as PI control, pole placement control and linear quadratic control. The PI control scheme has been used here to study the performance of the system. In normal operation, for the voltage control of a bus, the value of V_{mref} depends on the desired voltage profile at that particular bus; therefore, the power flow or frequency variation measuring and actuating circuits (PFFVMAC) are not needed.

The PFFVMAC block is needed when some feedback signal is taken from the power system for improving the transient stability of the system. There are two control objectives in the STATCOM control: ac-bus voltage control and dc-link voltage control. Therefore, two internal control loops containing two PI controllers are used here. The dc capacitor voltage is regulated around a reference value V_{dcref} which is kept fixed and is chosen considering the rating of the STATCOM.

Since the output voltage of the inverter and V_m should be in phase, a phase-locked loop (PLL) is used that has V_m as input and angle $Q1$ as output. Ideally, for pure reactive power exchange between the compensator and the line, the dc link voltage should remain constant. However, the capacitor discharges due to losses in switching, snubber circuits, and in transformers. Therefore, to keep the capacitor voltage constant, some amount of real power exchange is needed between the inverter and the ac system.

The PI controller-1 with an input of the error between V_{dcref} and V_{dc} and output AQ facilitates this power exchange. If the inverter output voltage is made to lag the voltage of the ac system then the active power flow is from the ac system to the dc side of the inverter charging the capacitor.

The reverse will happen when the corresponding phase relation is reversed. Another control loop (PI controller-2) generates the modulation index.

The input to this PI controller is the difference between the reference rms value V_{mref} and the actual rms value of the voltage V_m at the point of connection. Therefore, in the control system shown in Fig.6, one loop sets the angle of the injected voltage to regulate the dc capacitor voltage while the other loop sets the modulation index to generate the required voltage profile.

G. Simulation Results

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level inverter is constructed in MATLAB-Simulink software. A new strategy with reduced number of switches is employed. For 7 level inverter requires 12 switches to get seven level output voltage



Fig. 7 switching pattern of Single Phase Seven Level Inverter

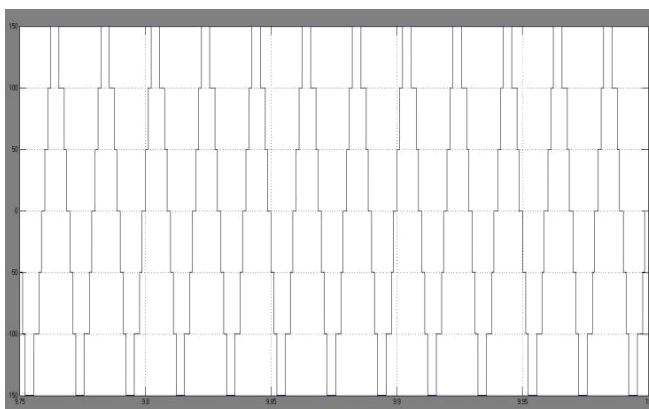


Fig. 8 Output Voltage for Single Phase Seven Level Inverter

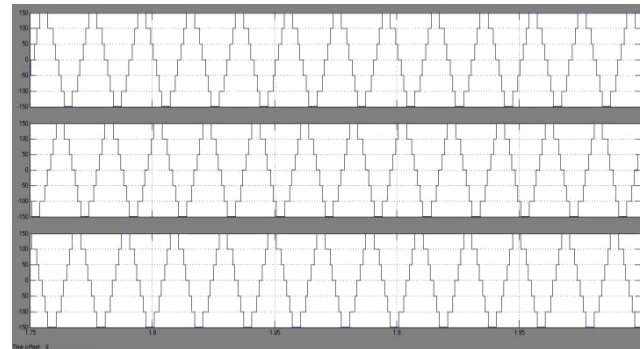


Fig. 9 Phase to ground voltage for Three Phase Seven Level Inverter

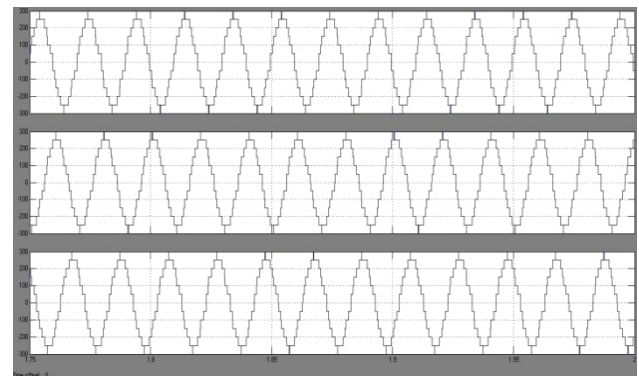


Fig. 10 Phase to Phase voltage for Three Phase Seven Level Inverter

III. CONCLUSION

In this paper, a proposal has been made for shunt compensations based on Seven - level flying capacitor inverter. The basic concepts and operational features of the inverter have been explored. A control scheme has been proposed which uses the preferential charging of flying capacitors to balance their voltages. The control scheme allows balanced flying capacitors to balance their voltages the control scheme flying capacitor voltage and, hence, output phase and line voltage as desired with much less than using the SPWM the simulation results verify the control scheme proposed. A STATCOM has been simulated based on the Seven - level inverter. The proposed STASTCOM generates output voltage waveform with lower harmonic distortion and allowed higher power handing capability. The performance of the compensation have been investigated on an simulation system. The simulation results confirm that the proposed STATCOM have satisfactory performance.

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