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FPGA Implementation of Key Components in OFDM Receiver

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ABSTRACT— Orthogonal Frequency Division Multiplexing is the technique of choice in digital broad band applications. That must cope of highly dispersive transmission media at low receiver cost. It requires very accurate frequency synchronization between the receiver and the transmitter with frequency deviation of the sub-carriers will no longer be orthogonal, causing inter-carrier interference (ICI). Therefore, OFDM has become one of most popular baseband modulation techniques of its high efficiency in combating multipath fading and its high data rate transmission capability for wireless communications. In baseband OFDM receiver consists of inner receiver and outer receiver. The inner receiver performs signal detection; carrier frequency offset (CFO) estimation, CFO compensation, symbol timing detection, cyclic prefix (CP) remove, FFT, channel estimation, channel equalization, phase tracking, phase compensation and QAM slicing. The outer receiver includes of deinterleaver, depuncturer, Viterbi decoder and descrambler. The function of OFDM outer receiver is necessary to decode the received signal and it adopts a number of area efficient hardware structures to reduce the hardware cost. The objective is to implement of OFDM baseband outer receiver in Xilinx vertex-4 Field Programmable Gate Array Logic (FPGA) and using Hardware Description Language (HDL).

KEYWORDS— OFDM, FPGA, VHDL, Outer Receiver

I.INTRODUCTION

Orthogonal frequency division multiplexing is the technique of choice in digital broad band applications of highly dispersive transmission media at low receiver cost. Therefore, OFDM has become one of most popular baseband modulation techniques of its high efficiency in Combating multipath fading and its high data rate transmission capability for wireless communications.

A literature survey shows that, Chu Yu [1] proposed architecture employs low-power register files and resource-sharing techniques. The design adopts a number of area-efficient hardware structures to further reduce the hardware cost. A.Troya [2] proposed low power synchronizer and channel estimator in inner receiver for wireless local area network. The objective of the work is the optimization, with respect to area, and the signal processing algorithms and their implementation. In [3] present efficient implementation of FFT/IFFT in OFDM applications. This design adopts a single-path delay feedback style as the proposed hardware architecture. To eliminate the read-only memories (ROM's) used to store the twiddle factors. This architecture applies a reconfigurable complex multiplier and bit-parallel multipliers to achieve a ROM-less FFT/IFFT processor that consumes lower power than the many existing works. D. A. El-Dib [4] proposed implementation adopts the "pointer" concept: a pointer is assigned to each register. Instead of copying the contents from one register to another register, the pointer which points to the first register is altered to point to the second register. The power dissipation, performance, size of the memory, and the speed of the survivor sequence management are analyzed for both the TB method, and the proposed RE method. . In this paper [5], the one-pointer VD is proposed; in that convolutional encoder initial state is known. So that the entire SMU is reduced to only one row and decoded data bits are generated in the required order, and row of memory is dispensable. The one-pointer architecture, referred as memory less Viterbi decoder (MLVD), reduces the power consumption of a traditional trace back VD by approximately 50%, but has some performance degradation. Various OFDM processors have been proposed for hardware implementation in [6]-[13].In [10] describes the design challenges and circuit implementation of a two-chip set that forms a complete 802.11a solution in CMOS technology. Zhen-dong Zhang [14] proposed a design methodology, it distributes the three permutations of an interleaver to both write address and read address. To improve the power reduction [15] proposed a radix-4 64-point pipeline FFT processor. In

order to speed up the FFT computations, more advanced solutions have been proposed using an increase of the radix. This work presents OFDM outer receiver and to implement in Xilinx vertex-4 Field Programmable Array Logic using VHDL.

II. OFDM RECEIVER

The block diagram of OFDM receiver shown in Fig.1.and it contains inner receiver and outer receiver.

In OFDM, the inner receiver performs signal detection, carrier frequency offset (CFO)estimation, CFO compensation, symbol timing detection, cyclic prefix (CP) remove, fast Fourier transform (FFT),Channel estimation, channel equalization, phase tracking, and phase compensation, and quadrature amplitude modulation (QAM) slicing (also called symbol de-mapping).

The outer receiver includes of deinterleaver, depuncturer, Viterbi decoder and descrambler. The function of OFDM outer receiver is necessary to decode the received signal and it adopts a number of area efficient hardware structures to reduce the hardware cost.

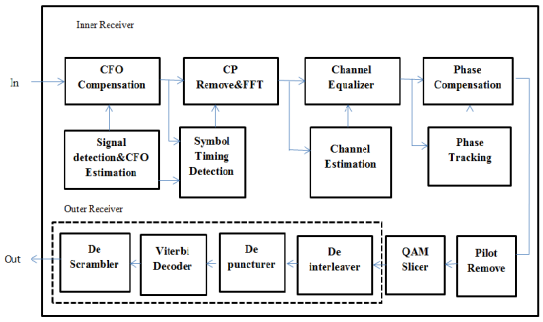


Fig.1. Block diagram of OFDM baseband receiver

III. OUTER RECEIVER

To improve power reduction, this work proposes an OFDM baseband outer receiver with low-power consumption for wireless local area networks. The proposed architecture consists a de-interleaver, de-puncturer, channel decoder, and descrambler and it reduces an area and number of hardware architecture. The following subsections describe the functions of all the modules in this design.

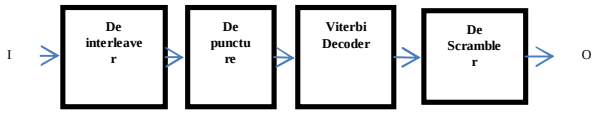


Fig.2.Block diagram of OFDM outer receiver

A.Deinterleaver & Depuncturer

To rearrange blocks of data bits by mapping adjacent coded bits into non adjacent subcarriers to protect against burst errors. The block size is the same and the number of bits is coded in a single OFDM symbol. The symbol size itself is

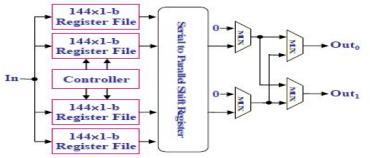


Fig.3.Block diagram of deinterleaver&depuncturer

determined by the number of data subcarriers and the modulation scheme employed. To recover the original transmitted data sequence, the deinterleaver performs an inverse operation on the interleaved data using the following algorithm:

$$S=\max(N_{BPSC}/2, \quad (1)$$

(1)

N_{BPSC} represents the coded bits in each subcarrier

B.Viterbi Decoder

The Viterbi algorithm is commonly used in a wide range of communication and data storage applications and it is used for decoding convolutional codes. The rate of convolutional coder is defined as the number of inputs bits to the output bits. Based on the Viterbi decoder (VD) algorithm, this proposes the novel VD architecture this architecture consists of a branch metric unit (BMU), a path metric unit (PMU), a add compare-select unit (ACSU), and Survivor memory unit (SMU).

The algorithm of Viterbi decoding is the branch metric unit calculation where the received data symbols are compared to the ideal output of the encoder from the transmitter. Path metric computation where the path metrics of a stage is calculated by adding the branch metric associated with the received symbol to the path metrics from the previous stage of the trellis diagram.

BMU calculates distance (metric) between the received noisy symbol and output symbol of state transition (branch) and the transition between two states is represented by a branch, which is assigned a weight, referred to as a branch metric. It measure of the likelihood of the transition, given the noisy observations. The branch metric that are accumulated along a path from path metric. For the two branches entering the same state, the branch smaller path metric survives and other one is discarded.

ACSU receives the possible branch metrics and the state metrics storage unit. An ACSU module adds each incoming branch metric of the state to the corresponding state metric compares the two results to select a smaller one and it updates the state metric storage with selected value.

In SMU responsible for keeping track of the information bits associated with the surviving paths

designated by the path metric Calculation. The basic design approaches are Register Exchange Method and Trace Back Method. In both techniques, a shift register is associated with every trellis node throughout the decoding operation. Since one of the major advantages is low power design, the proposed decoder design has been implemented using the trace back method which dissipates less power. The major disadvantage of the Register Exchange approach is that, its routing cost is very high in the case of long-constraint lengths and it requires much more resources.

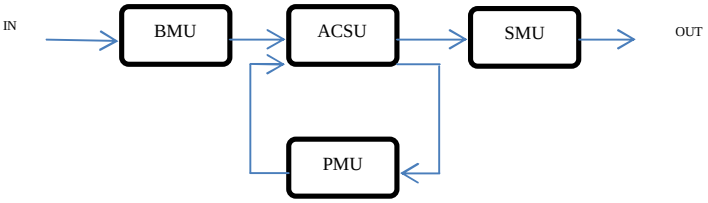


Fig.4.Block diagram of Viterbi decoder

C.Descrambler

The sequence of modulated data, and demodulated data, are no longer identical to the original data sequence provided by the data source. Then the original sequence should be restored out of the demodulated data sequence in the receiver. This operation is called descrambling is accomplished according to the rule which is the inverse of one used for scrambling and performed by a circuit called descrambler. The final stage of the OFDM receiver is a descrambler as shown in fig.

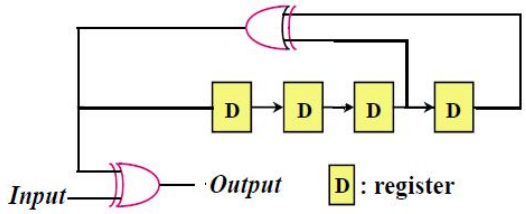


Fig.5. Block diagram of Descrambler.

The performance of data systems must be independent, the specific bit sequence to be transmitted and allowed to occur, repeated bit sequences can cause wide variations in the received power level as well as difficulties for adaptive equalization and clock recovery.

IV. RESULTS

The simulation result is done through VHDL code using Xilinx in vertex4. To observe device utilization, RTL is generated, verified and synthesized using Xilinx Synthesis Tool (XST).

Deinterleaver&depuncturer:

The deinterleaver & depuncturer,which will be better in terms of speed and occupies lesser area which in turn improves the performance of the orthogonal frequency division multiplexing communication system is to be developed.

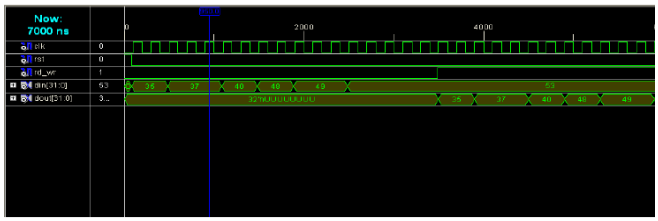


Fig.6.The above fig. shows the simulation results of deinterleaver and depuncturer. The input is given as hexadecimal value such as 35, 37,40,48,49, and its corresponding output is taken at dout.

Viterbi decoder:

The simulation results of Viterbi decoder as shown in below. To reduce the decoding complexity Viterbi decoder is used and it improves the decoding speed.

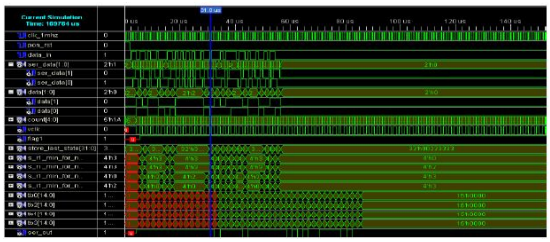
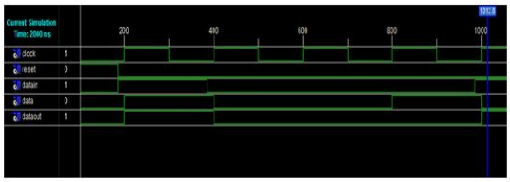


Fig.7.The above fig.shows the simulation results of Viterbi decoder and the input message is given as 010101010101 and the output is taken from der_out.

Descrambler

The bit of the message stream enters the register and shift from one stage to next when clock is applied. The performance of data transmission systems must be independent of the specific bit sequences being transmitted. Since all the problems are eliminated if the bit sequence is random.



F ig.8.Simulation waveform of descrambler as shown. The bit of the message stream (01100001) enters the register and shift from one stage to next when clock is applied and the output is taken as the same as the descrambling action.

DEVICE UTILIZATION SUMMARY:

The device XCSVFX140, Vertex 4 is used. The device utilization summary of deinterleaver &depuncturer and Viterbi decoder as shown. Which its gives the details of number of devices used from the available devices and also represented in %. Hence as the result of the synthesis process and the device utilization

used device and package as represented. This device utilization includes Logic utilization, Logic distribution and Total gate count for the design.

Device utilization	Used	Available	%utilization
No.of slices	6975	63168	11%
No.of slice utilization	466	126336	1%
No.of LUTs	13586	126336	10%
No.of bonded IOBs	14	768	2%
No.of GCLKs	2	32	6%

Table.1.Device utilization of deinterleaver&depuncturer

Device utilization	Used	Available	%utilization
No.of slices	36658	63168	58%
No.of slice utilization	38567	126336	30%
No.of LUTs	35869	126336	28%
No.of bonded IOBs	212	768	27%
No.of GCLKs	3	32	3%

Table.2.Device utilization summary of Viterbi decoder

V. CONCLUSION

The proposed design uses a number of area-efficient structures, such as hardware. The outer receiver includes of deinterleaver, depuncturer, Viterbi decoder and descrambler. The function of OFDM outer receiver is necessary to decode the received signal and it adopts a number of area efficient hardware structures to reduce the hardware cost. The objective is to implement of OFDM baseband outer receiver in Xilinx vertex-4 Field Programmable Gate Array Logic (FPGA) and using Hardware Description Language (HDL).

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