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FPGA Design of Reconfigurable Binary Processor Using VLSI

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Abstract—Binary image processing is a powerful tool in many image and video applications. In this paper we proposed efficient hardware architecture of Binary image processor for low power applications and also propose an Efficient Majority Logic Fault Detection algorithm on binary image processor to reduce the error rate. Binary image processor's architecture is a combination of input and output control units, reconfigurable binary processing module, processor control unit, register group and bus interfaces. The reconfigurable binary processing module consists of mixed-grained reconfigurable binary compute units and output control logic and it also performs mathematical morphology operations. The simulation and experimental results demonstrate that the processor is suitable for real-time binary image processing applications. The proposed binary processor is designed using Verilog HDL, simulated using Modalism software and synthesized using Xilinx project navigator.

Keywords—Binary image processing, field programmable gate array(FPGA), mathematical morphology, mixed grained, real time, reconfigurable.

I. INTRODUCTION

BINARY IMAGE processing is extremely useful in various areas, such as tracking, object recognition, motion detection and machine intelligence, image analysis and understanding, video processing, computer vision identification and authentication systems [1]-[5]. Binary images are images whose pixels have only two possible intensity values (0 or 1).It assigns a 0 for black and a 1 for white. In binary image processing, such processors are inefficient and difficult. The formations of binary images are obtained by thersolding the gray scale images. The important characteristics of binary images are distance transform. High-speed implementation of binary image processing operations can be efficiently realized by using chips specialized for binary image processing. In this paper, we present reconfigurable binary image processor is a microprocessor with erasable hardware that can rewrite itself dynamically and also can transform itself from a video chip into central processing unit (CPU) to a graphics chip. Mathematical morphological operations were presented to perform the reconfigurable binary image processing chips. A reconfigurable binary image processor incorporating eight macro processing element is implemented to support real time change detection and background registration based on video and object segmentation algorithm. The advantages of binary Image processors are simple structure, less expensive, high Speed and wide application range

II. RELATED WORKS

In this paper, there are several types of traditional methods are Application-specific chip, SIMD (single Instruction multiple data), Dual rail encoding methodology and Edge detection algorithm. Application-specific chip and hardware have been reported for various applications. It designed for a special application, including environmental monitoring, auto emission control, and personal digital assistants (PDAs).In 500-dpi cellular-logic processing array was implemented to verify and enhance fingerprint images [6]. The reconfigurable technique can bridge the gap between flexibility and application-specific chip. The major drawback of application-specific chips is the lack of flexibility, Complex architecture and High power consumption. In space dependent binary image processing was presented in MIPA4K to identify the local binary patterns [7]. Programmable analog vision processors based on the cellular neural or nonlinear

network universal machine architecture were proposed for a wide range of applications such as motion analysis and texture classification [8].A programmable single instruction multiple data SIMD (single instruction multiple data) real-time vision chip was presented to achieve high-speed target tracking [9]. It is particularly applicable to common tasks like adjusting the contrast of digital image or adjusting the volume of digital audio. It is a class of parallel computers in taxonomy and also it describes computers with multiple processing elements that perform the same operation on multiple data points simultaneously, such machines are exploiting data level parallelism. Most modern CPU designs include SIMD Instructions in order to improve the performance multimedia use. The major drawbacks of SIMD Methods are, it has large register files, high power consumption and large chip area, high error date recovery. In SIMD instructions were implementing an algorithm usually requires human labor, then most compilers do not generate a SIMD instruction from a typical c program and for instance factorization in compilers is an acre area of computer science vector. Programming with particular SIMD instructions sets can involve numerous low level challenges.

Two rail encoding methodology provides a method to enhance the security properties of a system making DPA. The major drawbacks of Two rail encoding method for generically securing circuit against the frame work in which we analysis the encoding systems and taint about the target system and limitation of equipment. Portable surveillance camera architecture [10] requires too many components and is too complicated for portable applications; lack of flexibility, large area, and high elapsed time for data recovery. Recently, a vision chip with the architecture of a massively parallel cellular array of processing elements was presented for image processing by using the asynchronous or synchronous processing technique [11].

In a high-resolution pixel-parallel SIMD vision chip the silicon area available for each processing element is very limited. Vision system technology that can achieve ultimate performance must be created in order to pioneer new applications. The vision chip integrates image sensors with processing elements (PEs) in one chip and performs real-time parallel image processing. The main disadvantage of this method it is difficult to perform complex calculations and algorithms that are currently performed in DSP or general-purpose computers. Some chips have limited application range. Other general-purpose chips have the architecture of a digital processor array, in which each digital processor handles one pixel. When the chips will become extremely large so large sized images are processed. To overcome these methods we have presented a binary image processor they were needed to design a less expensive, fast execution, small area and wide application range and also it is suitable for real-time binary image processing.

III. Proposed Architecture

In this paper we proposed efficient hardware architecture of Binary image processor for low power applications and also propose an Efficient Majority Logic Fault Detection algorithm on binary image processor to reduce the error rate. The proposed architecture is designed for applications in image or video processing, computer vision, machine intelligence, and identification and authentication systems

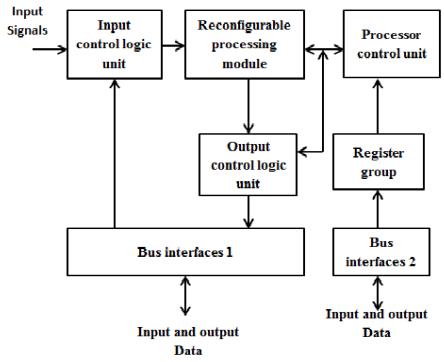

Fig.1.Architecture of binary image processor

A. Reconfigurable Processing Module

The diagram of the reconfigurable binary processing module (RBPM) is given in Fig. 2. It can be divided into two main parts they are output control logic and input data. The first part is the output control logic, they selects the output from all the binary compute unit outputs according to the given parameters and converts the series data of 1-b binary images into parallel data.

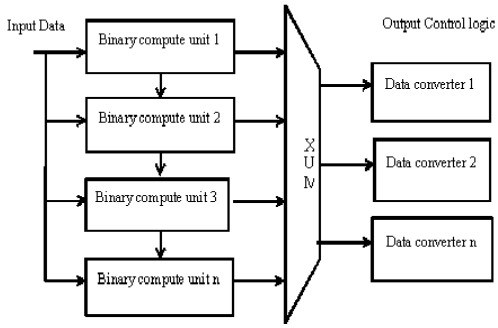

Fig.2 Reconfigurable processing module

The second part consists of several binary compute units (1, 2…n). It can perform binary logic and binary image operations at a high speed. Binary compute unit contains two binary compute elements; four multiplexer's and binary set operation as shown in Fig.3a

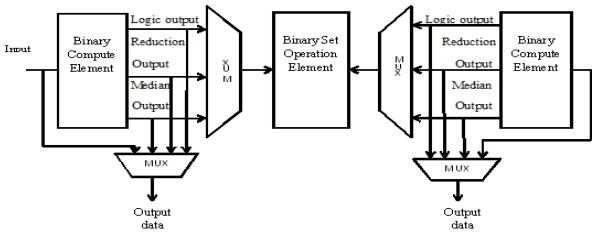

Fig. 3(a)Architecture of binary compute unit

Left side binary compute element produces three outputs are going to the multiplexer they are logic output, reduction output, and median output. These output and input signals passes through the input of bottom multiplexer and then produces output data and also that the similar operation on the right side of the binary

compute element. These two multiplexers of output feeding through the input as binary set operation element. Binary compute unit has mixed grained architecture.Mixed-grained reconfigurable architecture consisting of fine-grained and coarse-grained fabrics, each of which can be con figured for different levels of reliability depending on the reliability requirement of target application. It supports both behavioural synthesis and flexible reliability. Binary compute units can be executed in parallel manner and is decided by configurable registers. Set operation element can perform in binary set operations.

Binary compute element consists of line memory, two multiplexer, registers, binary logic element, reduction element and median output element as shown in fig.3 (b).The input of the image signals passes through line memory to multiplexer and also single random access memory (SRAM), registers to multiplexer. The output of the first multiplexer going to register (a1, a2, a3) and second multiplexer going to register (b1, b2, b3).These registers are feed to three Binary logic element. It can perform Logic gate operations and straight through output but second and third binary logic element produces reduction output and median output via reduction element and median filter. Reduction element can perform reduction logic gate operations. Median filters. Binary compute element has coarse grained architecture, some examples of reconfigurable binary processing module in pipelined manner. They are RBPM is reconfigured to an eight-stage pipelined architecture, two four-stage pipelined architectures such that two images can be processed simultaneously.

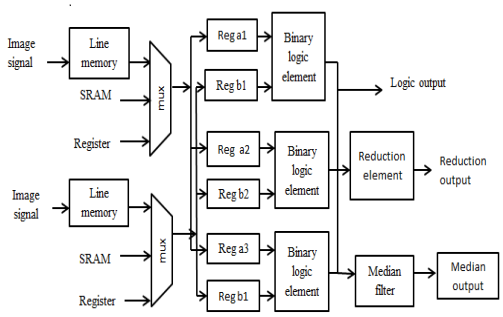

Fig. 3(b) Architecture of the binary compute element

The reconfigurable architecture provides higher hardware utilization and also process times are 1/8 than the pipelined architecture. It consists of two types they are fine-grained and coarse grained. Fine grained corresponds to the bit level, coarse grained corresponds to the world level basically, coarse-grained systems will have less method calls than a fine-grained system. Clearly coarse-grained methods will be fewer and do more work than the broken-down fine-grained versions. The mixed-grained architecture is more flexible and efficient, fewer reconfiguration parameters than the coarse-grained architecture, fine-grained architecture.

B. Input and Output Control Logic Unit

Input and output control logic is a part of binary image processor architecture. It contains two down sampling, four data converters, and two first in first output, synchronization circuit. Image signals passes through down sampling, data converter to multiplier then inputs are selected from parameters in SRAM, register. Data converters 1 and 2 convert 1binary image signals in to 32 bit parallel data. Data converter 3 and 4 convert the 32 bit parallel data in to 1 binary image signals.

Conventionally, digital colour images are represented by setting specific values of the colour space coordinates for each pixel. Colour spaces with decoupled luminance and chrominance coordinates (YUV type) allow the number of bits required for acceptable colour description of an image to be reduced. This reduction is based on greater sensitivity of the human eye to changes in luminance than to changes in chrominance. The main approach is to set individual value of luminance component to each pixel, while assigning the same colour (chrominance components) to certain groups of pixels (sometimes called *macro pixels*) in accordance with some specific rules. This process is called *down sampling* and there are different sampling formats depending on the underlying scheme. To increase the processing rate, two down sampling circuits are added to down-sample image signals before they are processed by the data converters 1 and 2.

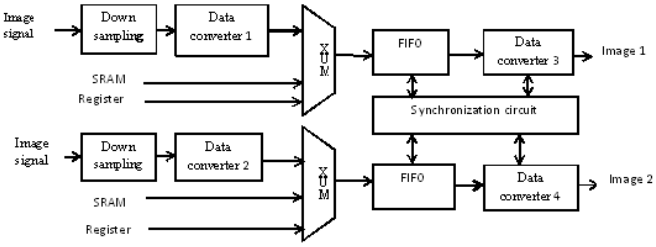

Fig.5 Block diagram of Input and output Control logic Unit

C. Processor Control Unit, Register Groups and Bus Interfaces

Processor control unit is a multipurpose series of industrial control products that are field programmable for solving various applications. Configuration registers can read the configuration information in processor control unit and also controls the components of binary image processor architecture. Register group is an important part of the proposed architecture. It contains interaction information, reconfigurable information and control parameters. Bus interfaces can transfer the data

D. Mathematical Morphology Operations

Mathematical morphology is set theory-based methods of image analysis and plays an important role in many digital image processing algorithms and applications, e.g., noise filtering, image analysis or pattern recognition. But it can be employed as well as on graphs, surface meshes, solids and many other spatial structures. The basic binary morphological operations are dilation, erosion and based on set theory, lattice theory and random functions. It has two operands on each operation The other binary morphological operations such as opening, closing, hit-and-miss operation are based on various combinations of the two basic operations, dilation, and erosion.it based on the algebra of nonlinear operator operating on the object shape and also yields fast algorithm. Applications of binary

morphology operations are shape simplification; shape enhancing, skeletonizing, thinning and thicking.

Fig. 5(a) Input image

0	0	1	0	0
0	0	1	0	0
1	1	1	1	1
0	0	1	0	0
0	0	1	0	0

(b) structuring element

Dilation expands the connected sets of 1s of binary image. It can be used for expanding shapes, filling holes, gaps and gulfs. Erosion shrinks the connected sets of binary image. It can be used for shrinking shapes, removing bridges, branches and small protrusions.

(c) Dilation

(d) erosion

Closing is the compound operation of dilation followed by erosion. Opening is the compound operation of erosion followed by dilation

(e) Opening

(f) closing

IV. Simulation Results

The results are obtained after carrying out the experimentation by using the following tools. They are Modalism 5.5e for simulation, Xilinx FPGA Navigator 9.2i for synthesis. Fig.5 (a) shows technology schematic view, (b) RTL Schematic view, (c) internal circuit of LUT (look up table).In this paper coding is present in behavior level modeling. This is the highest level of abstraction provided by Verilog HDL, so we can easily design and manipulating. Behavioral level modeling is that creating of output in image. A module can be implemented in terms of the desired design algorithm without concern of the hardware implementation details. Designers need to be able to evaluate the trade-offs of various architecture and algorithms before they decide on the optimum architecture and algorithm to implement in hardware.

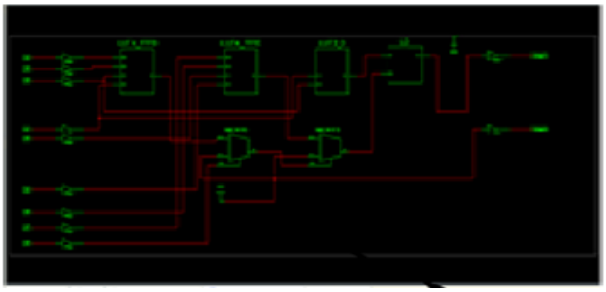

Fig.5.technology schematic view

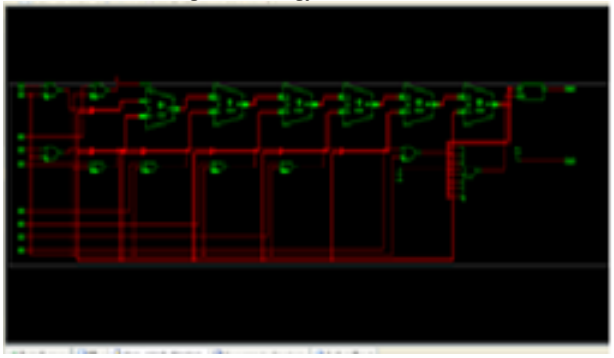

Fig.6.RTL Schematic view

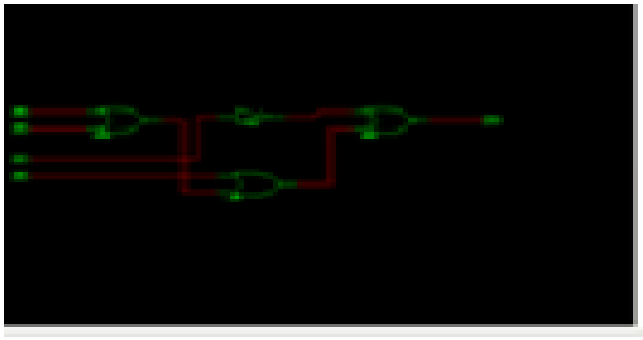

Fig.7 Internal circuit of LUT

Table 1
Performance Evolution

s.no	Parameters	Existing methods		1-D MIMD(proposed)
		SIMD(1-D)	ASIP	
1	Power Consumption	278mw	260mw	158.95mw
2	Latency	7.6ns	6.9ns	4.368ns
3	Gate Counts	700	670	400
4	Speed	low	median	high

In Table 1 performance evaluation of parameters between existing methods and proposed methods. Parameters are power consumption, latency, gate counts, and speed. The architecture comparison shows that the 2-D SIMD array is suitable for processing small fixed-resolution images.The1-D array application-specific instruction set processor (ASIP) in has a large chip area. In this paper presented in 1-D MIMD array has high performance, low power consumption, and small area.

V. CONCLUSION

In this paper we proposed efficient hardware architecture of Binary image processor for low power applications and also propose an Efficient Majority Logic Fault Detection algorithm on binary image processor to reduce the error rate. The architecture uses the 1-D MIMD array and suitable to perform real time binary image processing. The binary image processor architecture contains input control logic unit, reconfigurable processing module, processor control unit and register group. The reconfigurable processor has a mixed-grained architecture it has the characteristics of high flexible and performance and can also perform the Basic mathematical morphology operations. The processor, featured by a binary image processor they were needed to design a less expensive, fast execution, small area and wide application range high speed, simple structure.

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