

FPGA Implementation of Digital Modulation Schemes

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ABSTRACT— Software Defined Radio (SDR) has been one of the new techniques developed to change the way the traditional wireless communication system work. This paper deals with the Field-programmable gate-array (FPGA) implementation of Digital Modulator such as Quadrature amplitude modulation (QAM), Binary amplitude-shift keying (BASK), Binary frequency shift keying (BFSK) and Binary phase-shift keying (BPSK). Since digital modulation is more secure and more efficient in long-distance transmission and noise detection and correction than its analog counterpart, it has an important place in modern communications. They employ the minimum number of blocks necessary for achieving the modulation. The input carrier signal and message signal are generated using CO-ordinate Rotation Digital Computer (CORDIC) algorithm. These digital modulators were developed and compiled to a Very high speed integrated circuit Hardware Description Language (VHDL) net list, and were later implemented individually into Spartan 3 FPGA board.

KEYWORDS— Software Defined Radio (SDR); Field-programmable gate-array (FPGA); Quadrature amplitude modulation (QAM); Binary amplitude-shift keying (BASK); Binary frequency shift keying (BFSK) ; Binary phase-shift keying (BPSK) ; CO-ordinate Rotation Digital Computer (CORDIC)

I. INTRODUCTION

Field-programmable gate arrays (FPGAs) are semiconductor device that contains programmable logic elements (LEs) and reconfigurable interconnects to realize any complex combinational or sequential logic functions. Hardware implemented in an FPGA can be reconfigured by programming the logic elements and interconnections for specific applications, even after the installation of the

product. Today's FPGAs has static random-access memories (SRAMs), high-speed transceivers, high-speed

input/output (I/O) elements and hard-embedded processors.

A literature survey shows that, FPGAs are widely used in different applications, such as motor controllers [1], neural network implementations [2-4], finite-impulse-response (FIR) filter realization [5,6], fuzzy-logic controllers [7], etc. Implementation of digital modulation and demodulation using FPGAs has received considerable attention. Signal-processing systems such as software-defined radios (SDRs) can receive various kinds of modulated signals via software programming using digital signal processors (DSPs), FPGAs, general purpose processors (GPPs), and application specific integrated circuits (ASICs) [8,9]. In this context, FPGAs are the solution, due to their high flexibility and high speed [9].

Since digital modulation is more secure and more efficient in long-distance transmission. Moreover noise detection/correction is easier than analog, hence it has an important place in modern communications. A digital receiver for software-defined radios based on QAM techniques [10,11]; and BASK, BPSK, and BFSK [14,15] digital modulators to be used in communications systems [12,13]. All of these papers have in common the design of models in the MATLAB environment, Verilog HDL or VHDL and implementations using FPGAs.

The objective of this paper is to implement a fully digital QAM, BASK, BFSK, and BPSK modulators that employ the minimum number of digital blocks suitable for software-defined radio systems and are implemented individually into the Spartan 3 FPGAs. The input carrier signal and message signal are generated using COordinate Rotation DIGital Computer (CORDIC) algorithm, for more scalability or flexibility.

The paper is organized as follows. Section II, explains the theory of the QAM, BASK, BFSK, and BPSK modulations. Section III, explains the generation of input signal using CORDIC algorithm. Section IV deals with results and discussions and finally section V concludes this paper.

II. THEORY of the DIGITAL MODULATIONS

A. Quadrature Amplitude Modulation

Quadrature amplitude modulation (QAM) is a modulation scheme in which two sinusoidal carrier signals, one exactly 90 degrees out of phase with respect to the other, are used to transmit data over a physical channel. Because the orthogonal carrier signal occupy the same frequency band and differ by a 90 degree phase shift, each can be modulated independently and transmitted over the same frequency band. Finally it is separated by demodulation at the receiver. For a given bandwidth, QAM transmits data at twice the rate of standard pulse amplitude modulation (PAM) without any degradation in the bit error rate (BER). QAM and its derivatives are used in both mobile radio and satellite communication. These two carrier waves represent the in-phase (I) and Quadrature-phase (Q) components of our signal. These signals can be represented as

$$I = A\cos(\phi) \text{ and } Q = A\sin(\phi) \quad (1)$$

A QAM signal can be expressed as

$$A\cos(2\pi f_c t + \phi) = I \cos(2\pi f_c t) - Q \sin(2\pi f_c t) \quad (2)$$

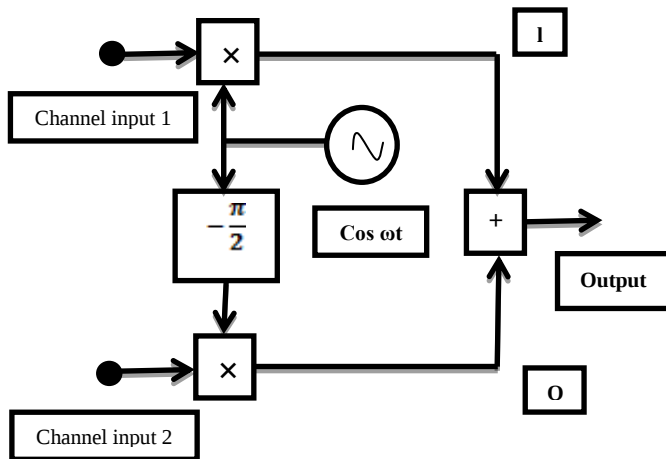


Fig. 1 A block diagram of QAM modulation

B. Binary Amplitude-Shift Keying Modulation

In a BASK (binary amplitude-shift keying) modulation, the amplitude of the sinusoidal carrier signal is in accordance with the message level ("0" or "1"), while keeping the frequency and phase constant. A block diagram of the BASK modulation and its signal waveforms are shown in Fig 2 and 3, respectively. Since there are sharp discontinuities at the transition points, the resulting BASK signal has an unnecessarily wide bandwidth. The band pass filter shown in Fig 2 removes the high-frequency components of the BASK signal. The

output is a band limited signal, ready for transmission by a power amplifier. BASK signal can be expressed as

$$S_{BASK}(t) = m(t) A \sin(2\pi f_c t + \Phi_0), 0 \leq t \leq T \quad (3)$$

Where $m(t) = 0$ or 1 (the binary message), T is the bit duration, and A , f_c , and Φ_0 are the amplitude, frequency, and phase of the sinusoidal carrier signal. The modulated signal has a power $P = A^2/2$ for both the states.

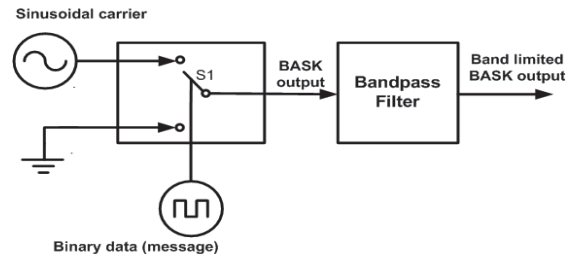


Fig. 2 A block diagram of BASK modulation.

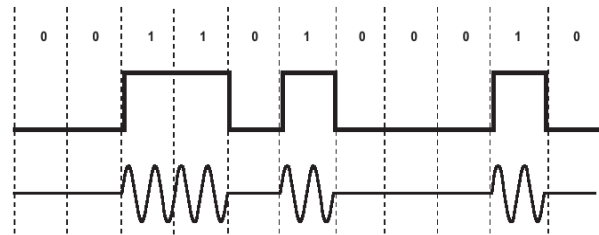


Fig. 3 The modulating-signal (message) and the BASK Signal waveforms

C. Binary Frequency-Shift Keying Modulation

In a BFSK (binary frequency-shift keying) modulation, the frequency of the sinusoidal carrier signal is in accordance with the message level ("0" or "1") while keeping the amplitude and phase constant. A block diagram of the BFSK modulation and its signal waveforms are shown in Fig 4 and 5 respectively. A BFSK signal can be expressed as

$$S_{BFSK}(t) = A \sin\{2\pi[f_c + m(t)f_m]t + \Phi_0\}, 0 \leq t \leq T \quad (4)$$

Where $m(t) = 0$ or 1 (the binary message), T is the bit duration, and A , f_c , and Φ_0 are the amplitude, frequency, and phase of the sinusoidal carrier signal. The modulated signal has a power $P = A^2/2$ for both the states.

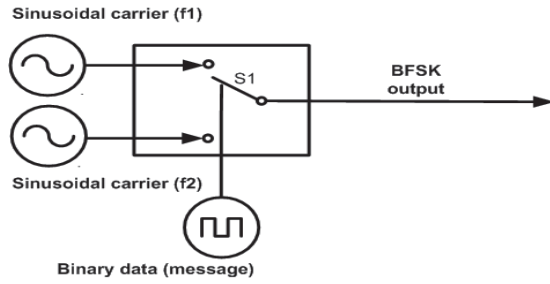


Fig. 4 A block diagram of BFSK modulation

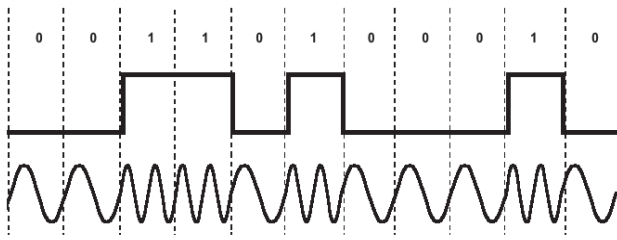


Fig. 5 The modulating-signal (message) and the BFSK Signal waveforms

D. Binary Phase-Shift Keying Modulation

In a BPSK (binary phase-shift keying) modulation, the phase of the sinusoidal carrier signal is in accordance with the message level ("0" or "1") while keeping the amplitude and frequency constant. A block diagram of the BPSK modulation and its signal waveforms are shown in Fig 6 and 7, respectively. A BPSK signal can be expressed as

$$S_{BPSK}(t) = A \sin[2\pi f_c t + m(t)\pi], 0 \leq t \leq T \quad (5)$$

Where $m(t) = 0$ or 1 (the binary message), T is the bit duration, and A , f_c , and Φ_0 are the amplitude, frequency, and phase of the sinusoidal carrier signal. The modulated signal has a power $P = A^2/2$ for both the states.

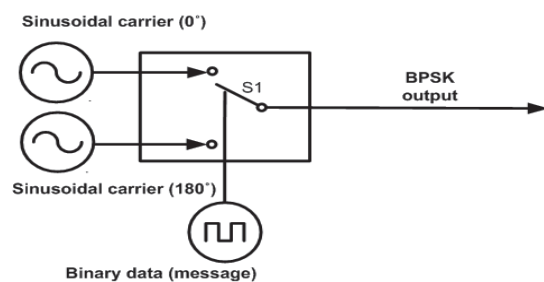


Fig 6. A block diagram of BPSK modulation

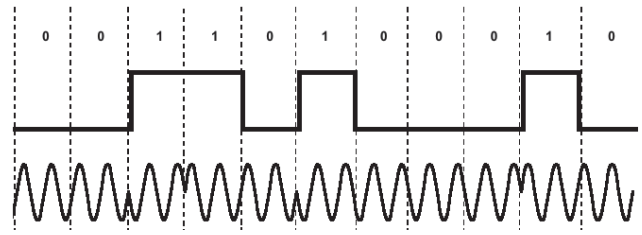


Fig7. The modulating-signal and BPSK signal waveforms

III. GENERATION of INPUT SIGNAL USING CORDIC

In this paper CORDIC algorithm is used to design a digital sine waveform generator. There are plenty of applications which require digital wave generators. Wireless and mobile systems are among the fastest growing application areas; in particular, Software Defined Radio (SDR) is currently a focus of research and development. An SDR system allows performing many functions based on a single hardware platform, thus highly reconfigurable resources for signal processing are needed, mainly for modulation of digital signals. Fourth generation (4G) wireless and mobile systems are currently the focus of research and development. They will allow new types of services to be universally available to consumers and for industrial applications. Broadband wireless networks will enable packet based high data rate communication suitable for video transmission and mobile Internet applications.

A. The CORDIC Algorithm

CORDIC is based on the common rotation equations:

$$\begin{aligned} x' &= x \cdot \cos \phi - y \cdot \sin \phi = \cos \phi \cdot [x - y \cdot \tan \phi] \\ y' &= y \cdot \cos \phi + x \cdot \sin \phi = \cos \phi \cdot [y + x \cdot \tan \phi] \end{aligned} \quad (6)$$

If $\tan \phi = \pm 2^i$, multiplication in (6) can be performed by a simple shift operation. This allows the vector to be rotated by desired angle in a sequence of smaller rotations by angle $\phi_i = \pm \tan^{-1}(2^{-i})$

$$\begin{aligned} x_{i+1} &= k_i [x_i - y_i \cdot d_i \cdot 2^{-i}] \\ y_{i+1} &= k_i [y_i + x_i \cdot d_i \cdot 2^{-i}] \end{aligned} \quad (7)$$

Where,

$$k_i = \cos(\tan^{-1}(2^{-i})) = \frac{1}{\sqrt{1 + 2^{-2i}}}, d_i = \pm 1$$

B. Modes of The CORDIC Algorithm

CORDIC rotator works in two modes: rotation and vectoring

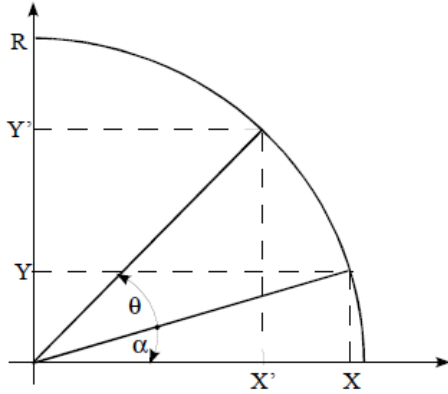


Fig. 8 The Rotation (X' , Y') and vectoring (X , Y) modes of the CORDIC algorithm

In the first mode it rotates the input vector by specified angle. The angle accumulator is initialized with the desired rotation angle. For this mode, CORDIC equations are:

$$\begin{aligned} x_{i+1} &= x_i - y_i * d_i * 2^{-i} \\ y_{i+1} &= y_i + x_i * d_i * 2^{-i} \\ z_{i+1} &= z_i - d_i * \tan^{-1}(2^{-i}), \end{aligned} \quad (8)$$

Where,

$$d_i = \begin{cases} -1, & z_i < 0 \\ 1, & \text{otherwise} \end{cases}$$

This gives the following result:

$$\begin{aligned} x_n &= A_n \cdot [x_0 \cos z_0 - y_0 \sin z_0] \\ y_n &= A_n \cdot [y_0 \cos z_0 - x_0 \sin z_0] \\ z_n &= 0 \end{aligned} \quad (9)$$

Where,

$$A_n = \prod_n \sqrt{1 + 2^{-2i}}$$

In the vectoring mode input vector is being rotated to the x axis while recording the angle required to make that rotation. The result of the vectoring operation is a rotation angle and the scaled magnitude of original vector. The CORDIC equations in this mode are:

$$x_{i+1} = x_i - y_i * d_i * 2^{-i}$$

$$\begin{aligned} y_{i+1} &= y_i + x_i * d_i * 2^{-i} \\ z_{i+1} &= z_i - d_i * \tan^{-1}(2^{-i}) \end{aligned} \quad (10)$$

Where,

$$d_i = \begin{cases} -1, & z_i < 0 \\ 1, & \text{otherwise} \end{cases}$$

Then:

$$\begin{aligned} x_n &= A_n \sqrt{x_0^2 + y_0^2} \\ y_n &= 0 \\ z_n &= z_0 + \tan^{-1}\left(\frac{y_0}{x_0}\right) \\ A_n &= \prod_n \sqrt{1 + 2^{-2i}} \end{aligned} \quad (11)$$

The CORDIC algorithm in every mode is limited between

$$-\frac{\pi}{2} \text{ and } \frac{\pi}{2}.$$

This limitation is caused by the first rotation angle $\phi_0 = \tan^{-1}(2^0)$

To achieve simplicity of hardware realization, the idea used in CORDIC are to (i) decompose the rotations into a sequence of elementary rotations through predefined angles that could be implemented with minimum hardware cost; and (ii) to avoid scaling, that might involve arithmetic operations such as square-root and division. The other idea is based on the fact the scale-factor contains only the magnitude information but no information about the angle of rotation [16].

IV RESULTS and DISCUSSIONS

The Digital modulation schemes such as of quadrature amplitude modulation (QAM), binary amplitude-shift keying (BASK), binary frequency shift keying (BFSK) and binary phase-shift keying (BPSK) were designed separately using Xilinx ISE 14.1 tool and its simulated results are shown below.

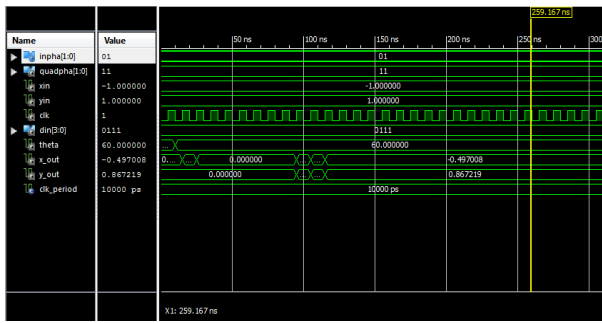


Fig. 9 The above figure shows the simulation result of QAM, where x_{in} , y_{in} represents the input signal and x_{out} & y_{out} represents the modulated signal. 0111 is given as the input and its corresponding output obtained is -0.49 & -0.86 which is same as that of manual calculation.

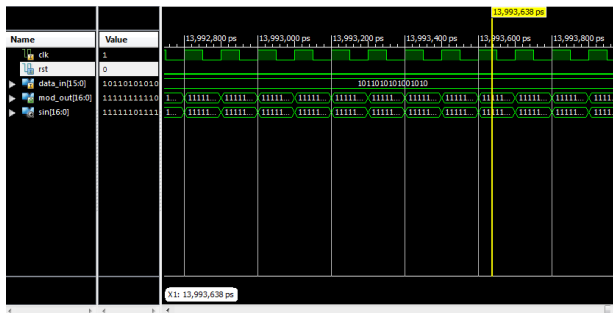


Fig. 10 The above figure shows the simulation result of BASK, where $data_{in}$ represents the input signal and mod_{out} represents the modulated BASK output signal. 10110101010 is given as the input and 11111111110 is the modulated output.

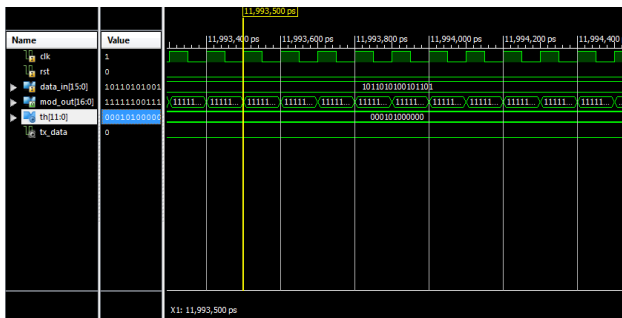
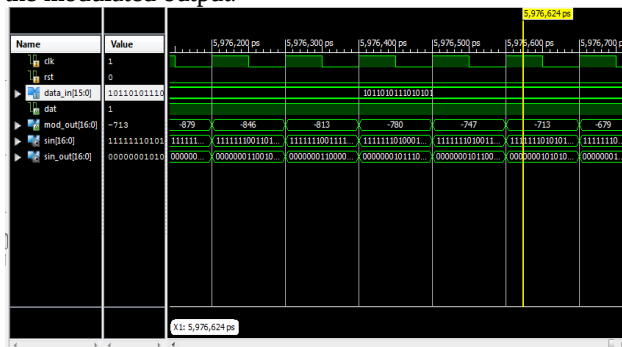


Fig. 11 The above figure shows the simulation result of BFSK, where $data_{in}$ represents the input signal and mod_{out} represents the modulated BFSK output signal. 10110101001 is given as the input and 11111100111 is the modulated output.



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Fig. 12 The above figure shows the simulation result of BPSK, where $data_{in}$ represents the input signal and mod_{out} represents the modulated BPSK output signal. By varying the phase, the modulated BPSK signal is obtained.

These modulators which are designed is implemented separately using Spartan 3 XC3S100E FPGA board.



Fig. 13 Implementation on Spartan 3 XC3S100E device.

The device Spartan 3 XC3S100E utilization memory for all the Digital modulators are shown in table which gives the total resources utilized.

TABLE I

DEVICE UTILIZATION of DIGITAL MODULATORS

LOGIC UTILIZATION	USED	AVAILAB LE	UTILIZATION
No. of Slices	692	960	72%
No. of Slice Flip Flops	125	1920	6%
No. of 4input LUTs	1326	1920	69%
No. of bonded IOBs	35	108	32%
No. of GCLKs	1	24	4%

V. CONCLUSION

FPGA implementations of QAM, BASK, BFSK, and BPSK digital modulators were demonstrated. The main advantages of the implementations were the minimum numbers of digital blocks used for performing digital modulations. The input signals for all these digital modulators were generated using CORDIC algorithm and corresponding output signals are obtained in digitized form. These design entry is done through VHDL coding in Xilinx environment and finally all these modulators were implemented separately using Spartan 3 FPGA.

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